Variability from Equipment to Circuit: The Horizon2020 Project SUPERAID7

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OUTLINE

- Introduction
- Consortium and project data
- Project structure
- Methodology used
- Topography Simulation for Advanced 3D Devices
- Interconnect Variability Simulation
- Some further glimpse on first results
- Conclusion

Introduction: Objectives of the SUPERAID7 Project

- Full project name ”Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7nm node”
- Development of a software system for the simulation of the impact of systematical and statistical process variations for advanced extended CMOS devices and interconnects
- Build on the results from SUPERTHEME
- Close interaction with leading European technology development projects (esp. KET Pilot Lines) via partner CEA/Leti and some members of the SUPERAID7 Industrial and Scientific Advisory Board
- Continued attention on data reduction / hierarchical simulation – from discretization of equipment to compact models – and on correlations
- Specific focus on advanced integrated topography simulation, carrier transport models for nanowire transistors and/or alternative channel materials, interconnect modeling and simulation

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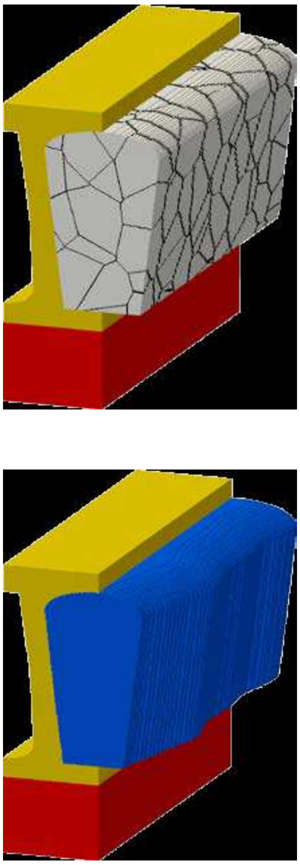
Introduction: Variations to be studied

- Various systematic variations occuring in most process steps
  - Variations in topograpohy steps especially important for 3D devices
- Layout effects – example Double Patterning
- *Statistical varitions directly affecting transistor behavior: RDF, MGG, LER/LWR*
- Interconnect variability: MGG, LER/LWR

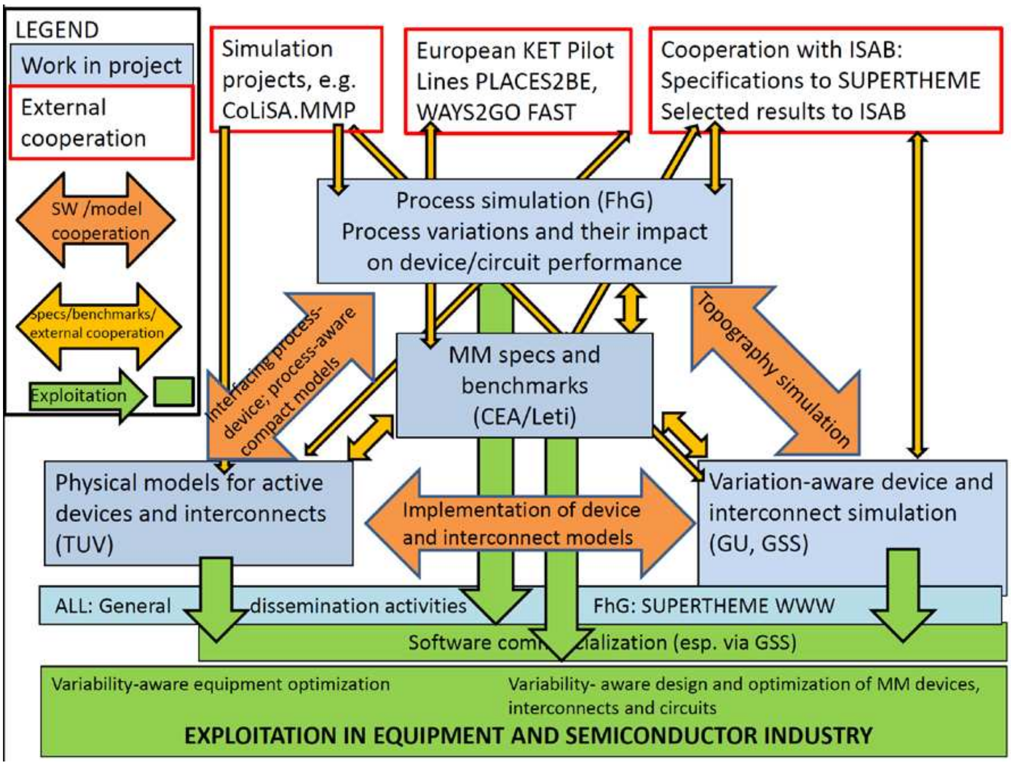


Figures: Copper granularity and LER in interconnects (from Glasgow University)

Consortium and Project Data

- Coordinator: Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany
- Further project partners
  - SW house: GSS (now a Synopsys company), Glasgow, UK
  - Research institute: CEA/Leti, Grenoble, France
  - Universities: Univ. Glasgow, UK; TU Wien, Austria
- Project period: 01/2016 – 12/2018
- EC funding: 3,377,527.50 € from Horizon 2020 ICT25 Call “Generic micro- and nano-electronic technologies“
- See www.superaid7.eu

SUPERAID7 Project Structure



LEGEND
Work in project
External cooperation
SW /model cooperation
Specs/benchmarks/ external cooperation
Exploitation 🟩

Simulation projects, e.g. CoLiSA.MMP

European KET Pilot Lines PLACES2BE, WAYS2GO FAST

Cooperation with ISAB: Specifications to SUPERTHEME Selected results to ISAB

Process simulation (FhG) Process variations and their impact on device/circuit performance

Interfacing process-device; process-aware compact models

MM specs and benchmarks (CEA/Leti)

Topography simulation

Physical models for active devices and interconnects (TUV)

Implementation of device and interconnect models

Variation-aware device and interconnect simulation (GU, GSS)

ALL: General dissemination activities

FhG: SUPERTHEME WWW

Software com alization (esp. via GSS)

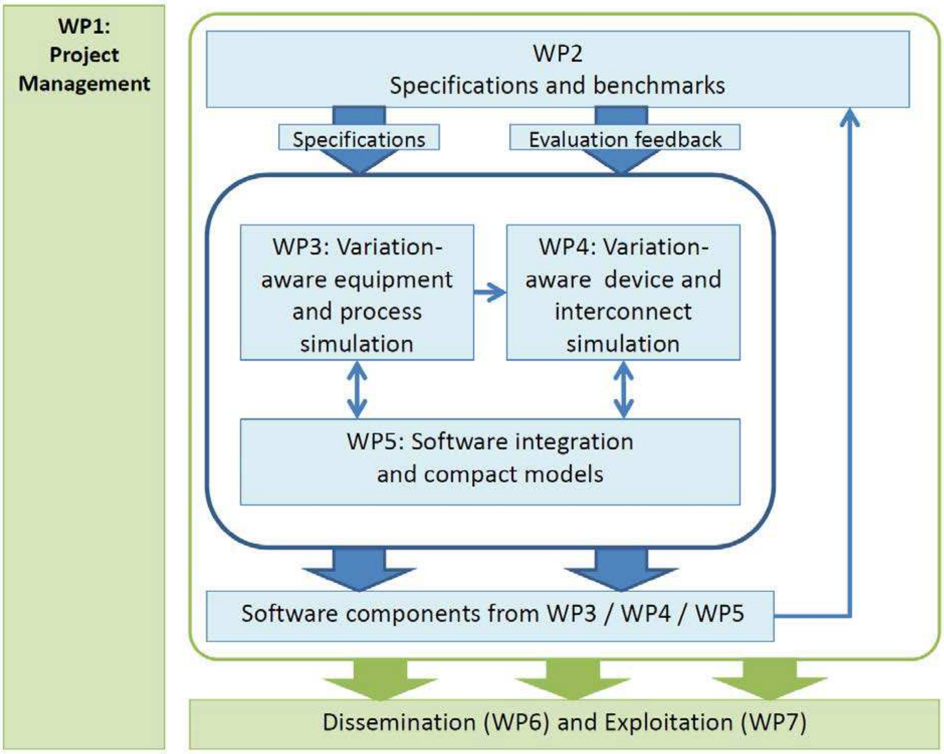
Variability-aware equipment optimization

Variability- aware design and optimization of MM devices, interconnects and circuits

EXPLOITATION IN EQUIPMENT AND SEMICONDUCTOR INDUSTRY

(From SUPERAID7 proposal and DoA)

SUPERAID7 Project Structure



WP1: Project Management

WP2
Specifications and benchmarks

Specifications

Evaluation feedback

WP3: Variation-aware equipment and process simulation

WP4: Variation-aware device and interconnect simulation

WP5: Software integration and compact models

Software components from WP3 / WP4 / WP5

Dissemination (WP6) and Exploitation (WP7)

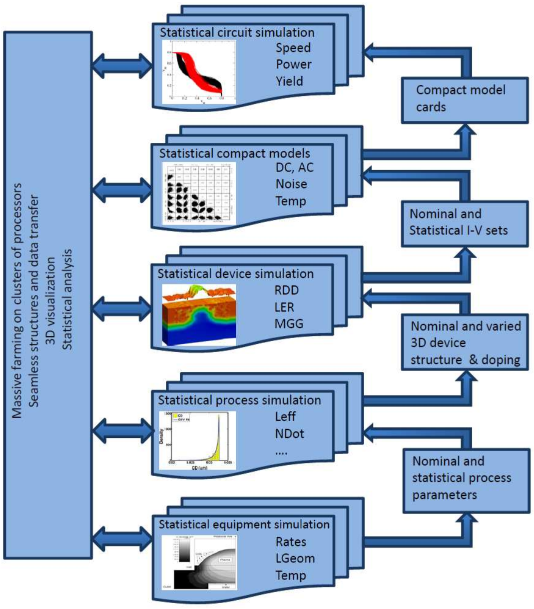
(From SUPERAID7 proposal and DoA)

Methodology Used

Simulation levels and tools used

Extension and closer integration of system from preceding SUPERTHEME project

- Equipment simulation: Q-VT (Quantemol), CFD-ACE (ESI Group)
- Process simulation:
  - Lithography: Dr.LiTHO (Fraunhofer)
  - Etching/deposition: ANETCH / DEP3D (Fraunhofer); Vienna TS
  - Implantation/annealing: Sentaurus Process (SNPS)
- Device simulation: GARAND (GSS)
- New interconnect simulator by GU/GSS/TU Wien
- Statistical compact model extraction: MYSTIC (GSS)
- (Circuit simulation: RandomSpice (GSS))



Massive farming on clusters of processors
Seamless structures and data transfer
3D visualization
Statistical analysis

Statistical circuit simulation
Speed
Power
Yield

Compact model cards

Statistical compact models
DC, AC
Noise
Temp

Nominal and Statistical I-V sets

Statistical device simulation
RDD
LER
MGG

Nominal and varied 3D device structure & doping

Statistical process simulation
Leff
NDot
....

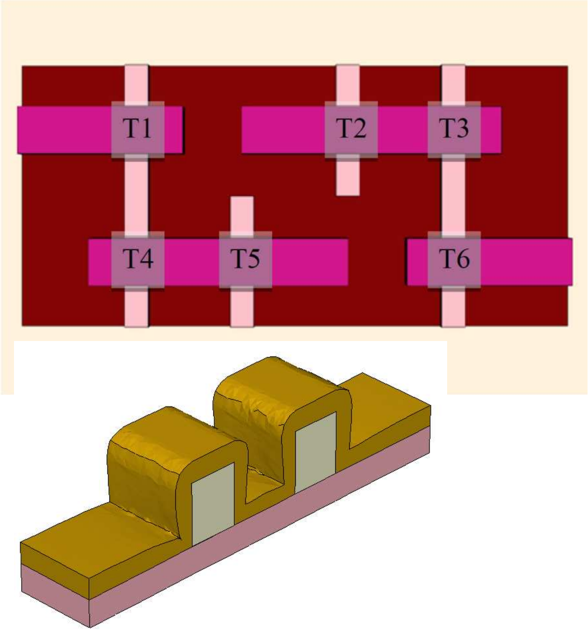
Nominal and statistical process parameters

Statistical equipment simulation
Rates
LGeom
Temp

Topography Simulation for Advanced 3D Devices
Motivation

- Motivation: Small features/pitches need Double Patterning or EUV Lithography
- Double Patterning introduces additional sources of variability:
  - Pattern effects
  - Difference between first and second incremental lithographay step
- Especially 3D devices affected by details of lithography/deposition/etching steps
  - E.g. resist shape, not only footprint

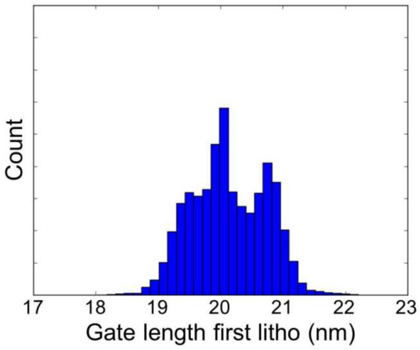
⇒ Advanced integrated topography simulation necessary

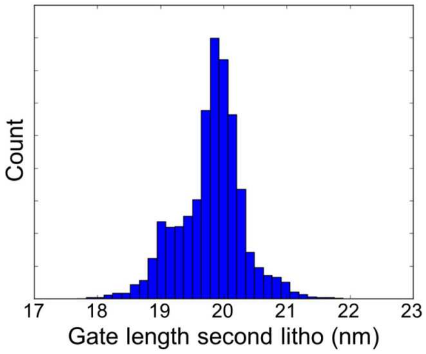


SRAM layout and SADP simulation – see presentation O14.1

Topography Simulation for Advanced 3D Devices
Motivation (II)

- SADP – depending on details of patterns, lithography, deposition and etching steps:
  - Differences between inner and outer lines
  - Some process variations may affect final feature sizes and/or pitches
  - Effect of some other process variations may be stonghly decreased
- Litho-Freeze-Litho-Etch and Litho-Etch-Litho-Etch Double Patterning: Generally difference between features generated in firts and second incremental litho step
- See presentation O14.1





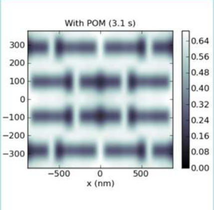
Topography Simulation for Advanced 3D Devices

Background tool from IISB: Dr. LiTHO

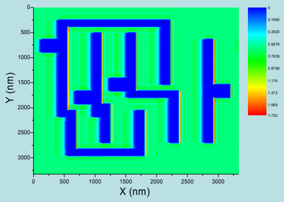
Dr. LiTHO

- Accurate and efficient imaging algorithms: Dr.Image
- Electromagnetic field solvers: Waveguide (RCWA), TASPAL (FDTD)
- Advanced optimization algorithms: Ginga, PSO, …
- Usage
  - Available under Linux and Windows
  - Highly flexible and easy to combine with other software
  - Python

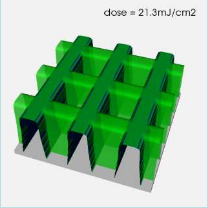
Aerial image of the poly layer of an SRAM cell



Rigorous simulation of an EUV-mask



Flexible simulation of different options for double-patterning-lithography

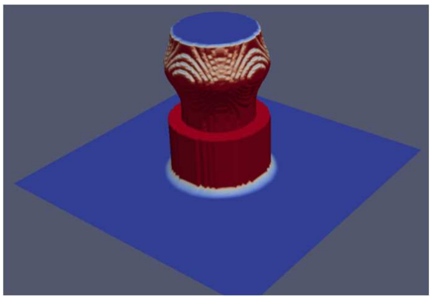


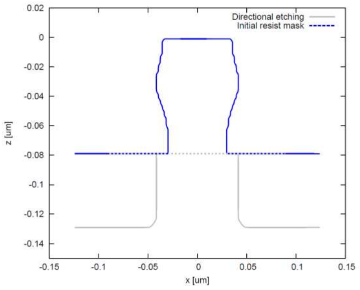
Topography Simulation for Advanced 3D Devices

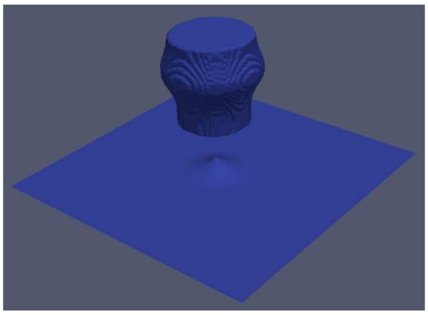
Integration Lithography/Deposition/Etching Simulation

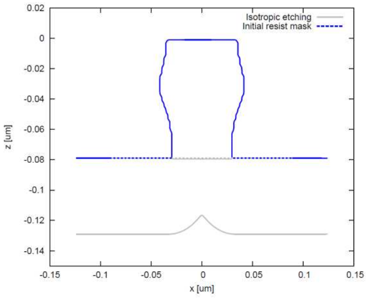
- Close integration between Dr.LiTHO, ANETCH/DEP3D (IISB), and Vienna TS
- Impact of realistic mask shape simulated with Dr.LiTHO for
  - directional etching
  - anisotropic etching

  simulated with Vienna TS





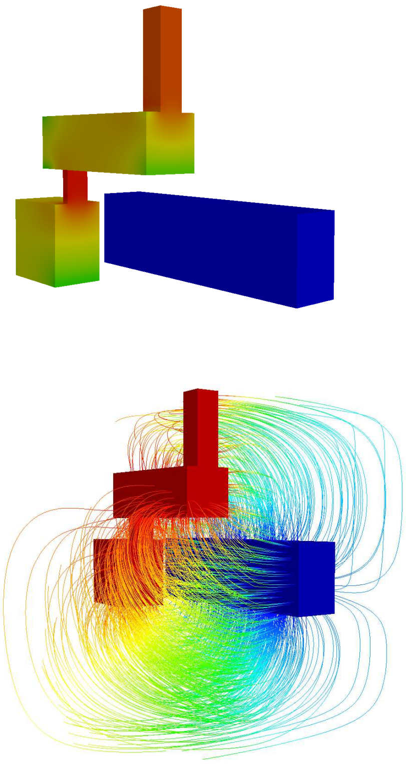




Interconnect Variability Simulation
Outline

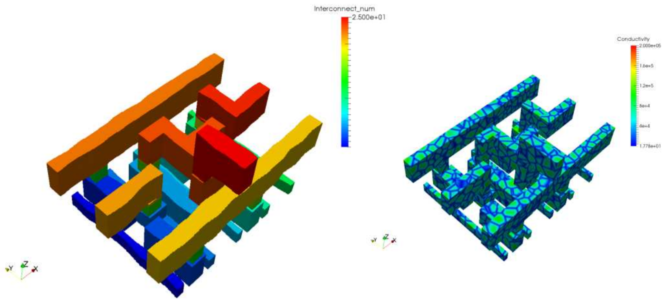
- Joint work by GSS, GU and TU Vienna, including:
  - Development of a 3-D Laplace-like solver for the evaluation of capacitive and resistive elements in advanced interconnect wiring
  - Use of process variability data
  - Extraction of compact RC circuit models in format compatible for circuit simulation

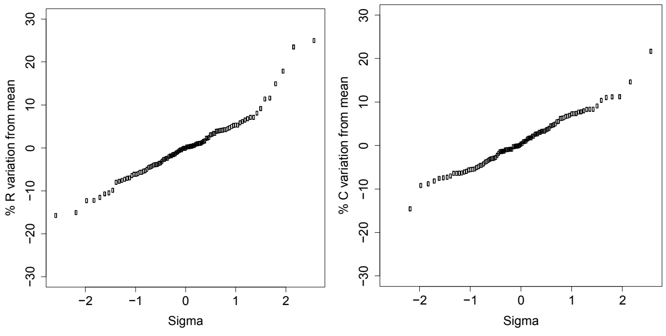
⇒ New tool CONNECTCAD



Interconnect Variability Simulation
Example for First Results

- Introducing statistical variability for Nominal Process Corner
- Top line left /right: LER and MGG
- Example: Distribution of a SINGLE-LINE (R_max) and INTER_LINE (C_max) in the system, due to LER





Some further glimpse on first results

6 related presentations at SISPAD 2016 conference

- O1.3: T. Sadi et al., “One-dimensional Multi-Subband Monte Carlo Simulation of Charge Transport in Si Nnaowire Transistors“
- O10.1: L. Wang et al., ”TCAD Proven Compact Modelling Re-centering Technology for Early 0.x PDKs
- O13.2: L. Bourdet et al., ”High and low-field contact Resistances in Trigate Devices in a Non-Equilibrium Green’s Functions”
- O20.1: Z. Zeng et al., ”Carrier scattering by workfunction fluctuations and interface dipoles in high-/metal gate stacks”
- P4: T. Al-Ameri et al., ”Impact of strain on the performance of Si nanowires transistors at the scaling limit: A 3D Monte Carlo / 2D Poisson Schrodinger simulation study”
- P15: Z. Zeng et al., ”Size-dependent carrier mobilities in rectangular silicon nanowire devices

Conclusions

SUPERAID 7

- Within SUPERAID7 a program system for the simulaiton of the impact of variations from equipment to circuit level is being developed
- The project especially aims at extended CMOS down to 7 nm and below
- Besides required physical device models core activities deal with integrated topography simulaiton and with interconnect simulation.

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