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Size-dependent carrier mobilities in rectangular silicon nanowire devices

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***Abstract*—Multi-gate transistors have attracted considerable attention as a way to overcome the scaling issues of planar MOSFETs. Although the effects of structural confinement on the carrier mobilities have been discussed extensively, the transition from silicon thin films to silicon nanowires (SiNWs) has been little investigated. In this contribution, we perform quantum calculations of the size-dependent carrier mobilities in gate-all-around rectangular SiNWs with leading dimension up to 50 nm, in the non-equilibrium Green's functions (NEGF) framework. We find that when the smallest width or height falls in the sub-10 nm range, nearest neighbor corner channels tend to merge and form "side channels" with much lower mobilities. On top of the numerical results, we have derived a simple model, which bridges square NW devices with thin film devices, and describes the size dependence of the carrier mobilities in rectangular SiNWs in a wide range of dimensions.**

I. INTRODUCTION

In a continuous effort to increase drive current and to control short-channel effects, Metal-Oxide-Semiconductor (MOS) transistors have evolved from classical, planar, single-gate devices to three-dimensional devices with a multi-gate structure [Double-Gate (DG), Tri-gate or Gate-All-Around (GAA) devices] [1]. Among multi-gate architectures, GAA silicon nanowire (SiNW) transistors demonstrate the best gate control and hence the best short-channel figures (sub-threshold slopes, drain-induced barrier lowering, ...). Consequently, considerable attention has been devoted to the study of GAA devices [2]–[7]. Although significant insights have been brought by these studies, the transition from silicon thin films to SiNWs has been little investigated up to now. In this work, we discuss how the carrier mobilities vary when going from SiNWs to silicon thin films.

In order to achieve a consistent description of this transition, we have performed quantum calculations in the Non-Equilibrium Green's Functions (NEGF) framework on rectangular SiNWs with leading dimension up to 50 nm. Based on the numerical results, we have developed a simple model, which bridges the DG devices with the square GAA (SQGAA) NW devices, and which describes the size dependence of the carrier mobilities in rectangular SiNWs over a wide range of dimensions.

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II. METHODOLOGY AND DEVICES

The simulated devices are rectangular GAA SiNW channels with width W and height H. Both the $\langle 100 \rangle$ [with $\{001\}$ facets] and $\langle 110 \rangle$ [with horizontal (001) and vertical $(1\bar{1}0)$ facets] nanowire orientations are considered. The gate-stack is made of 0.6 nm of SiO_2 and 2.4 nm of HfO_2. The transport properties of the SiNWs are computed in a NEGF framework based on the effective mass approximation for the electrons and on a three bands $\mathbf{k} \cdot \mathbf{p}$ model for the holes. The NEGF equations are solved self-consistently in a fully coupled mode space approach [8]. In our calculations, we have taken into account the carrier-phonon and surface roughness (SR) scatterings. The local approximation has been adopted for the carrier-phonon self-energy. The SR profiles are generated from a standard Gaussian autocorrelation function model with rms fluctuations $\Delta = 0.45$ nm and correlation length $L_c = 1.0$ nm. A detailed review of the methodology and the parameters for the carrier-phonon interactions can be found in Refs. [9] and [10]. The carrier mobilities are computed from a quasi-Fermi level analysis [11] on a 30 nm-long channel.

III. RESULTS AND DISCUSSION

We first discuss the electron and hole mobilities in rectangular SiNWs as a function of the width W and height H. The NEGF mobilities are computed in rectangular SiNWs with one side (H or W) equal to 7 nm and the other one ranging from 7 to 50 nm for electrons and from 7 to 35 nm for holes. The results are plotted in Fig. 1 (symbols). Note that H and W play equivalent roles in $[100]$ SiNWs (which have equivalent (010) and (001) facets, but not in $[110]$ SiNWs (which have non-equivalent (001) and $(1\bar{1}0)$ facets).

For electrons, we find that (*i*) $\langle 100 \rangle$ SiNWs perform better than $\langle 110 \rangle$ SiNWs, and (*ii*) $\langle 110 \rangle$ SiNWs with width $W > H$ show larger mobilities than $\langle 110 \rangle$ SiNWs with height $H > W$. These trends can be well understood from band structure arguments [12].

In $[100]$ SiNWs, the Δ valleys split into light ($m^* = 0.19\ m_0$) $\Delta_{y,z}$ valleys at the Γ point, and much heavier ($m^* = 0.92\ m_0$) Δ_x valleys at $k \neq 0$. Under strong inversion bias, the electron gas is confined at the surface of the SiNW by the electric field, mostly in the light Δ_y valleys on the lateral (010) facets, and mostly in the light Δ_z valleys on the top and bottom (001) facets. In $[110]$ SiNWs, the Δ valleys

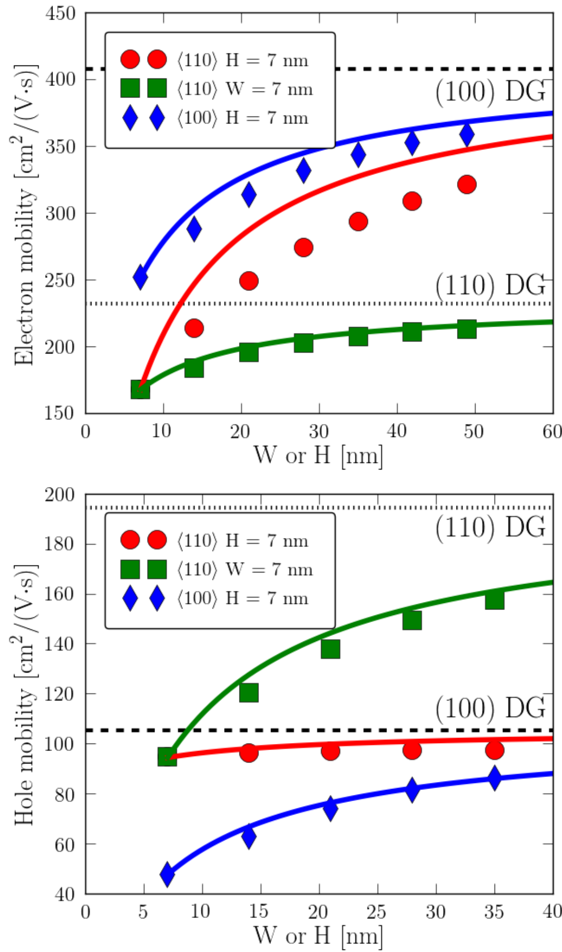

Fig. 1. Electron (upper panel) and hole (lower panel) mobilities in rectangular ⟨100⟩ and ⟨110⟩ GAA SiNWs as a function of width (W) or height (H) at carrier density $n = 8 \times 10^{12}$ cm^{-2}. The symbols are the NEGF results. The dashed and dotted horizontal lines are the NEGF reference mobilities in (100) and (110) DG devices, respectively. The solid lines are the interpolations from SQGAA NW devices to the limiting DG devices using Eq. (2).

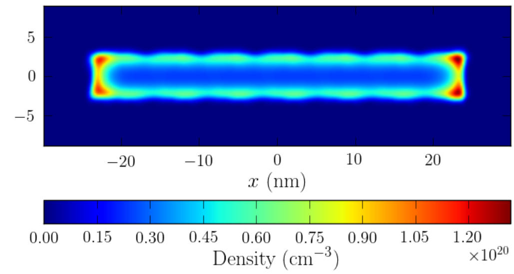

Fig. 2. Contour plot of the charge density distribution in a rectangular ⟨100⟩-oriented GAA SiNW device with (W, H) = (7 nm, 49 nm).

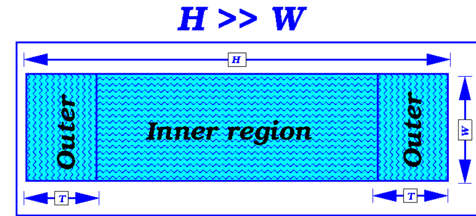

Fig. 3. Schematic representation of the partition of the charge distribution of Fig. 2 into two contributions, one from the side channels (outer region) with thickness T, and one from the inner region with thickness $H - 2T$.

split into light ($m^* = 0.19\ m_0$) Δ_z valleys at Γ point and heavier ($m^* = 0.55\ m_0$) $\Delta_{x,y}$ valley off Γ. Again, under strong inversion bias the electron gas is mostly confined in the light Δ_z valleys on the top and bottom (001) facets, but in the heavier $\Delta_{x,y}$ valleys on the lateral $(1\bar{1}0)$ facets. Therefore, wide ⟨110⟩ SiNWs with dominant (001) facets ($W > H$) perform better than tall ⟨110⟩ SiNWs with dominant $(1\bar{1}0)$ facets ($H > W$). Likewise, ⟨001⟩ nanowires with only (001) facets show better mobilities than ⟨110⟩ SiNWs with mixed facets.

The trends are opposite for holes. ⟨110⟩ SiNWs with $H > W$ indeed perform better than ⟨110⟩ SiNWs with $W > H$, and ⟨110⟩ SiNWs always outperform ⟨100⟩ SiNWs. Again, these trends can be explained by band structure arguments. Indeed, holes confined on {110} facets tend to show lighter transport masses than holes confined on {001} facets [13]; in square ⟨110⟩ SiNWs the highest valence subband has a clear light hole character and is well separated from the others, while in square ⟨100⟩ SiNWs the topmost valence bands are almost degenerate and heavy, which decreases carrier velocity and enhances inter-subband scattering [12].

In general, the mobility increases with increasing SiNW cross section, and tends to the expected DG limit (W or $H \longrightarrow \infty$). However, the convergence can be rather slow, especially for electrons in ⟨110⟩ SiNWs with $W > H$. In order to understand the physics behind, we have analyzed the carrier density in the devices (Fig. 2). For simplicity – but without loss of generality – we focus on electrons. As shown in Fig. 2, the density in the moderate to strong inversion regime peaks in four "corner channels" that tend to merge in two "side channels" when H or W is in the sub-10 nm range. The electron (e) or hole (h) mobility can then be written:

$$\mu^{(e,h)} = \frac{n_{in}^{(e,h)}}{n_{in}^{(e,h)} + n_{\text{Side}}^{(e,h)}} \mu_{\text{DG}}^{(e,h)} + \frac{n_{\text{Side}}^{(e,h)}}{n_{in}^{(e,h)} + n_{\text{Side}}^{(e,h)}} \mu_{\text{Side}}^{(e,h)}, \quad (1)$$

where n_{in} and n_{Side} are the charge densities per unit length in the inner region and side channels (outer region) of Fig. 3, and μ_{DG} is the mobility in the limiting DG device. The mobility μ_{Side} in the side channels can be extracted from the data at a given size [e.g., $W = 7$ nm and $H = 14$ nm when

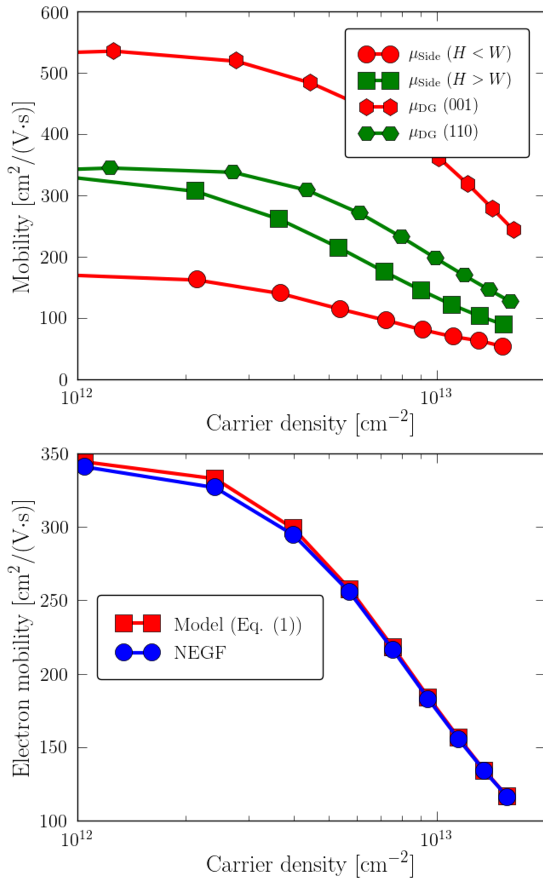

Fig. 4. Upper panel: Mobility computed in 7 nm-thick (100) and (110) DG devices, and mobility μ_{Side} in the side channels extracted from the data for the $\langle 110 \rangle$ SiNWs with $W = 7$ nm or $H = 7$ nm ($T = 3.5$ nm). Lower panel: Mobility in a $\langle 110 \rangle$ SiNW with (W, H) = (7 nm, 35 nm), as computed with NEGF and as obtained from Eq. (1) using the extracted mobility in the side channels.

$H > W$]. The extracted μ_{Side} is shown in Fig. 4 for $\langle 110 \rangle$ SiNWs. Eq. (1) turns out to give an excellent description of the mobility at all sizes and densities (see the lower panel of Fig. 4 for example). μ_{Side} depends on the carrier density and facet orientation. It is, as expected, lower on $(1\bar{1}0)$ than on (001) facets, and lower than in the corresponding DG device due to lateral quantum confinement in the side channel and enhanced surface roughness and phonon scattering.

The charge density n_{in} in the inner region increases linearly with W or H, while the charge density n_{Side} in the side channels is almost independent on the leading dimension (see Fig. 5). Actually, charge accumulation in both inner and outer regions is ruled by simple electrostatics, e.g. $n_{in} \simeq \alpha(W - 2T)$ and $n_{\text{Side}} \simeq \alpha(H + 2T)$ when $W > H$. Then Eq. (1) turns into a simple interpolation formula between the mobility μ_{SQ} of the square NW ($H = W$) and the mobility μ_{DG} of the

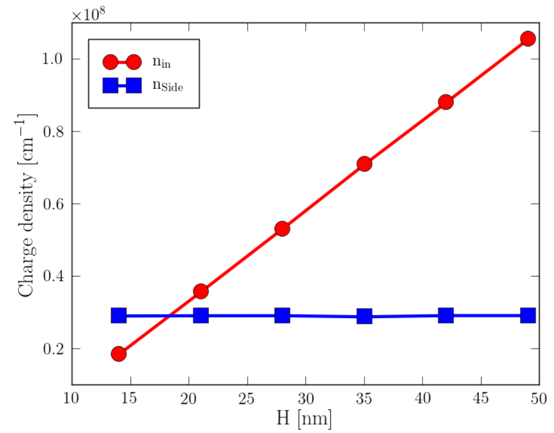

Fig. 5. Charge density in the inner region (n_{in}) and in the outer region (side channels, n_{Side}) as a function of the height H in $\langle 100 \rangle$ Si NWs. Here, $W = 7$ nm, $T = 3.5$ nm, and the total charge density is $n = 1.2 \times 10^{13}$ cm^{-2}.

limiting double gate device, namely:

$$\mu^{(e,h)} \approx \frac{W - H}{W + H}\mu_{DG}^{(e,h)} + \frac{2H}{W + H}\mu_{SQ}^{(e,h)} \quad (2)$$

when $W > H$, and:

$$\mu^{(e,h)} \approx \frac{H - W}{W + H}\mu_{DG}^{(e,h)} + \frac{2W}{W + H}\mu_{SQ}^{(e,h)} \quad (3)$$

when $W < H$. These equations reproduce the NEGF data very well in most cases, as shown in Fig. 1. Therefore, this model, which only requires the square GAA and DG mobilities as input, is able to describe the size dependence of the carrier mobilities in rectangular SiNWs over a wide range of dimensions and carrier densities.

CONCLUSIONS

In a real space NEGF framework, we have performed quantum calculations on the size-dependent carrier mobilities in gate-all-around rectangular silicon nanowire devices. We find that the carrier mobilities improve when increasing the leading dimension and converge to the expected double gate limit. However, when the smallest dimension falls in sub-10 nm range, the four corner channels merge into two side channels with low mobility. Their contribution remains significant even in rectangular devices with large width or height up to 50 nm, so that the mobility may be slow to converge to the double gate limit in some cases. On top of the numerical results, we have derived a simple model for the size-dependent carrier mobilities, which bridges the square gate-all-around nanowire devices with the thin film devices. This model may be used in the compact modeling of gate-all-around transistors.

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