

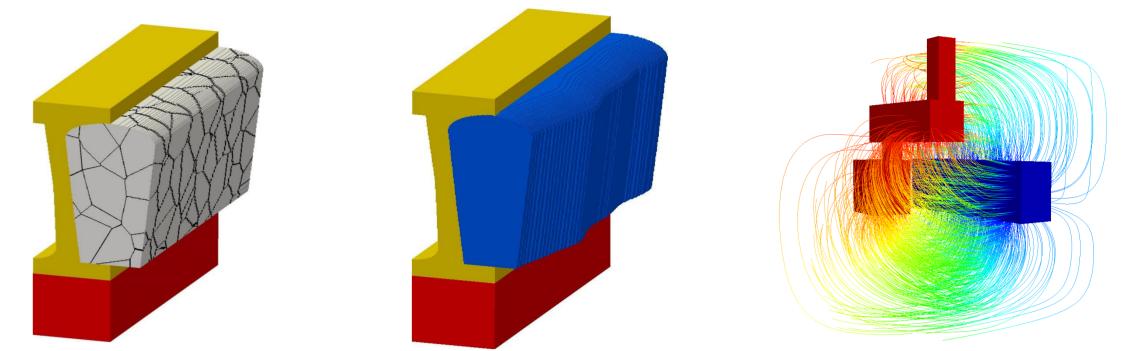
SUPERAID7

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Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

General description

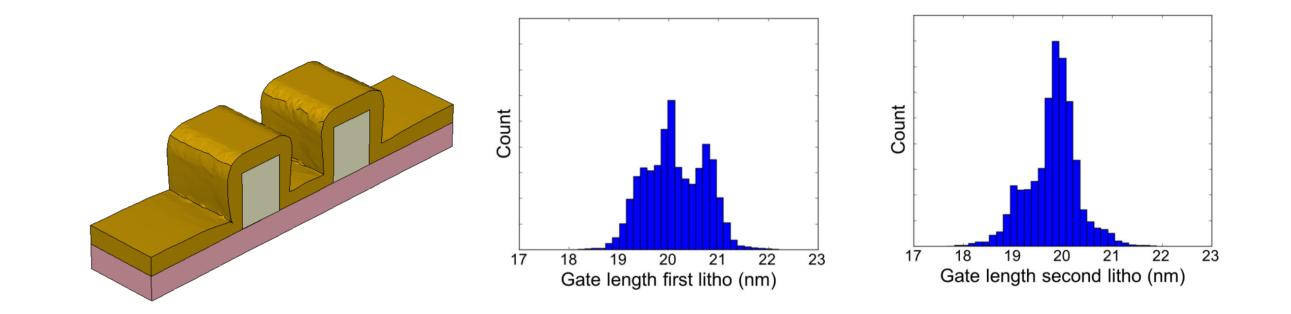
Modelling and simulation (TCAD) offer the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated. TCAD is a vital component for variability-aware Design-Technology Co-Optimization (DCTO), which is a key approach to optimize not only the performance but also the yield for aggressively scaled CMOS devices and circuits. SUPERAID7 will build upon the successful FP7 project SUPERTHEME which focused on advanced *More-than-Moore* devices, and will establish a software system for the simulation of the impact of systematic and statistical process variations on advanced *More Moore* devices and circuits down to the 7 nm node and below, including especially interconnects. This will need improved physical models and extended compact models. Device architectures addressed in the benchmarks include especially TriGate/ Ω Gate FETs and stacked nanowires, including alternative channel materials. The software developed will be benchmarked utilizing background and sideground experiments of the partner CEA. Main channels for exploitation will be software commercialization via the partner GSS and support of device architecture activities at CEA.



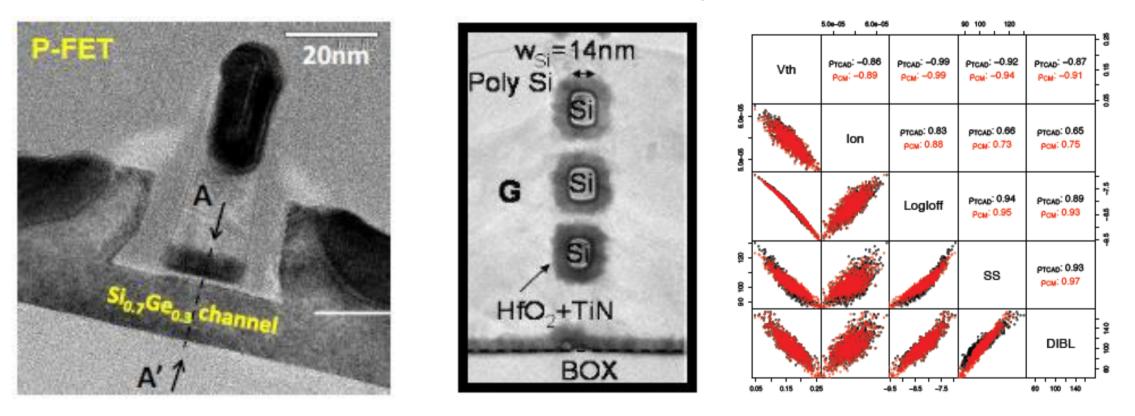
Goals / Objectives

- Development of a software system for the simulation of the impact of systematical and statistical process variations for advanced extended CMOS devices and interconnects
- Close interaction with leading European technology development projects (esp. KET Pilot Lines) via partner CEA/Leti and some members of the SUPERAID7 Industrial and Scientific Advisory Board

Left and middle: Examples for interconnect variability (copper granularity and line edge roughness; right: 3D interconnect electrical simulation (GSS)



Left: Self-aligned double patterning of fins (Fraunhofer IISB); litho-etchlitho-etch (LELE) patterning of gates: first (middle) and second(right) incremental lithography step (Fraunhofer IISB)



Trigate transistor (left) and stacked Gate-All-Around nanowires

- Continued attention on data reduction / hierarchical simulation from discretization of equipment to compact models – and on correlations
- Specific focus on advanced integrated topography simulation, carrier transport models for nanowire transistors and/or alternative channel materials, interconnect modeling and simulation

Societal impact / Results

The software suite being developed in SUPERAID7 will enable the assessment and minimization of the impact of process variations on advanced *extended CMOS* devices and circuits. This helps to optimize fabrication processes, device and circuit properties, and finally yield in semiconductor fabrication, and contributes to enabling further applications of micro and nanoelectronics.

Looking ahead

Future developments are planned in four main directions:

 Development of the variability-aware simulation ranging from equipment to circuit level (middle) (both CEA/Leti) as examples for target structure; right: Example for local variability in statistical compact model (GSS)

Partners

- Fraunhofer IISB, Erlangen
- Gold Standard Simulations Ltd (GSS), Glasgow
- CEA-Leti, Grenoble
- University of Glasgow
- Technische Universität Wien

Countries involved

- Germany
- Austria
- France
- United Kingdom

- Internal use of SUPERAID7 software at partners' sites for the development and optimization of equipment, processes, devices and circuits
- Demonstration of the software for DCTO applications
- Exploitation of the software developed via commercial offer of the SUPERAID7 partner Gold Standard Simulations

Additional information

More information is given at <u>www.superaid7.eu</u>

This includes among others

- Public deliverables, posters, information on software tools
- Currently 8 publications on SUPERAID7 results



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