Performance and Design Considerations for Gate-All-around Stacked-NanoWires FETs

S. Barraud, V. Lapras, B. Previtali, M.P. Samson, J. Lacord, S. Martinie, M.-A. Jaud, S. Athanasiou, F. Triozon, O. Rozeau, J.M. Hartmann, C. Vizioz, C. Comboroure, F. Andrieu, J.C. Barbé, M. Vinet, and T. Ernst

CEA-LETI, Minatec Campus, Grenoble, France

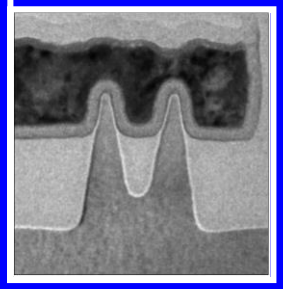
STMicroelectronics, Crolles, France

Context of this work

Two main MOSFET architectures for advanced CMOS

3D FinFET

22nm INTEL



16nm TSMC

14nm SAMSUNG
14nm INTEL

Scalability

?

28nm

22nm

22nm GF

16nm

14nm

10nm

7nm

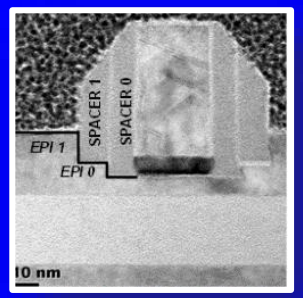
5nm

3nm

New MOSFET architectures need to be proposed

28nm ST

2D FDSOI

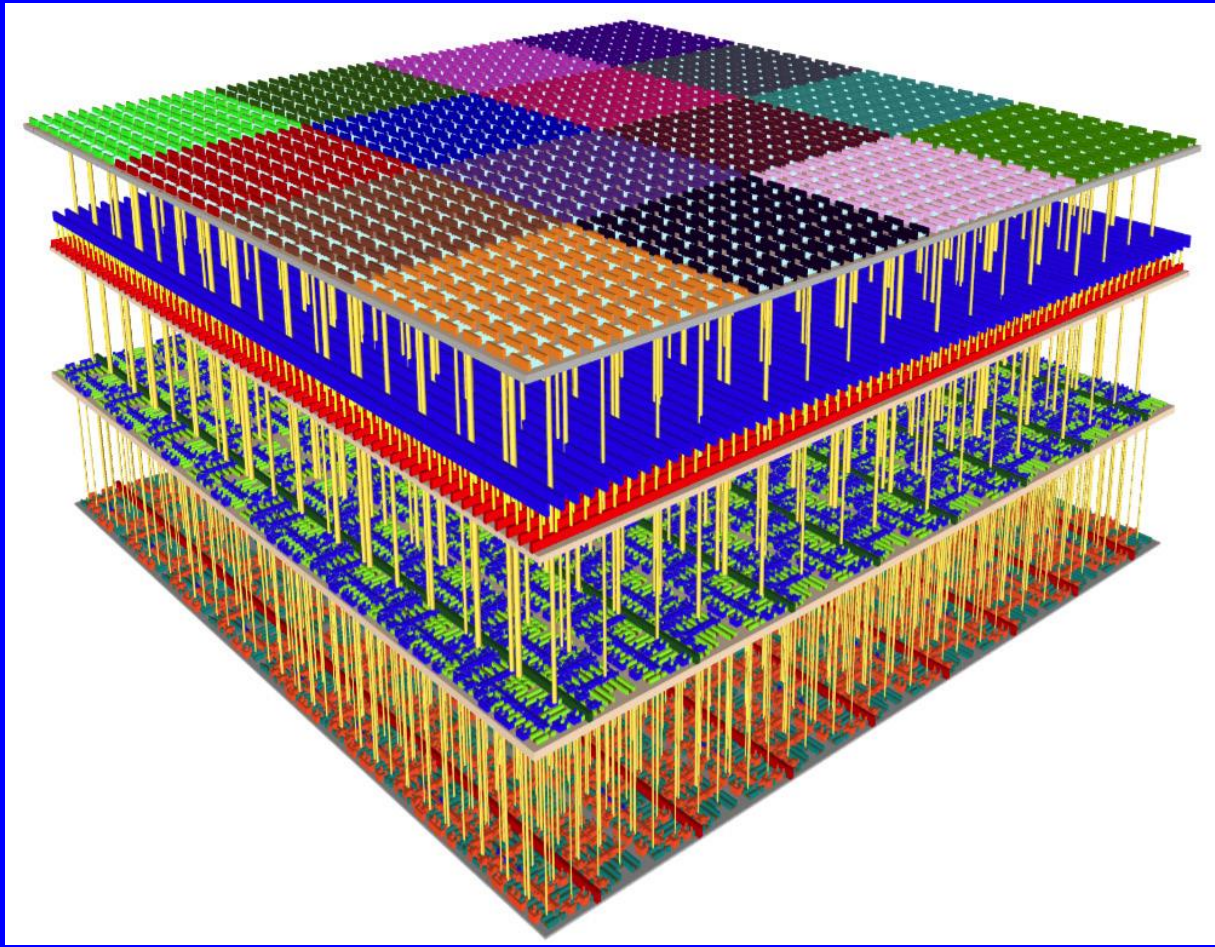


Back-gate control using thin BOX capacitive

Single-gate → reduction of SCE controlled by thinner T_{Si} or T_{BOX}

Context of this work

Plenty of space … at the top !



Max M. Shulaker et al., Nature 2017, Stanford

2017 press releases

May | 2017

Samsung set to lead the future of foundry with comprehensive process roadmap down to 4nm

4LPP (4nm Low Power Plus): 4LPP will be the first implementation of **next generation device** architecture – MBCFET™ structure (Multi Bridge Channel FET). MBCFET™ is Samsung's unique GAAFET (**Gate All Around FET**) technology that uses a **Nanosheet device** to overcome the physical scaling and performance limitations of the FinFET architecture.

https://news.samsung.com/global/samsung-set-to-lead-the-future-of-foundry-with-comprehensive-process-roadmap-down-to-4nm

June | 2017

IBM claims 5nm Nanosheet breakthough

IBM researchers and their partners have developed a new transistor architecture based **on Stacked Silicon Nanosheets** that they believe will make FinFETs obsolete at the 5nm node

http://www.eetimes.com/document.asp?doc_id=1331850&

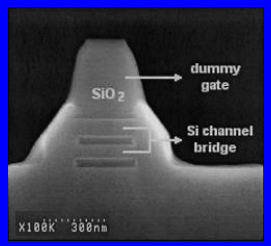
GAA MOSFET devices are becoming an industrial reality

3D stacked structures

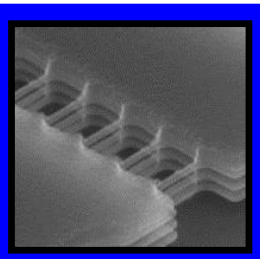
15 years of innovation

MultiBridge Channel MOSFET

S.Y. Lee et al SAMSUNG
IEEE Trans Nano 2003

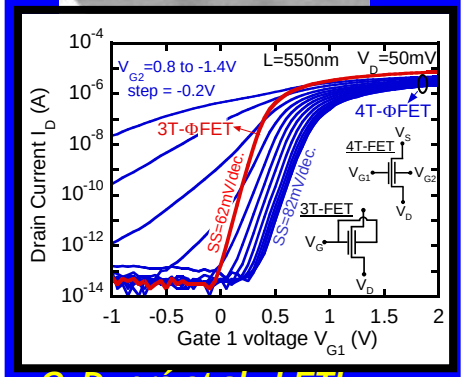


First Stacked NW CMOS



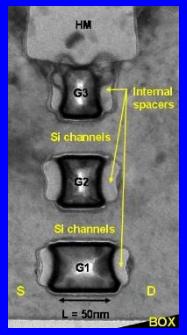
T. Ernst et al. , IEDM06

Nanowires with independent gates



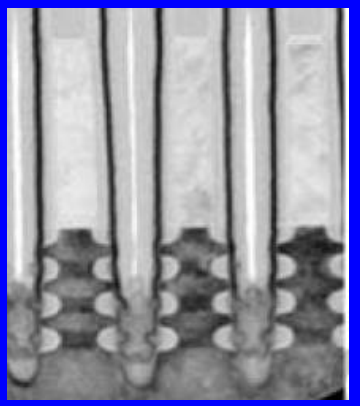
C. Dupré et al. LETI
IEDM 2008

Internal spacers introduction



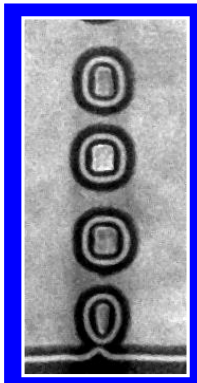
E. Bernard et al.
VLSI 08
LETI - STM

High density



IBM
N. Loubet & al. (VLSI 2017)

ONO crystalline 3D Flash

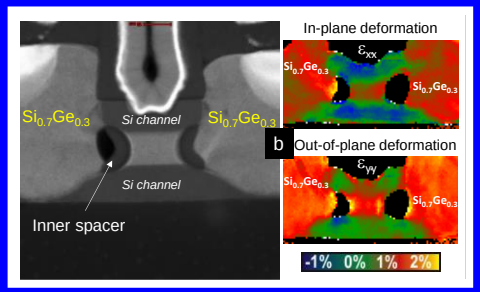


A. Hubert et al.
IEDM 2008 -LETI

13 crystalline levels !

T. Ernst et al.
Micro. Eng. 2011

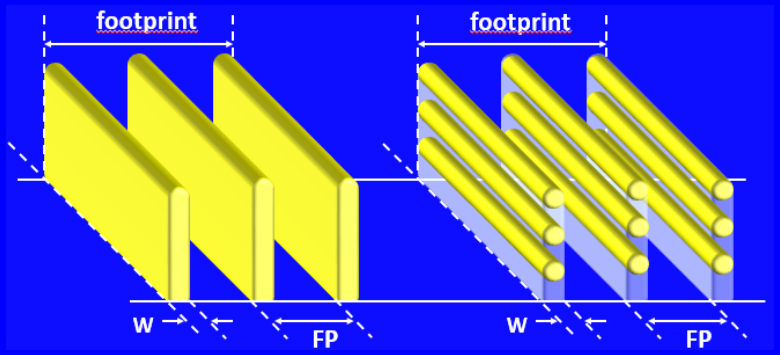
Strain booster

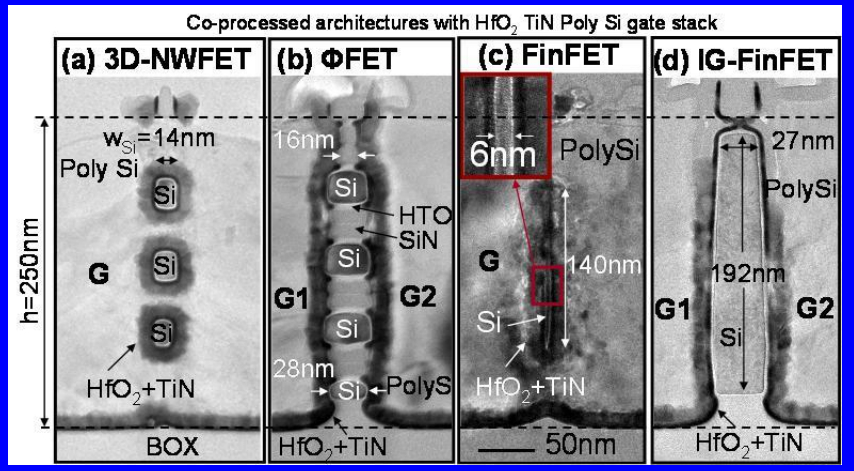


S. Barraud et al.
IEDM 2016

From FinFet to stacked NW

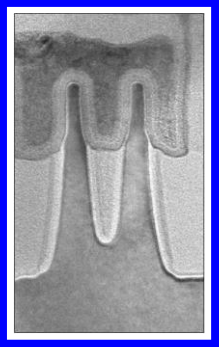
Fin FETs ➡ **GAA Wire FETs**



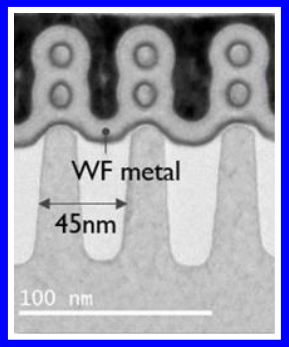


Same process (LETI 2008 – IEDM)

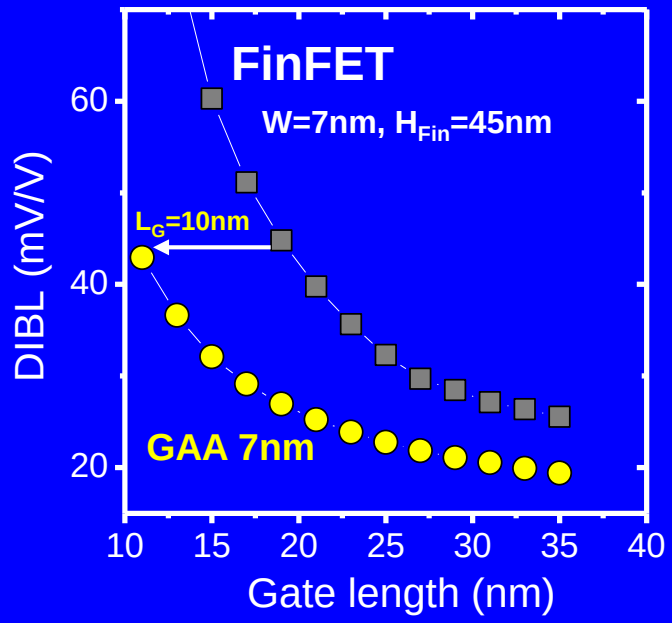
14nm INTEL [1]



IMEC [2]



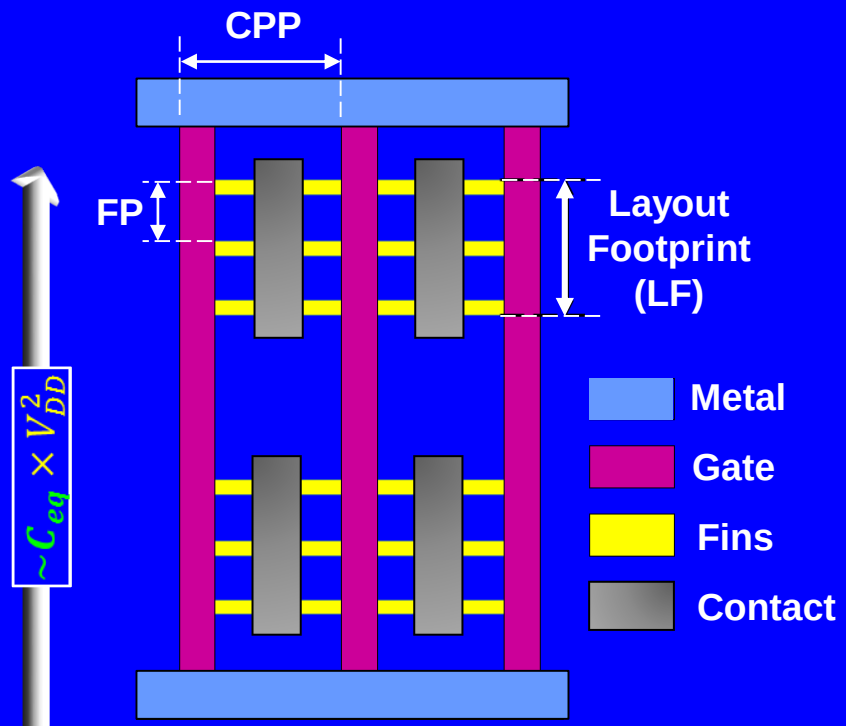
TCAD



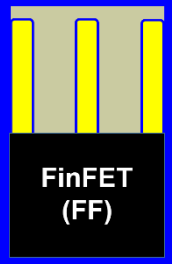
[1] S. Natarajan et *al.*, IEDM, 2014.

[2] H. Mertens et *al.*, VLSI Technology, 2016.

Motivation/Objective



Device architecture scaling



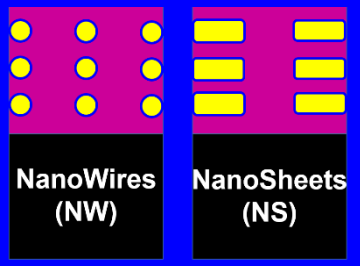
CPP scaling

↓

L_G reduction

↓

Electrostatic booster to keep low leakage current



Alternative options: GAA structures

- Increase I_{eff} per footprint
- Decrease C_{eq} per footprint

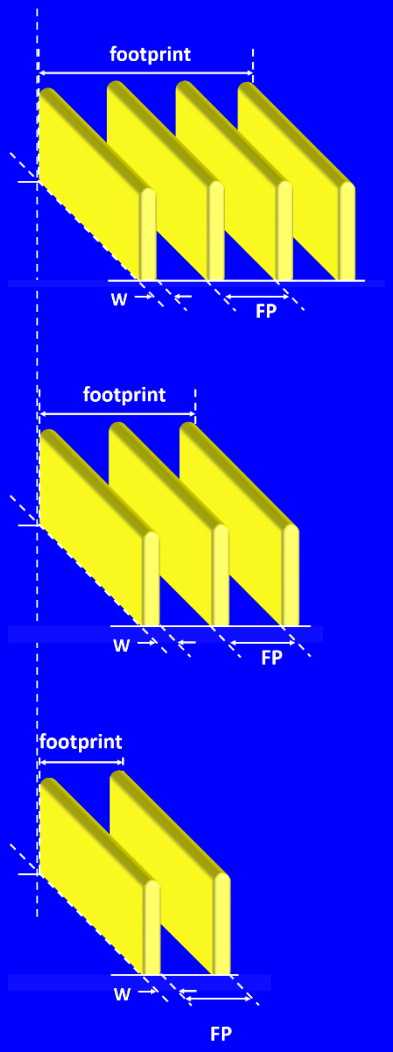
ELECTROSTATICS FF/NW/NS	MOBILITY FF/NW/NS	$C_{PARASITICS}$ FF/NW/NS	Device Fabrication FF/NW/NS

Outline

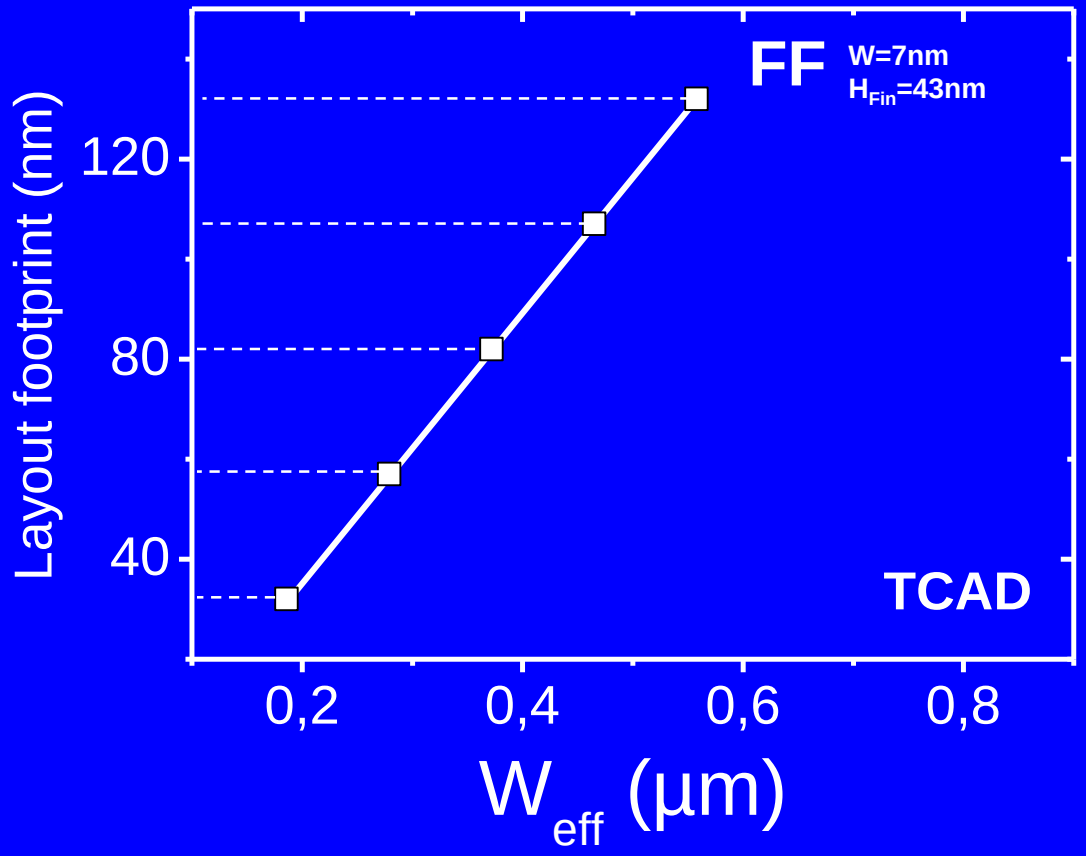
- Performance/Design consideration
- Device Fabrication
  - Inner spacer
  - SiGe S/D
- Strain Characterization
  - Precession Electron Diffraction
- Perspectives
- Summary and Conclusion

FinFET

Layout footprint (nm)



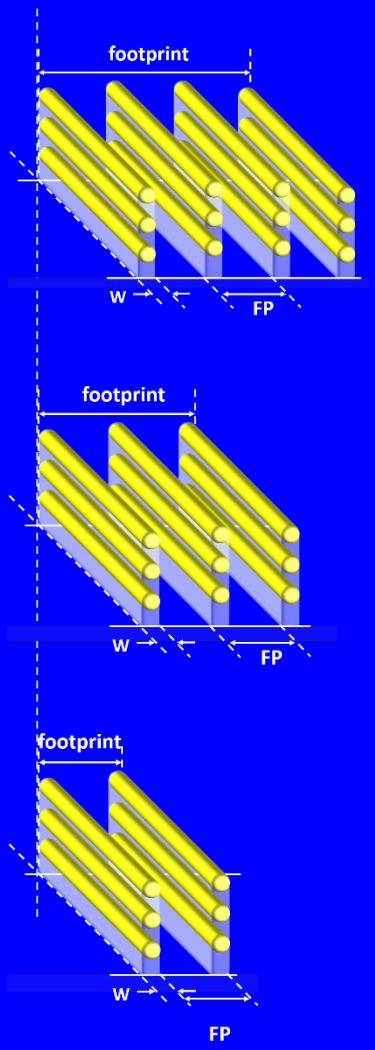
$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$



W_{eff}=circonference of Fin ($2H_{Fin}$+W)

FinFET to GAA Nanowires

Layout footprint (nm)



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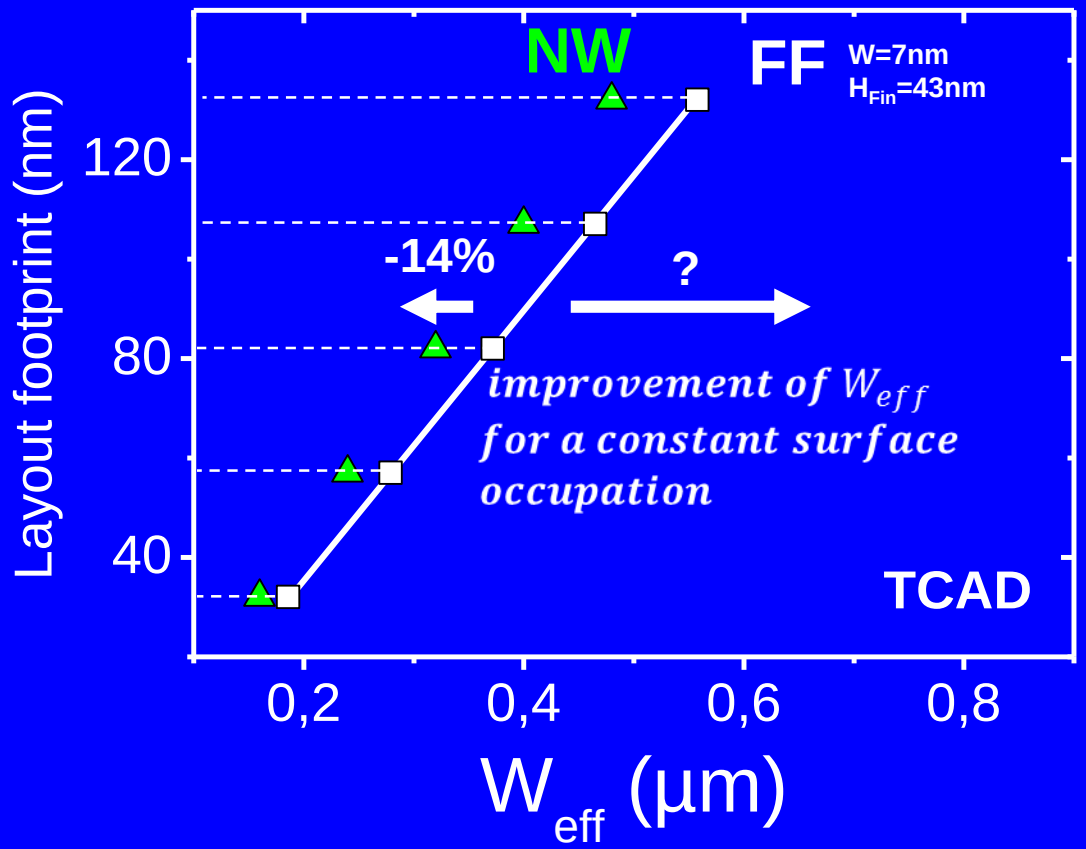
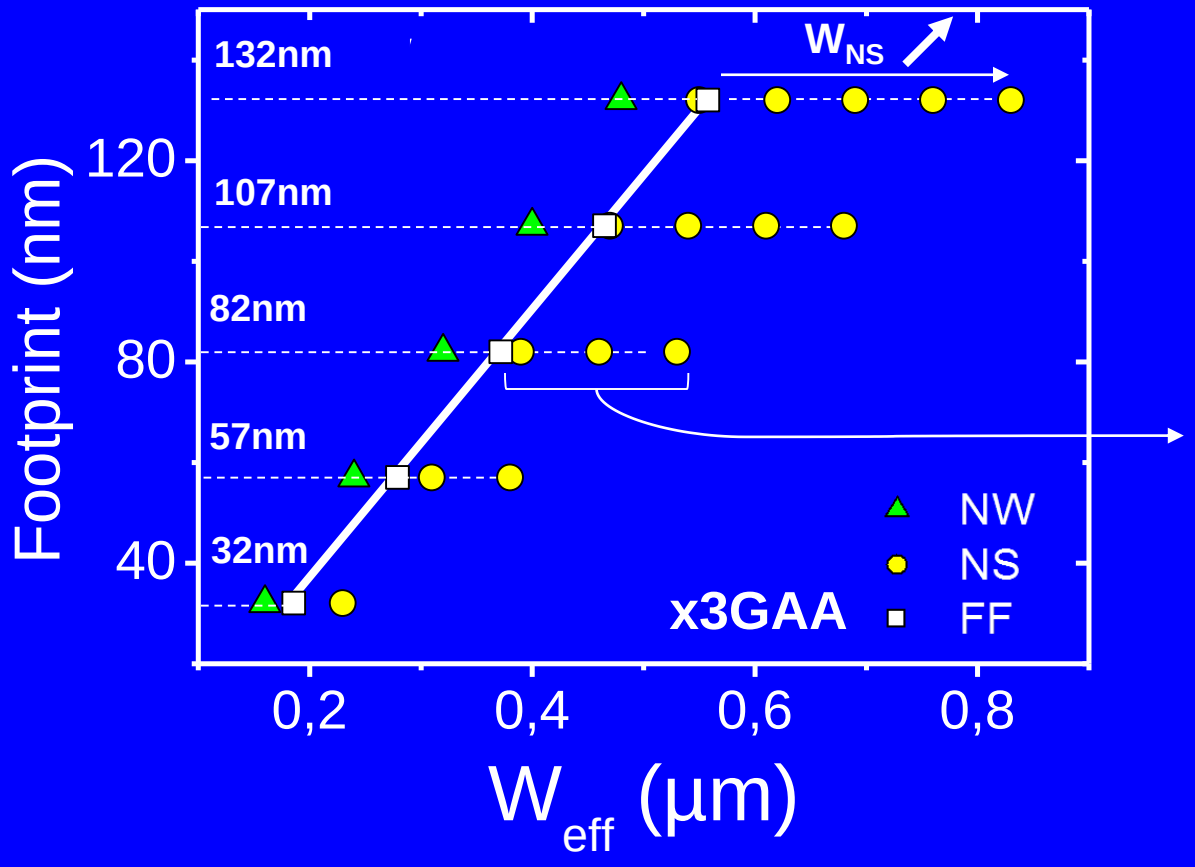


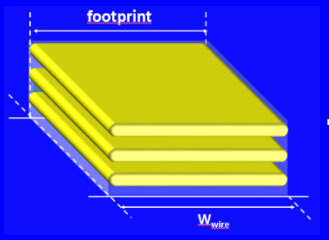
W_{eff}=circonference of Fin ($2H_{Fin}$+W)

GAA Nanowires to Nanosheets

$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

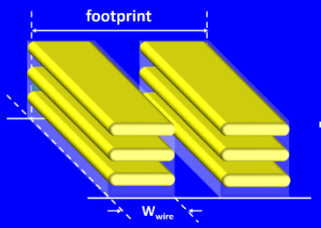


W=82nm



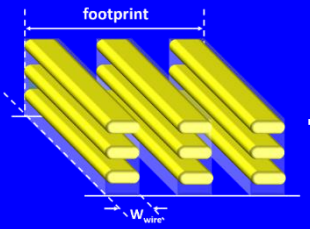
+5% W_{eff}

W=32nm



+24% W_{eff}

W=15nm

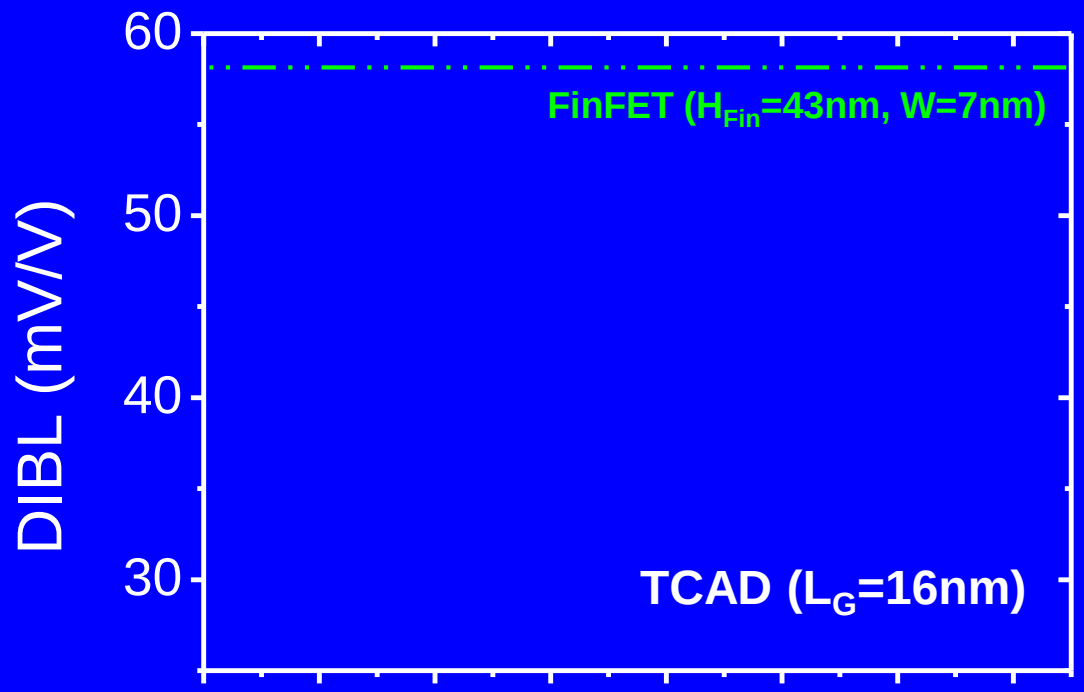


+42% W_{eff}

W_{eff}=circonference of Fin ($2H_{Fin}$+W)

Short-channel effects

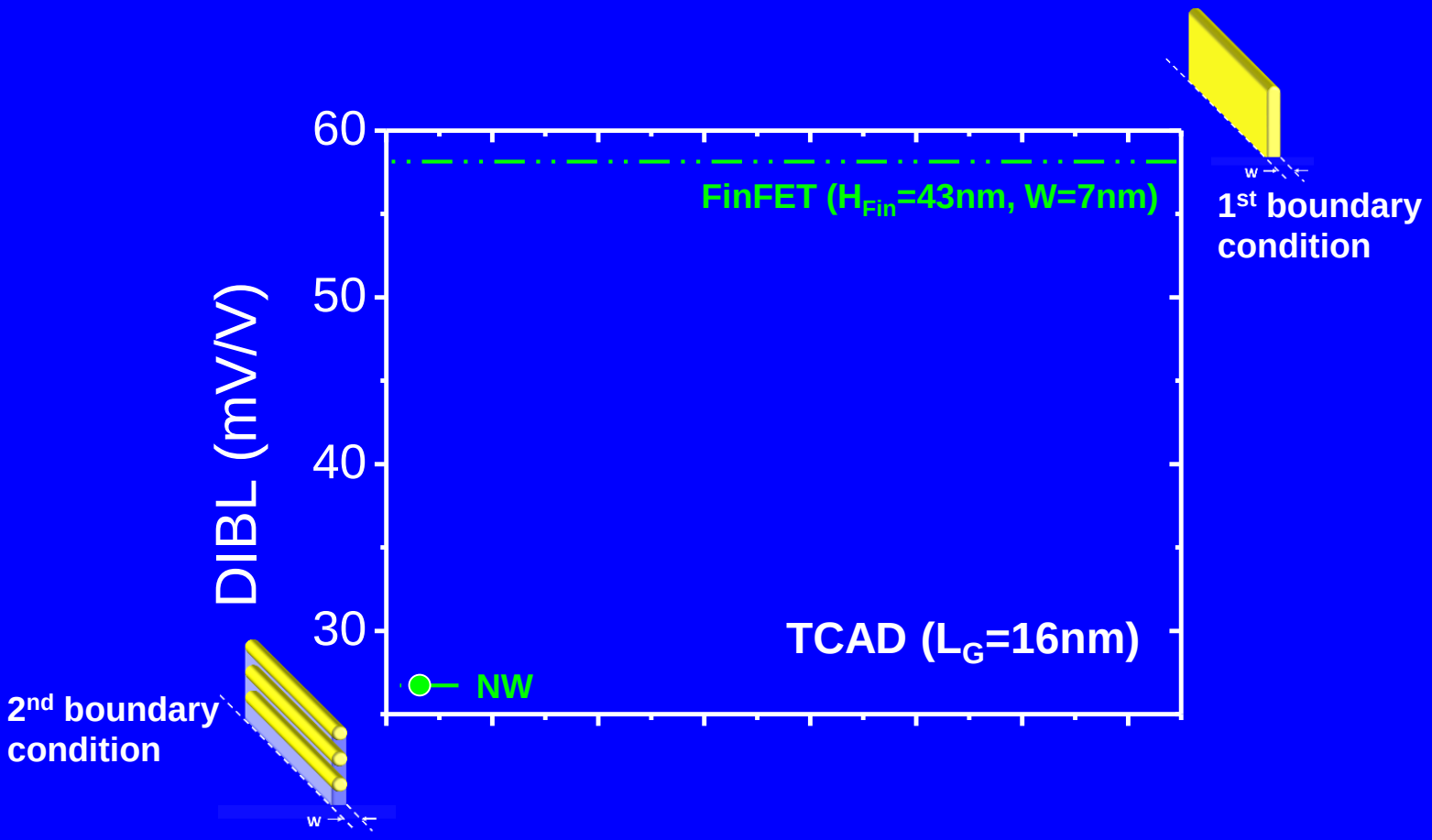
Electrostatics of multi-gates MOSFET transistors



1st boundary condition

Short-channel effects

Electrostatics of multi-gates MOSFET transistors

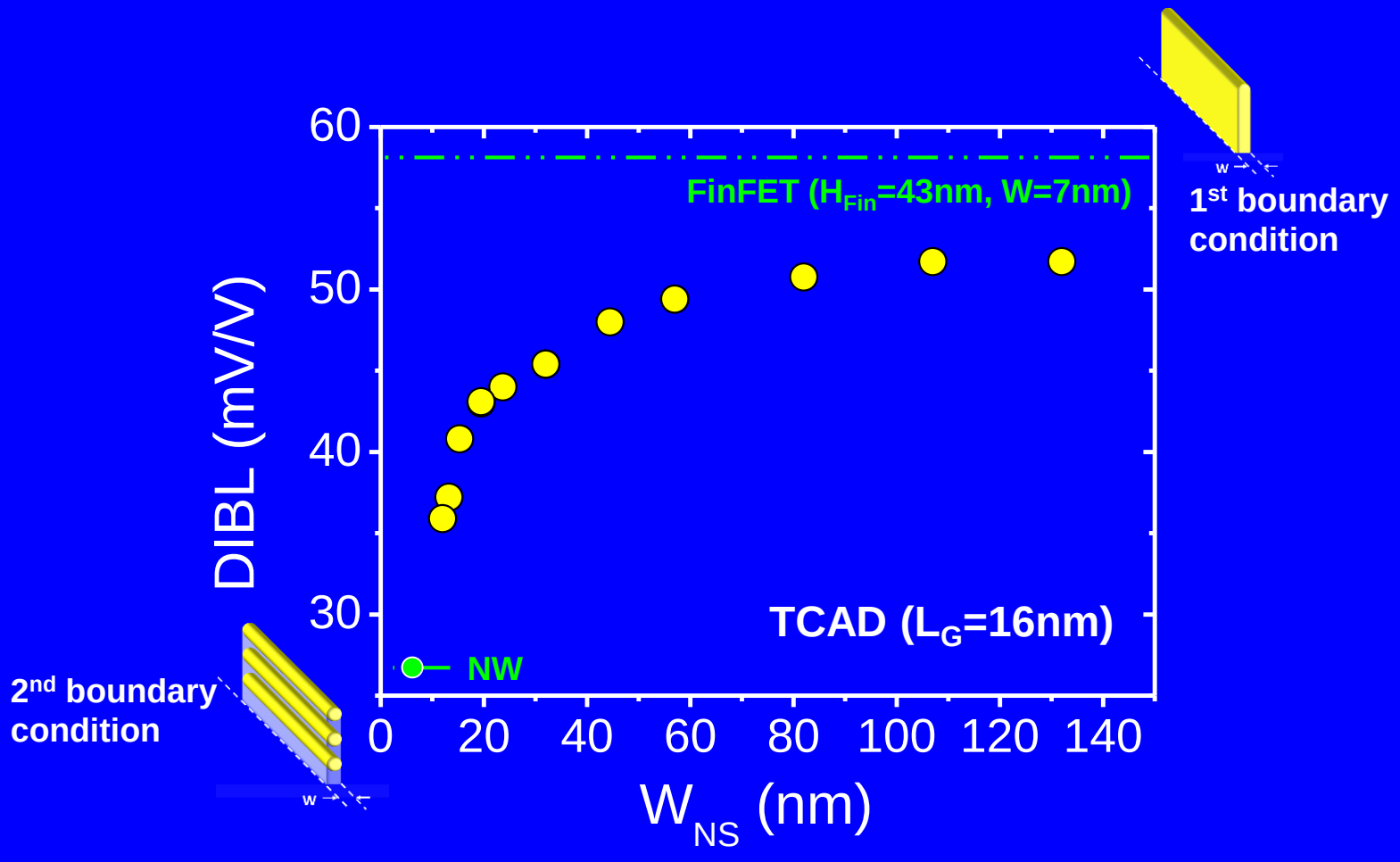


- Strong reduction of DIBL for Gate-all-around nanowire.

→ Optimal electrostatics control!

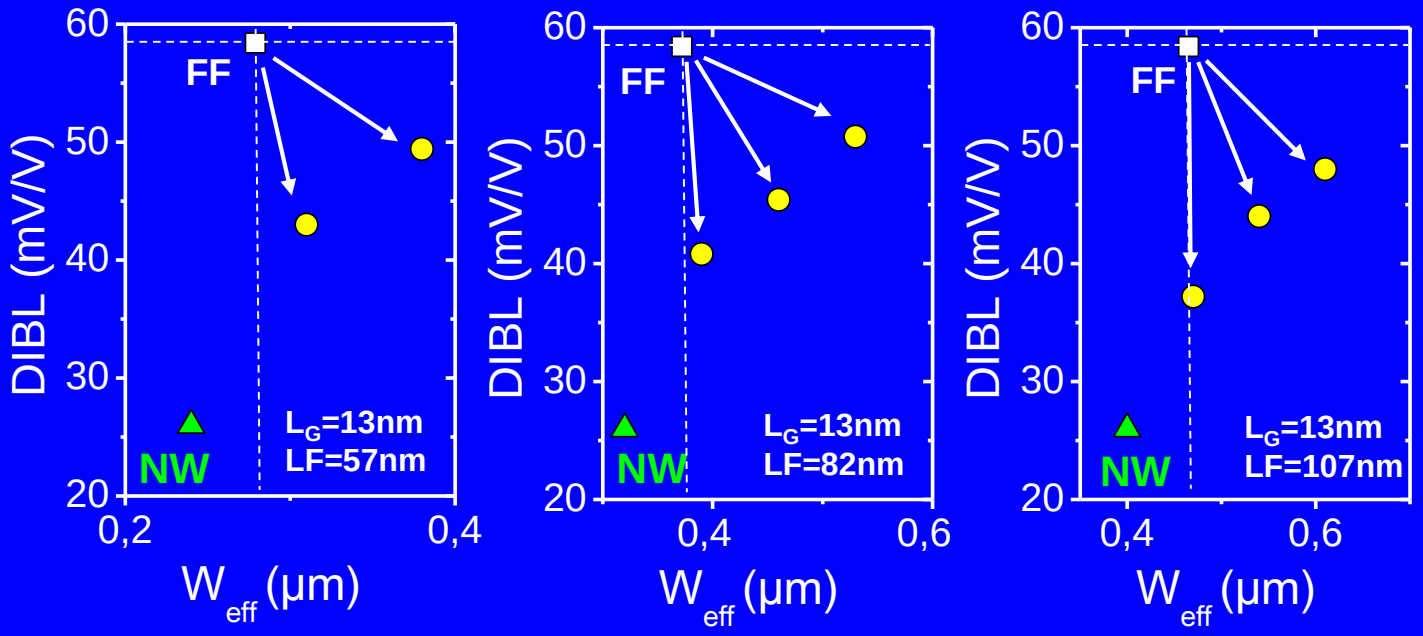
Short-channel effects

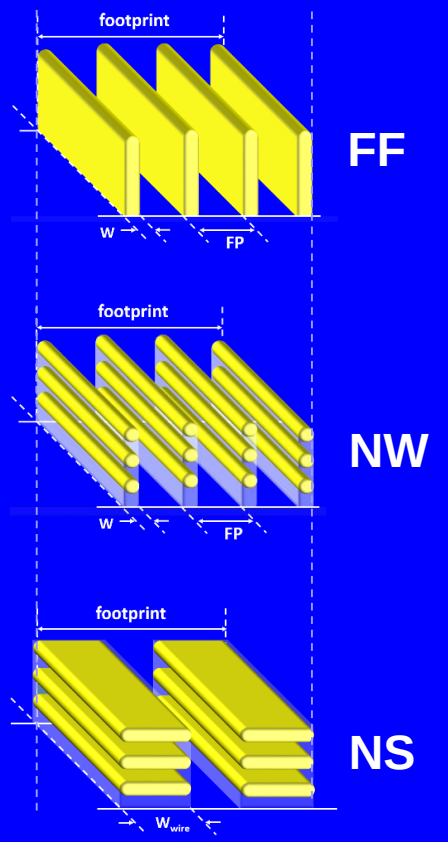
Electrostatics of multi-gates MOSFET transistors



• GAA Nanosheets (thin and wide wires) show intermediate DIBL between NW and FinFET. DIBL depends on wire width (W).

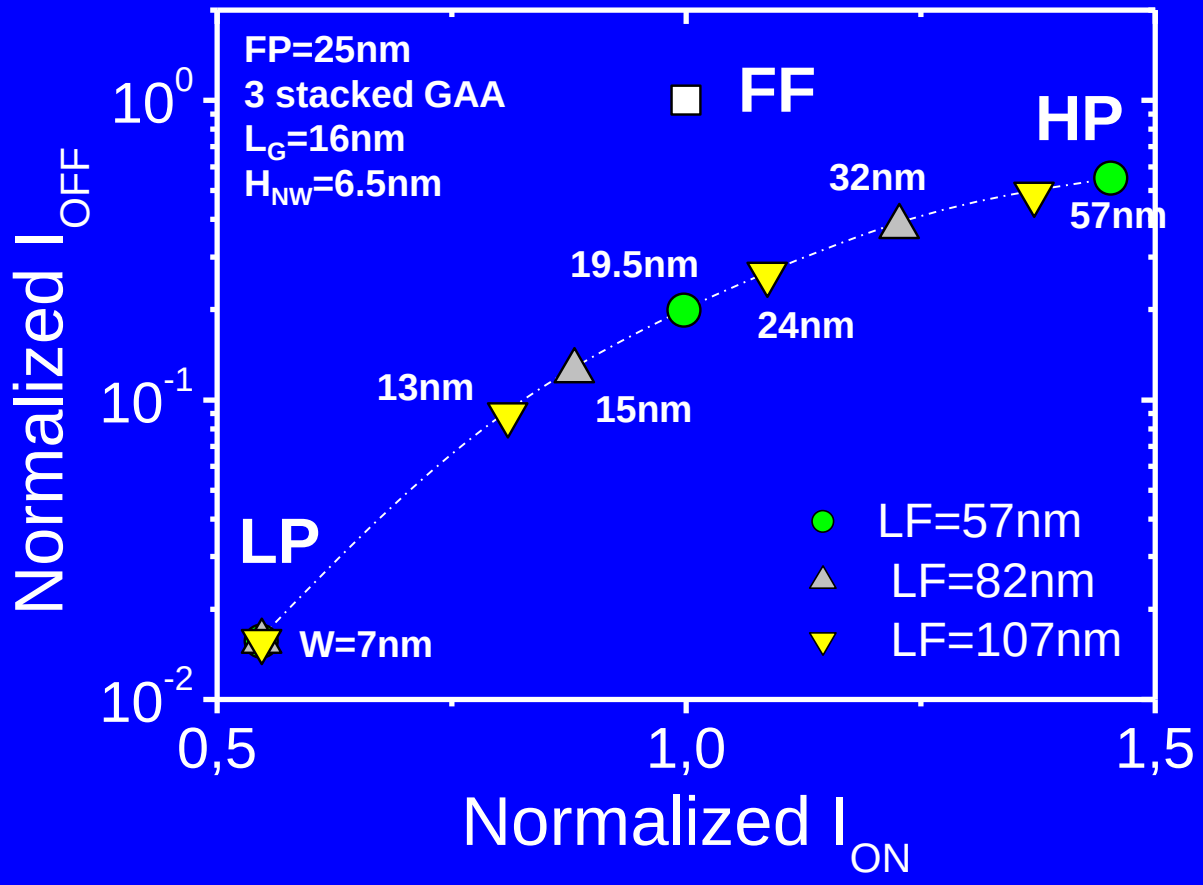
Tradeoff between SCE and W_{eff}





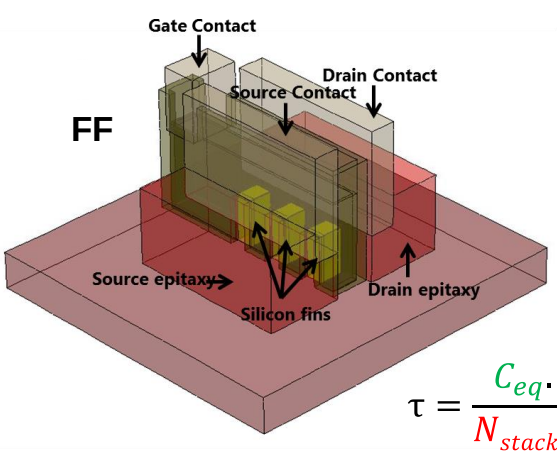
- GAA stacked-nanosheets maximize W_{eff} (drive current) per layout footprint with improved channel electrostatics.

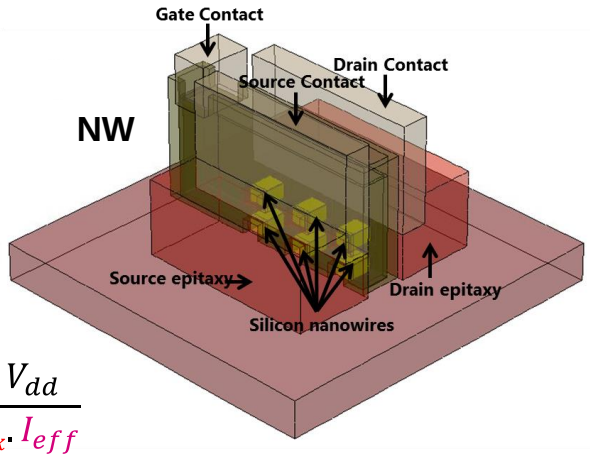
Power/Perf. Optimization



GAA Nanosheet transistors offers more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width.

Parasitic capacitances and delay

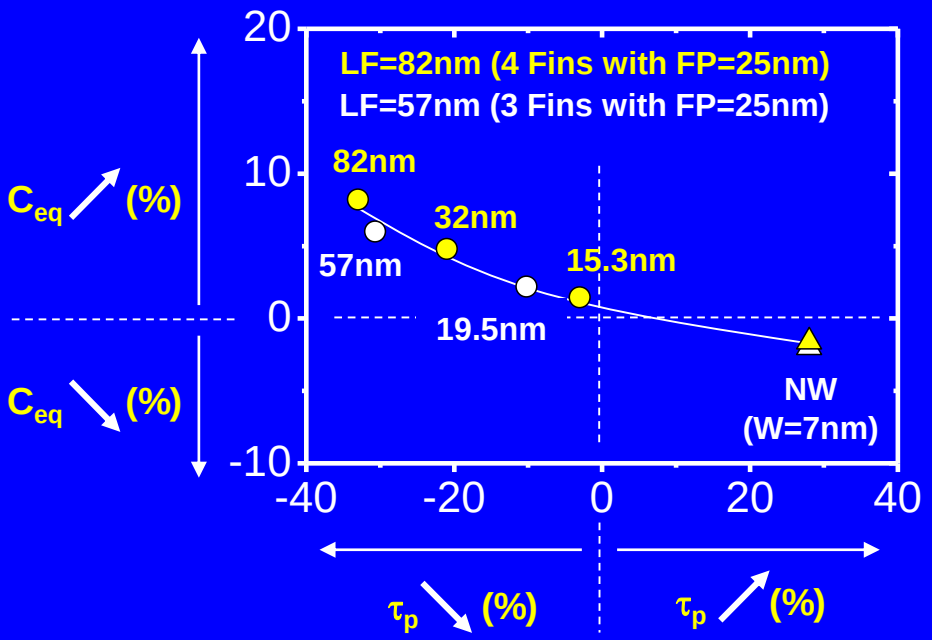




τ: Delay
I_{eff}: Effective drive current
$I_{eff}=(I_H+I_L)/2$
$I_H=I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$
$I_L=I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD})$
Supply voltage V_{DD}=0.7V
FO=3
L_G=16nm
Spacer size: 4.2nm
EOT=0.67nm
$C_{back\text{-}end}$=2fF
M=2: Miller effect in inverter

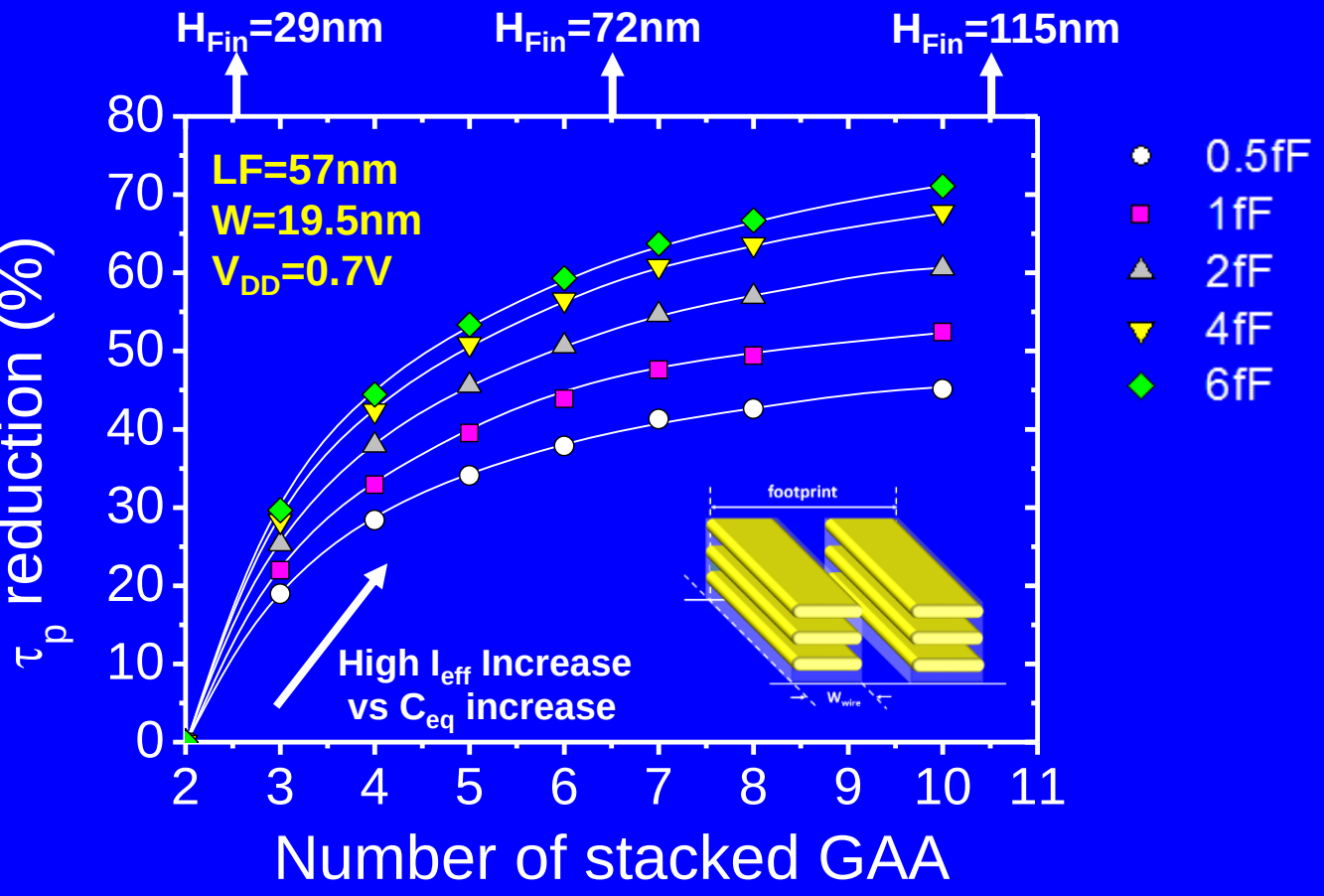
$$\tau = \frac{C_{eq}.V_{dd}}{N_{stack}.I_{eff}}$$

$$C_{eq} \approx (\mathrm{M}+2.\mathrm{FO}).C_{gd0} + {}^{3}/_{4}.\frac{\varepsilon_{SiO_2}.L_g.w_{eff}}{t_{inv}}.\mathrm{FO} + \frac{C_{back-end}}{2}$$



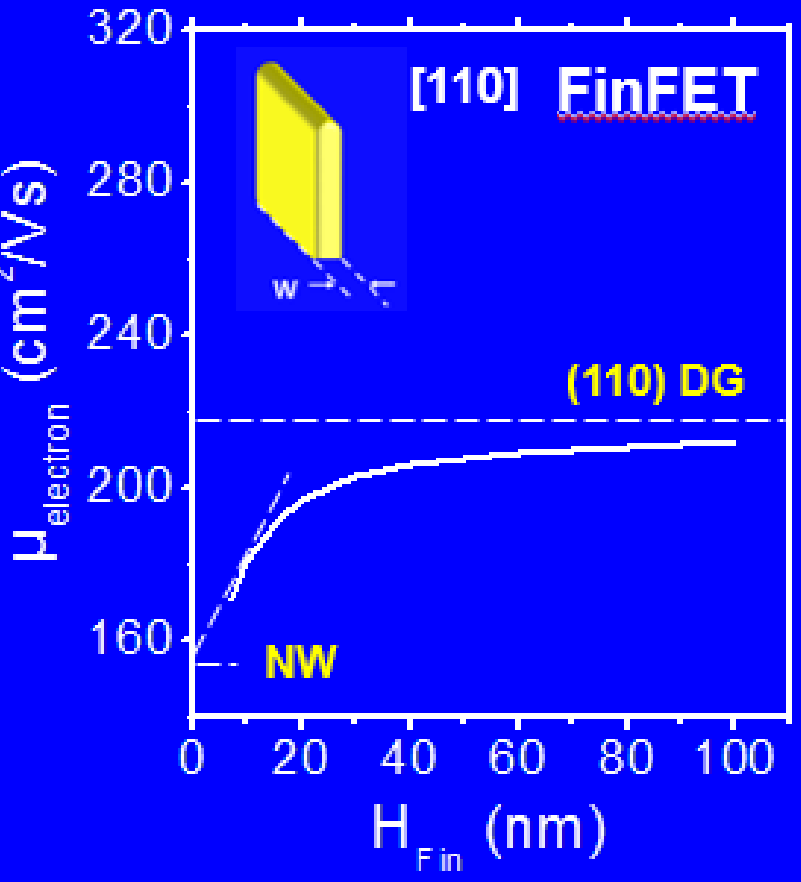
C_{eq} is reduced for NWs (W=7nm) but no delay reduction is achieved, while performance can be significantly improved for nanosheet design having wider wires. A delay reduction of around 20% is expected for W_{NS}~30nm

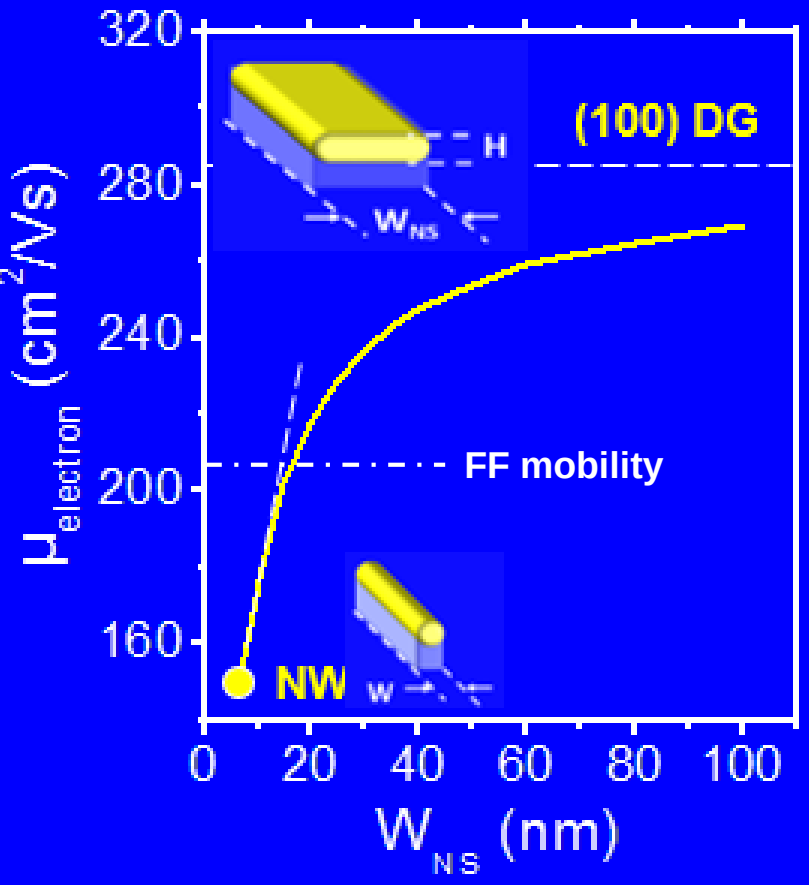
Number of Stacked-GAA NS



Saturation of τ_p reduction when the number of stacked nanowires increase (I_{eff} increase from N to N+1 is close to C_{eq} increase).

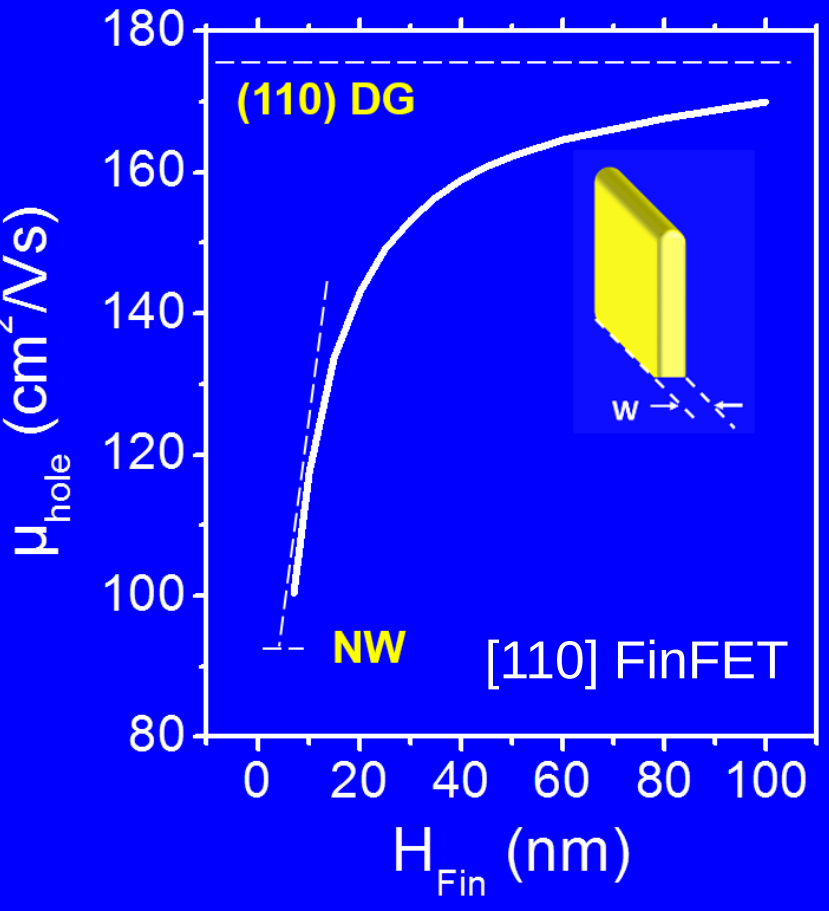
Electron mobility in NW/NS

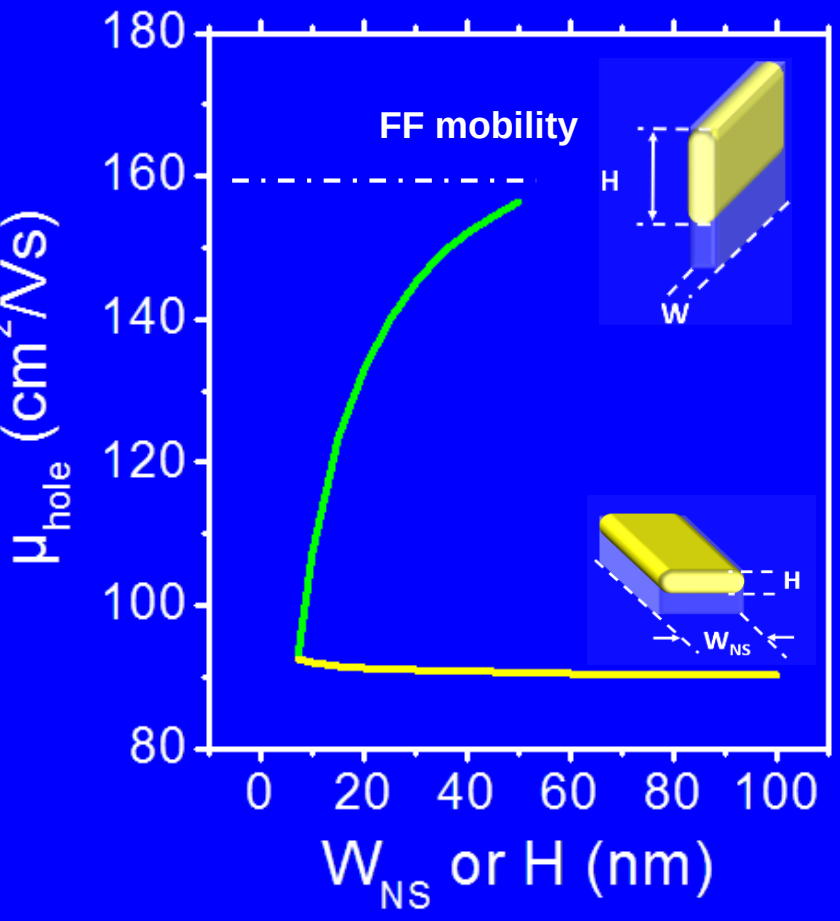




In GAA NanoSheet, $\mu_{electron}$ is increased due to high mobility in the (100) plan.

Hole mobility in NW/NS





Horizontal GAA NS for n-FETs and vertical GAA NS for p-FETs turn out to be the most effective solutions to promote electron and hole transport, respectively.

Outline

- Performance/Design consideration
- **Device Fabrication**
  - **Inner spacer**
  - **SiGe S/D**
- Strain Characterization
  - Precession Electron Diffraction
- Perspectives
- Summary and Conclusion

Devices Fabrication

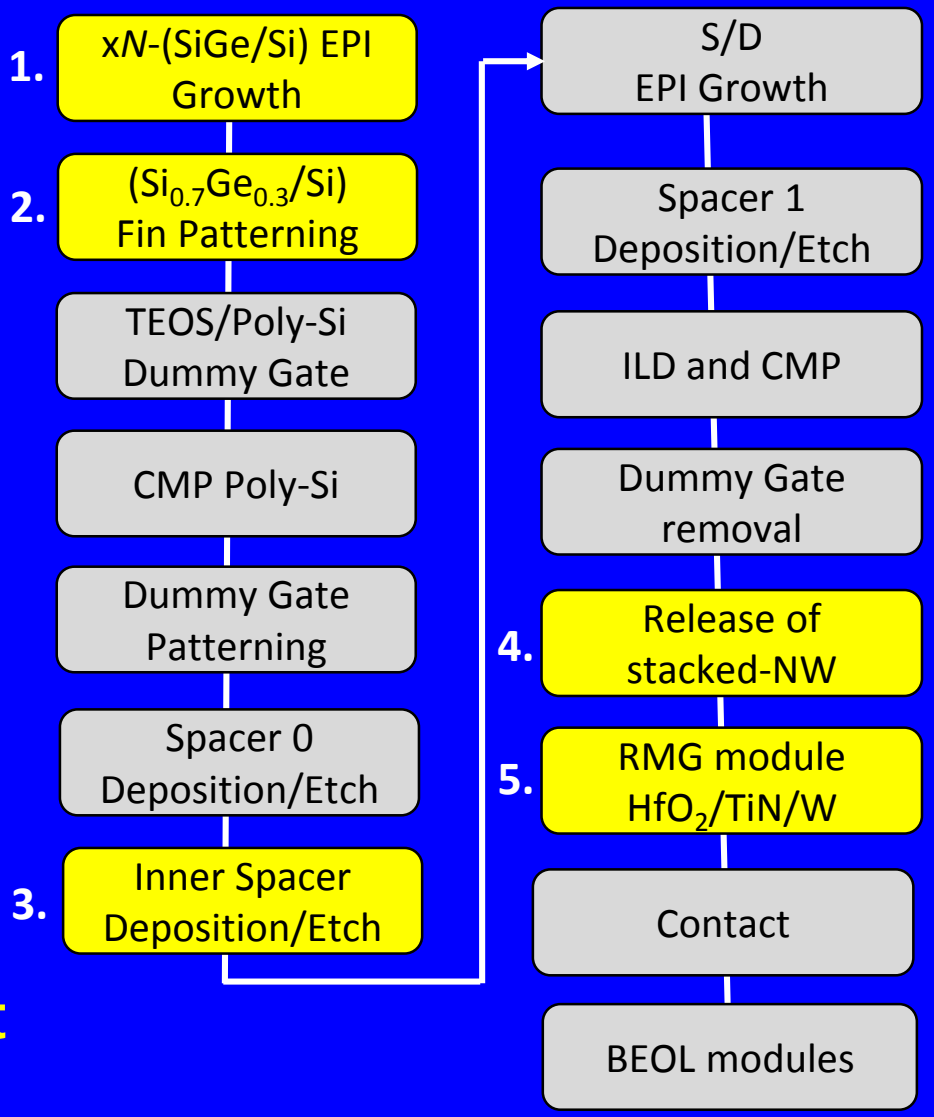
Horizontal Wires

RMG Process
300mm (100) SOI substrates

(Si/SiGe) multilayer:

Option1:
(**Si**/SiGe/**Si**) ≡
(**12nm**/12nm/**12nm**)

Option2:
(**Si**/SiGe/**Si**/SiGe/**Si**) ≡
(**7nm**/8nm/**7nm**/8m/**7nm**)

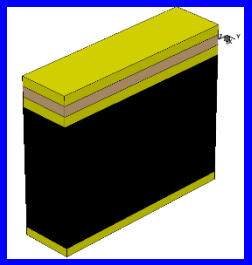


Grey steps are not different that FinFET process-Flow

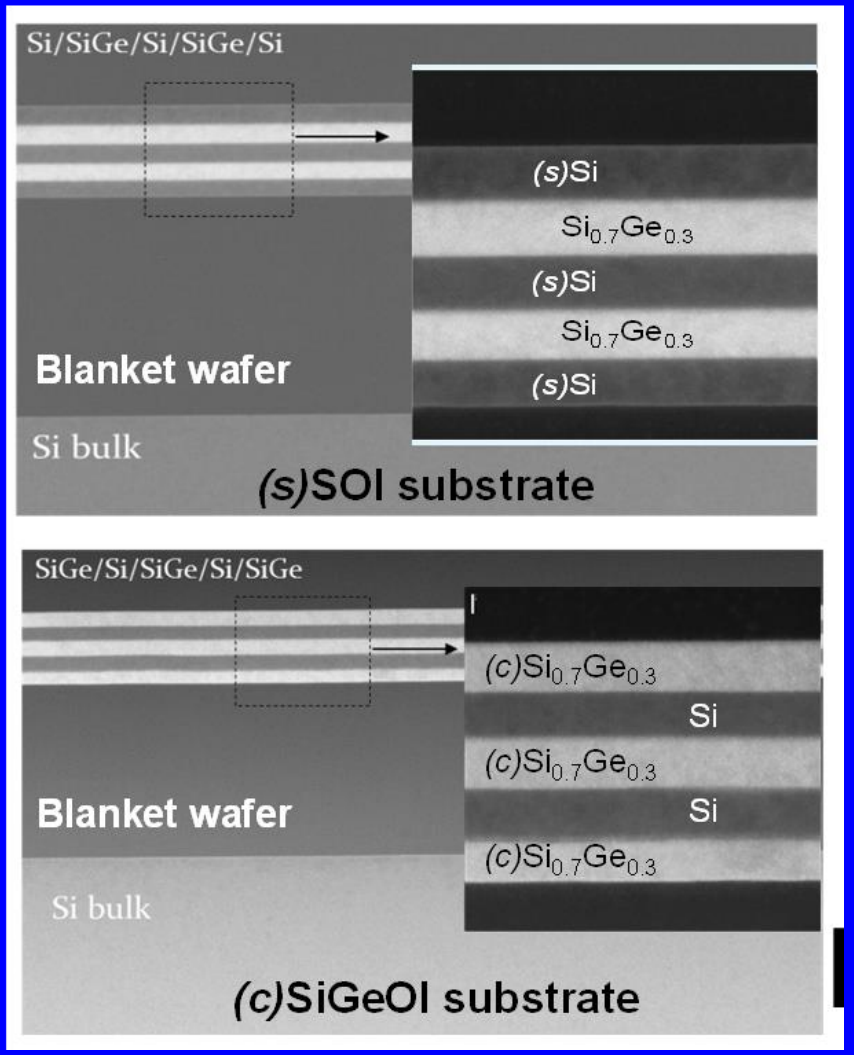
Devices Fabrication

Vertically stacked wires FETs Process-Flow

- **Superlattice (SiGe/Si)**
- Fin Patterning
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- Inner spacer formation
- Source/Drain Epitaxy
- ILD & CMP
- Dummy Gate Removal
- Formation of Suspended NW (release of NW)
- Gate Stack Formation
- Contact/BEOL



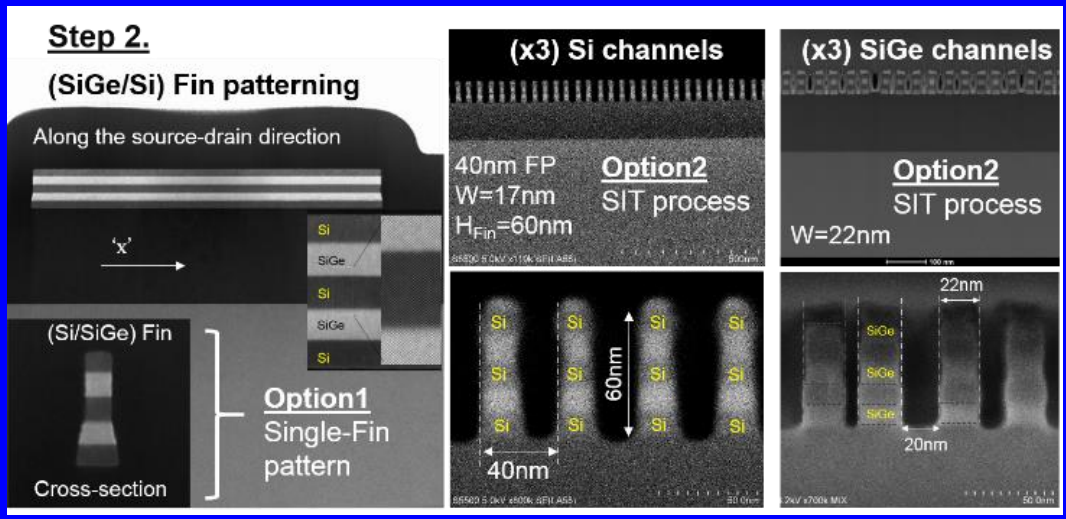
(Si/SiGe) Multi-layers



Devices Fabrication

Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- **Fin Patterning**
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- Inner spacer formation
- Source/Drain Epitaxy
- ILD & CMP
- Dummy Gate Removal
- Formation of Suspended NW (release of NW)
- Gate Stack Formation
- Contac/BEOL



S. Barraud & al. (IEDM 2016)

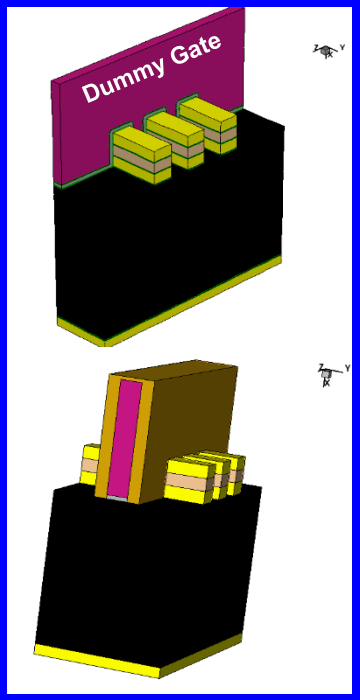
Individual and dense arrays of fins were patterned to fabricate stacked wires FETs. 40 nm Fin pitch / 60 nm height / 20 nm width

Devices Fabrication

Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
- **Dummy Gate Deposition & RIE**
- **Spacer Deposition and RIE**
- Inner spacer formation
- Source/Drain Epitaxy
- ILD & CMP
- Dummy Gate Removal
- Formation of Suspended NW (release of NW)
- Gate Stack Formation
- Contac/BEOL

SiO_2/Poly-Si Dummy Gate



spacer

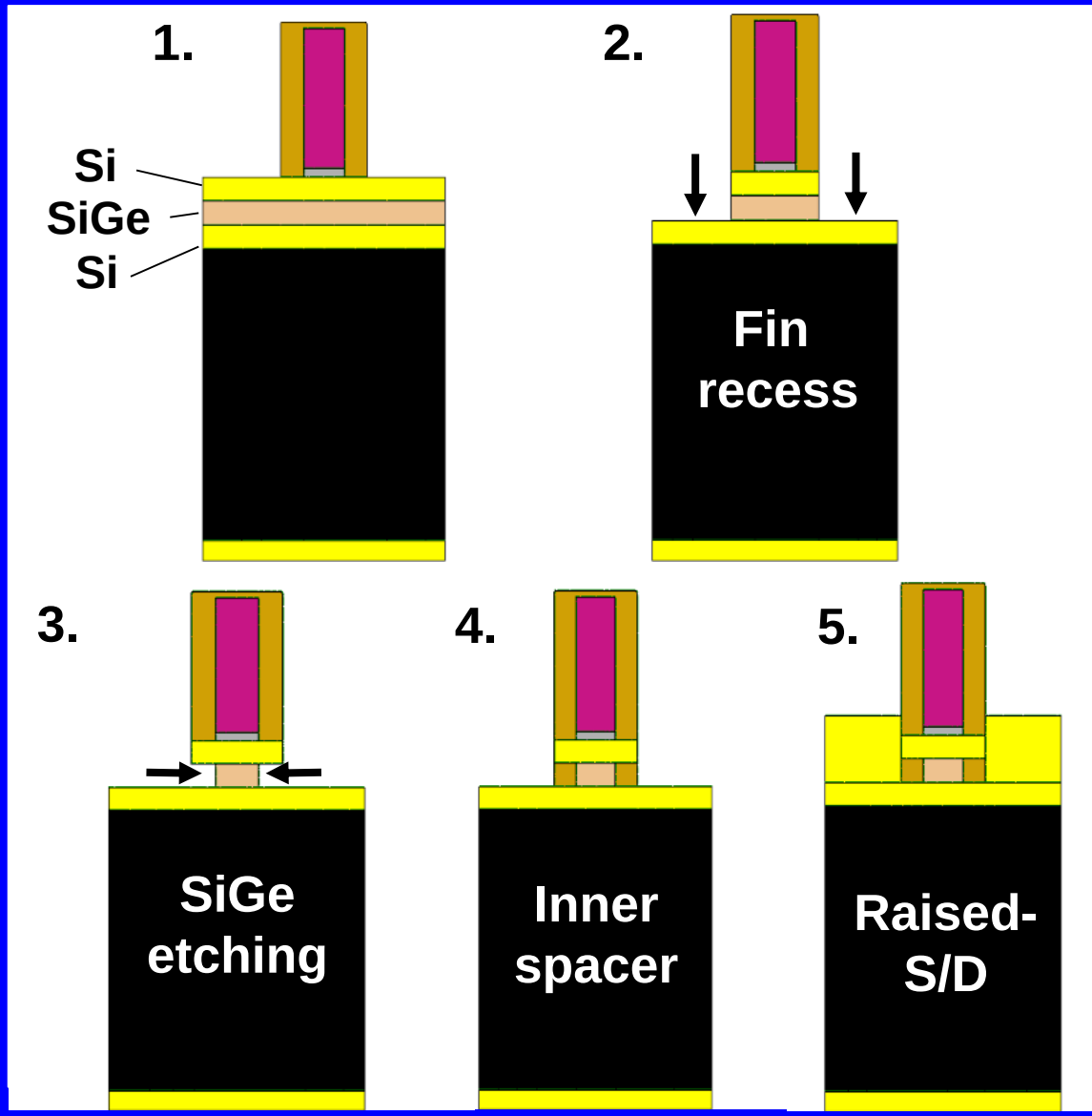
Not different that FinFET

Devices Fabrication

Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- **Inner spacer formation**
- Source/Drain Epitaxy
- ILD & CMP
- Dummy Gate Removal
- Formation of Suspended NW (release of NW)
- Gate Stack Formation
- Contac/BEOL

Definition and benefit of inner spacer ?

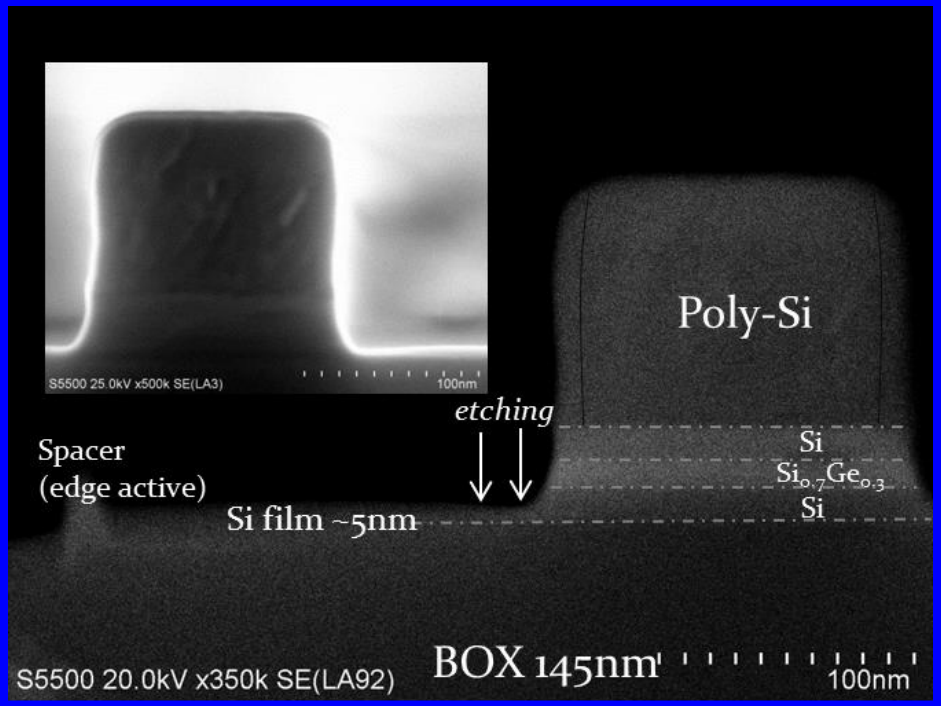


Devices Fabrication

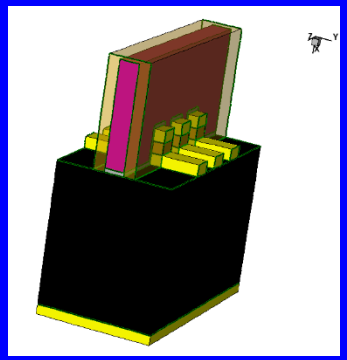
Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- **Inner spacer formation**
- Source/Drain Epitaxy
- ILD & CMP
- Dummy Gate Removal
- Formation of Suspended NW (release of NW)
- Gate Stack Formation
- Contac/BEOL

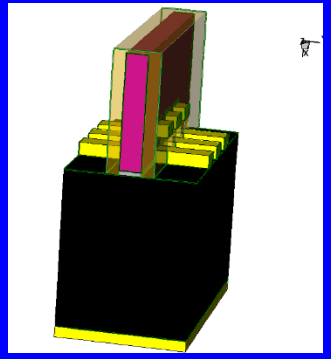
After the Fin recess



Fin recess



SiGe etching

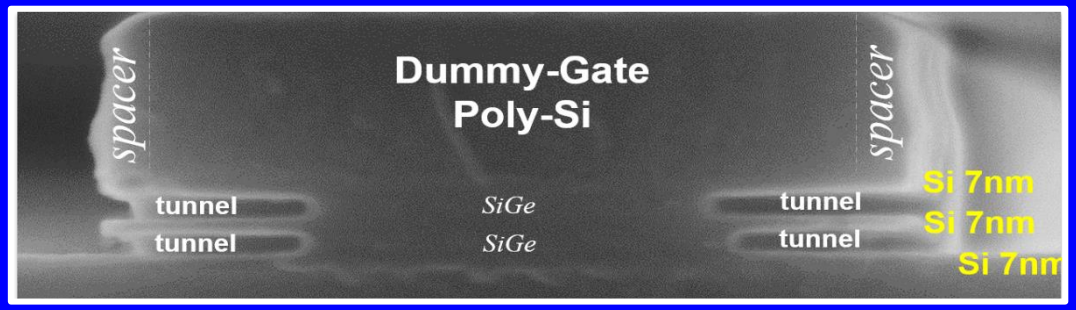


Devices Fabrication

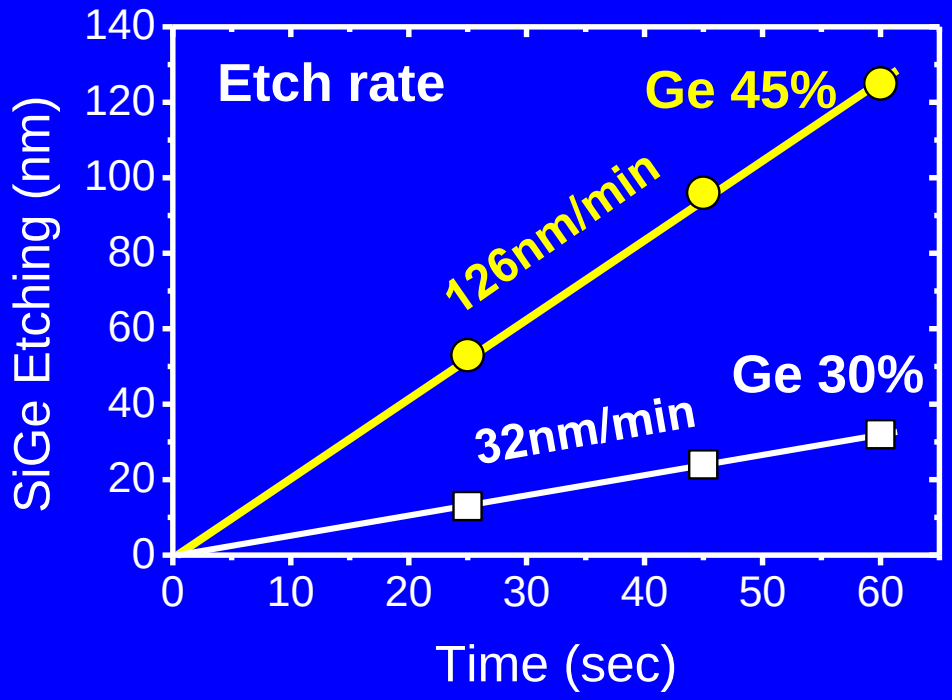
Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- **Inner spacer formation**
- Source/Drain Epitaxy
- ILD & CMP
- Dummy Gate Removal
- Formation of Suspended NW (release of NW)
- Gate Stack Formation
- Contac/BEOL

Second step



Etch depth profile with Si 7nm and SiGe 8nm



Devices Fabrication

Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- **Inner spacer formation**
- Source/Drain Epitaxy
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- Formation of Suspended NW (release of NW)
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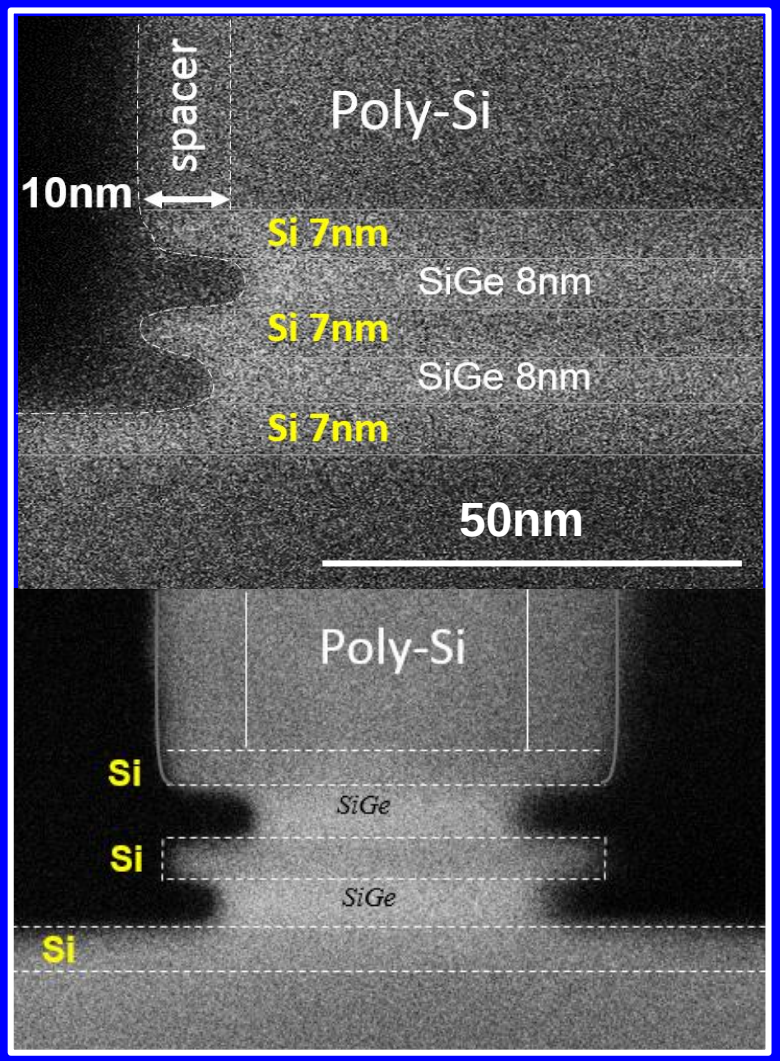

The depth of the SiGe recess was adjusted to match the thickness of future inner spacers

Devices Fabrication

Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
- Dummy Gate Deposition & RIE
- Spacer Deposition and RIE
- **Inner spacer formation**
- **Source/Drain Epitaxy**
- ILD & CMP
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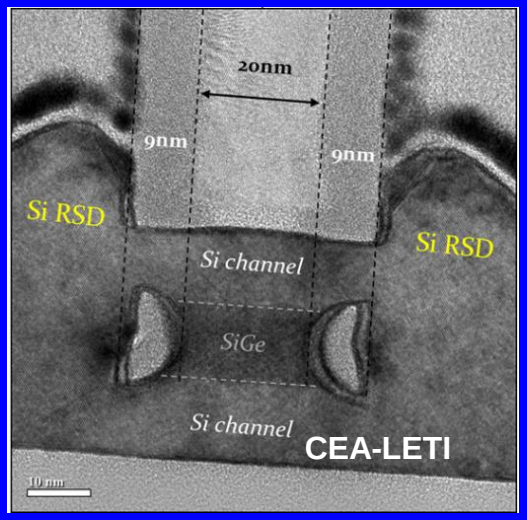
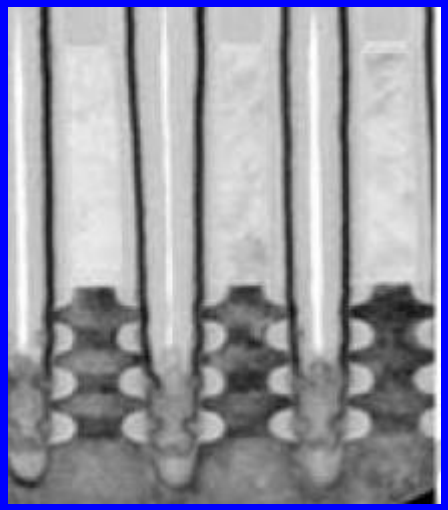
- Gate Stack Formation
- Contac/BEOL

S. Barraud & al. (IEDM 2016)



L_G=20nm
Spacer=9nm
T_{Si}=12nm
T_{SiGe}=12nm



IBM
N. Loubet & al. (VLSI 2017)

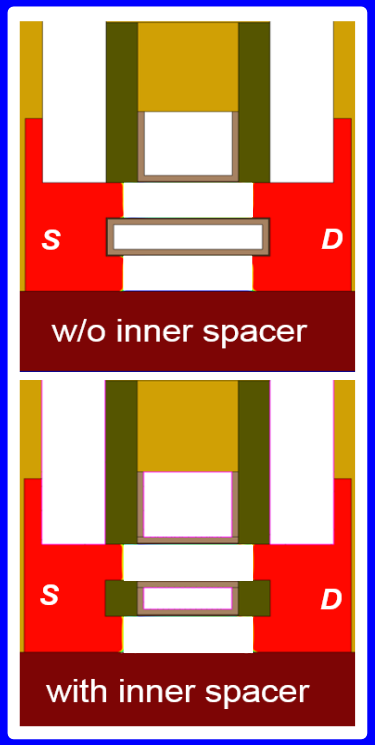
GAA nanosheet (x3)
T_{Si}=5nm
T_{SiGe}=10nm
44/48 CPP ground rules

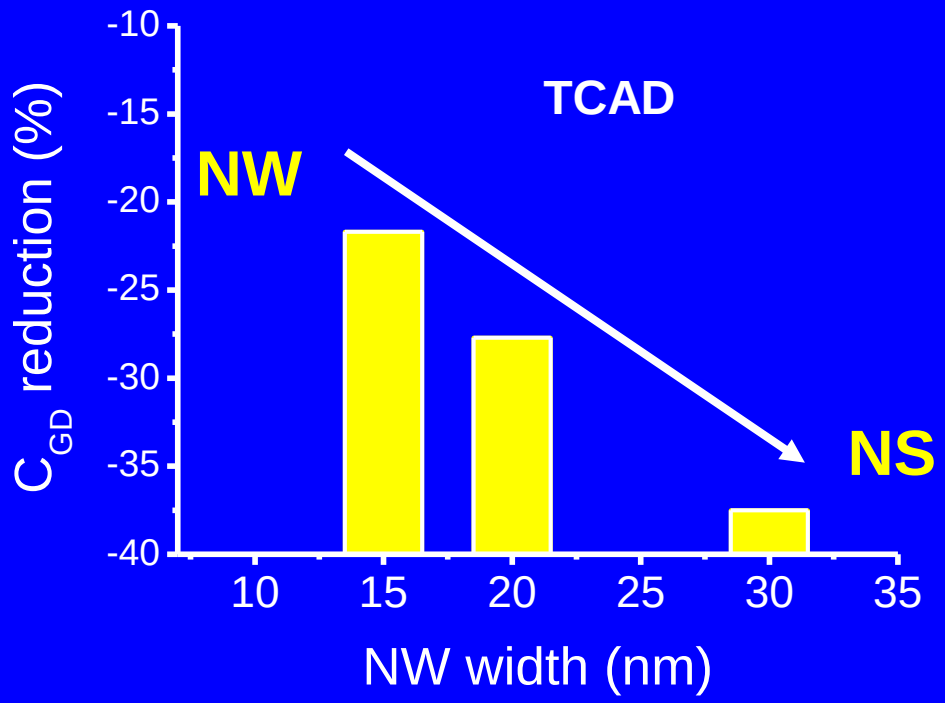
Which benefits for parasitic capacitances?

Benefit of inner spacer

Inner spacer is crucial for reducing intrinsic capacitances and to improve dynamic perf.

L. Gaben & al., ECS (2016)





The benefit of inner spacer is higher as the width is increased → 30-40% reduction of C_{gd} (W=20/30nm)

Devices Fabrication

Vertically stacked wires FETs Process-Flow

- Superlattice (SiGe/Si)
- Fin Patterning
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- Spacer Deposition and RIE
- Inner spacer formation
- **Source/Drain Epitaxy**
- ILD & CMP
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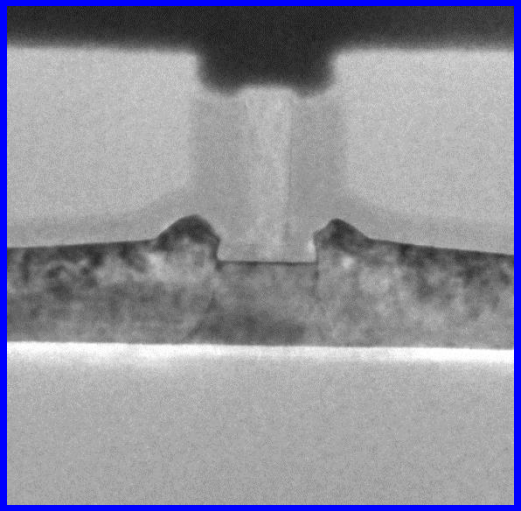
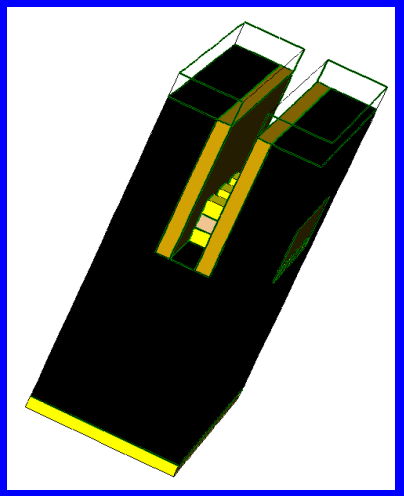
- Gate Stack Formation
- Contac/BEOL





In-situ Boron doped SiGe(:B) Source/Drain

In-situ Phosphorus doped Si(:P) Source/Drain

J. M. Hartmann et *al.*, Thin Solid Films, 520, p. 3185, 2012.

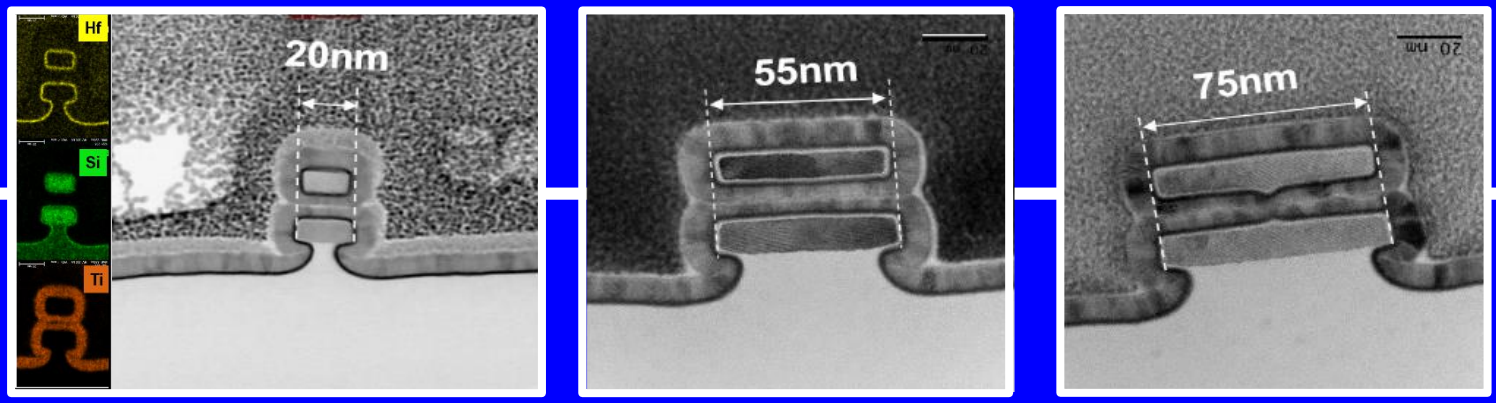
J. M. Hartmann et *al.*, Solid State Electronics, 83, p. 10, 2013.

Wide variety of stacked-wires

LETI
S. Barraud & al., IEDM 2016

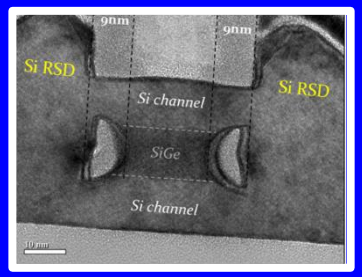
NW/NS Cross-section

NW

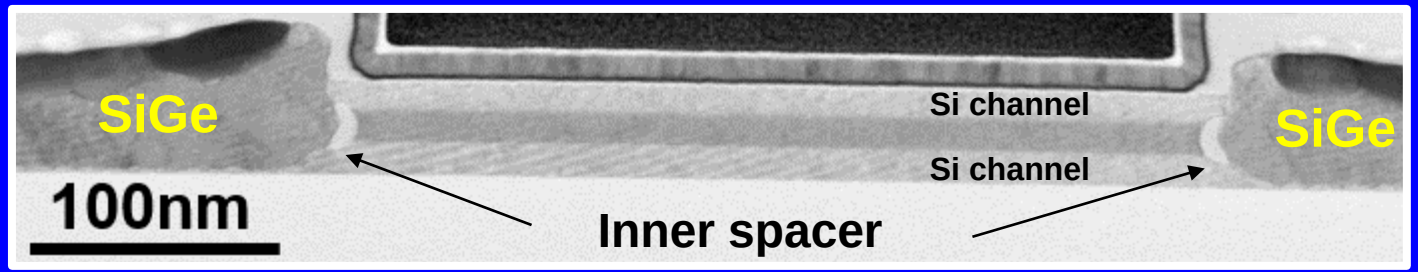


NS

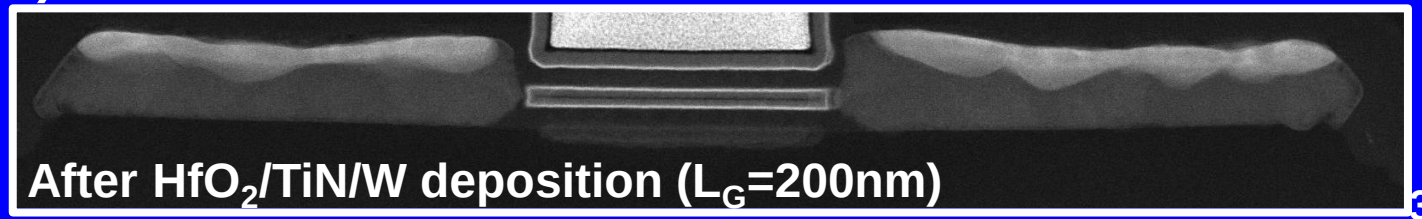
Along source-drain direction



Short-L_G (20nm)



Long-L_G (>300nm)



Strain characterization

1. **Superlattice (SiGe/Si)**
2. **Fin Patterning**
   - Dummy Gate Deposition & RIE
   - Spacer Deposition and RIE
   - Inner spacer formation
3. **Source/Drain Epitaxy**
   - ILD & CMP
   - Dummy Gate Removal
   - Formation of Suspended NW (release of NW)
4. **Gate Stack Formation**
   - Contac/BEOL

Strain engineering is another key factor for stacked-wires FETs.

Strain maps were obtained by TEM using Precession Electron Diffraction technique*

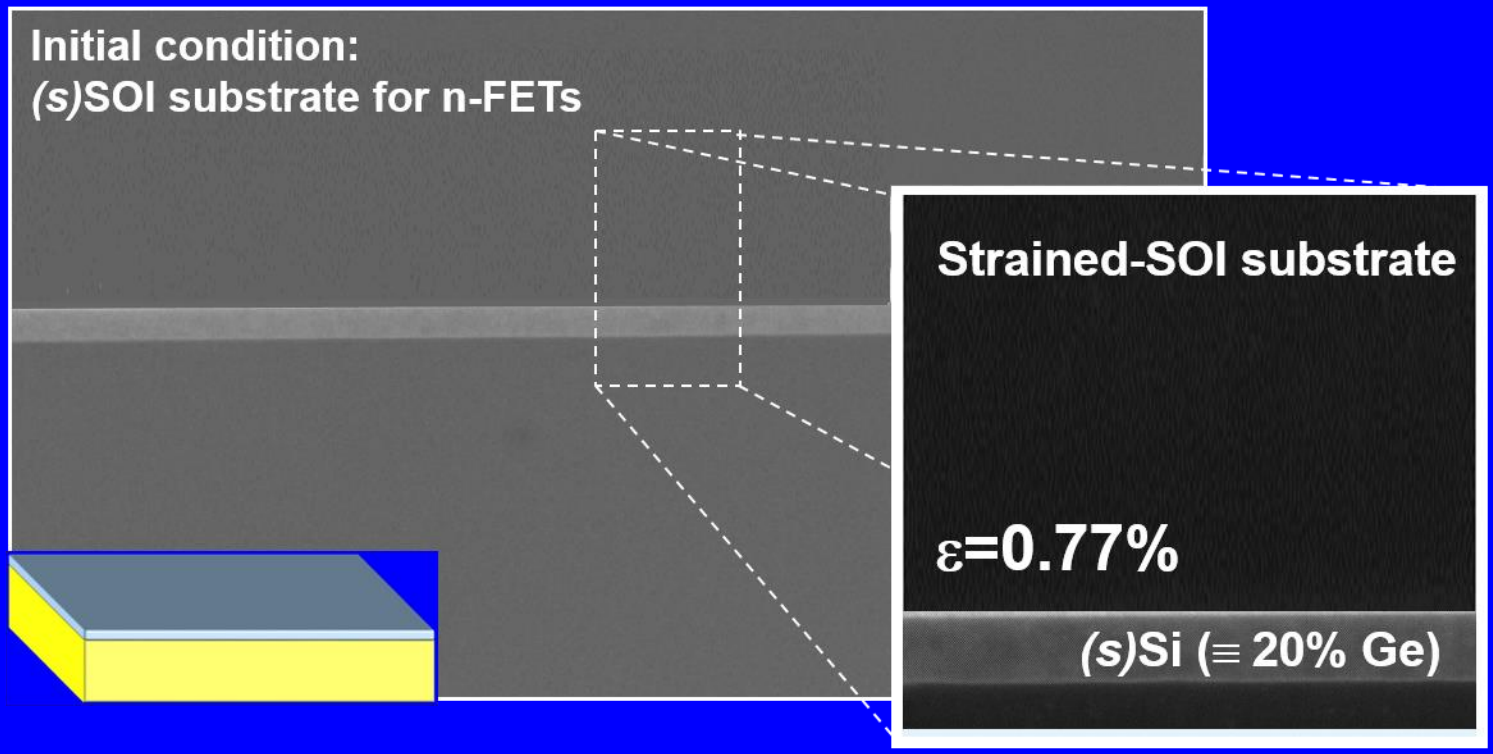
* M.P. Vigouroux et *al.*, APL **105**, 191906 (2014)

* D. Cooper et *al.*, Nano Lett. **15**, 5289 (2015)

Is initial strain (substrate-induced strain) can be used to boost performances?

Strain characterization

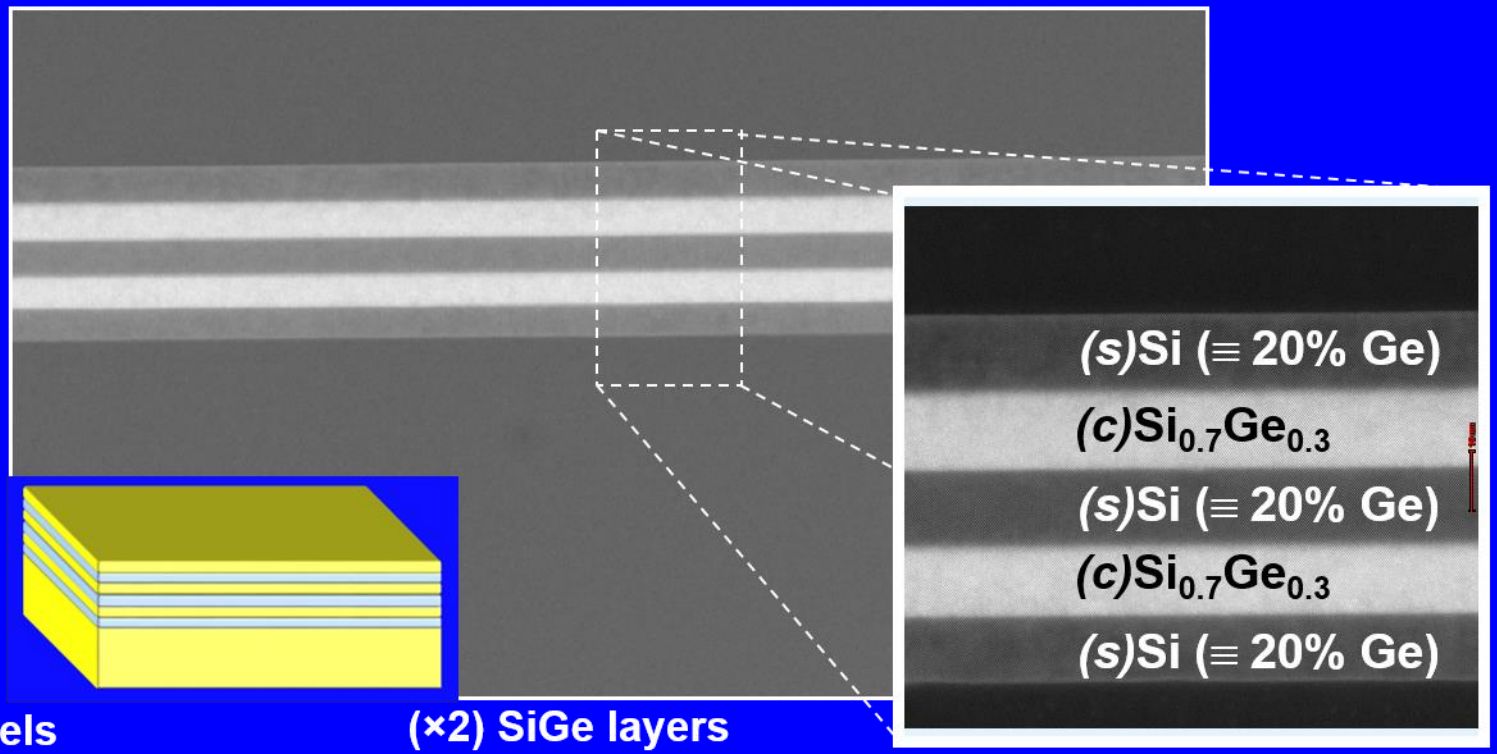
*(s)*SOI substrate for n-FETs



Blanket wafer – strained-SOI substrate (~1.4-GPa biaxial stress)

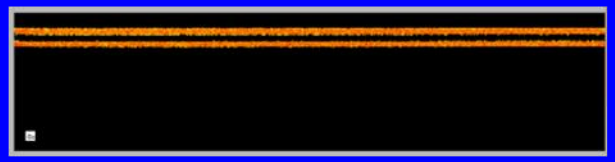
Strain characterization

(SiGe/Si) Superlattices (×3 tensile strained Si channels)



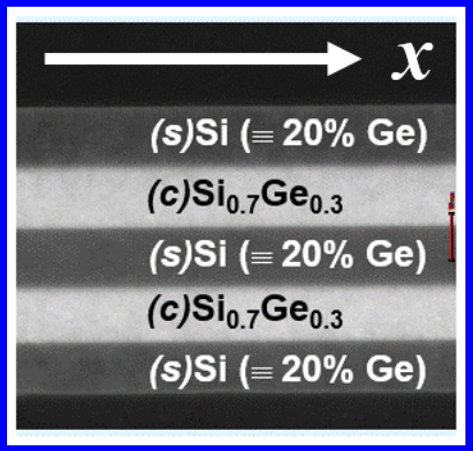
(×3) Si channels

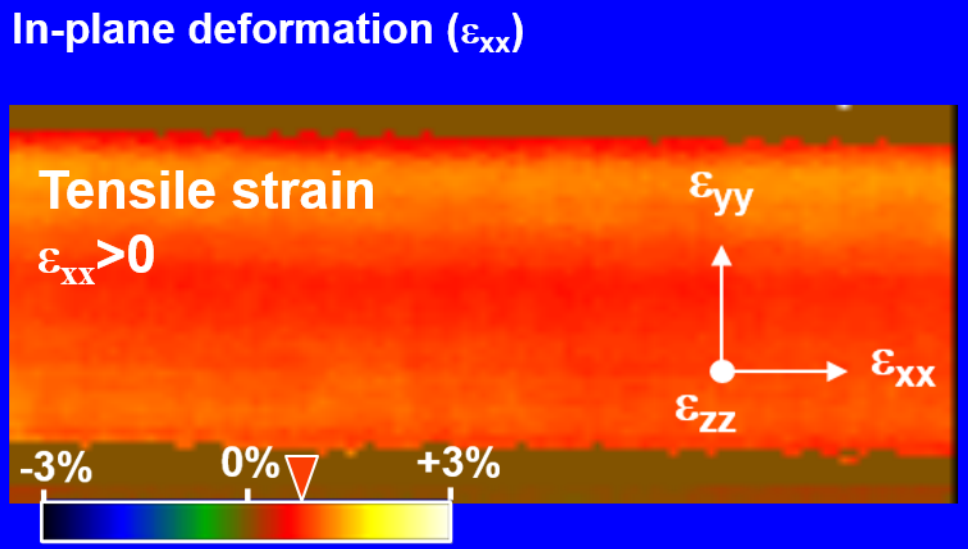
(×2) SiGe layers

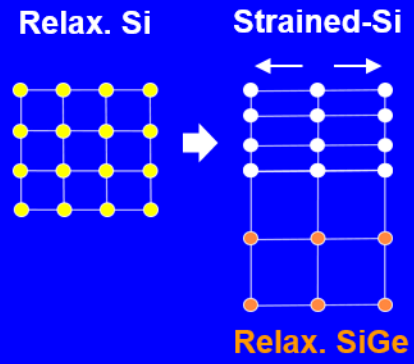


Here, the growth was made on a (*s*)SOI (~1.4-GPa biaxial stress) substrate in order to have ×3 tensile strained Si channels for *n*-FETs.

Blanket wafer data



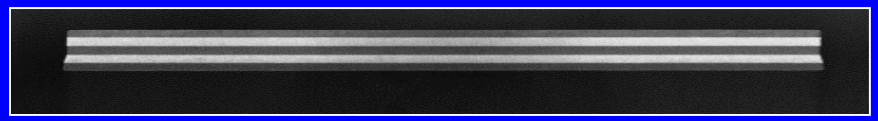




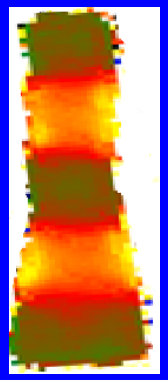
The substrate induced-strain (~1.4-GPa biaxial stress: ε_{xx}=0.77%) is well transferred in the stack.

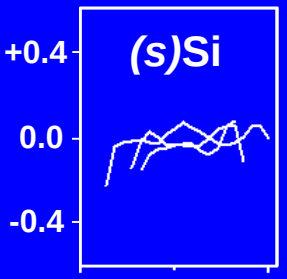
Fin patterning data

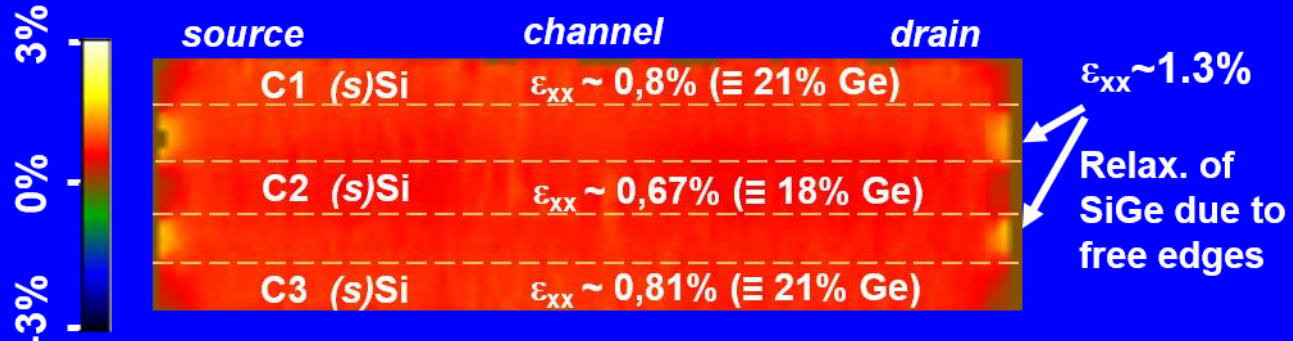
Along the source-drain direction



Def. (ε_{zz})
Fin width

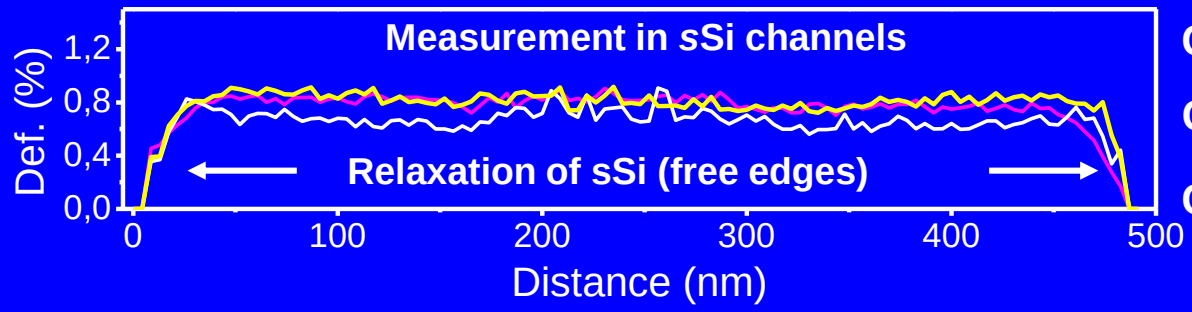




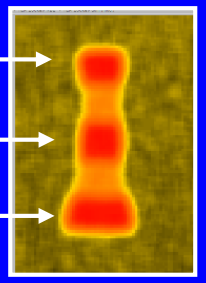


ε_{xx}~1.3%

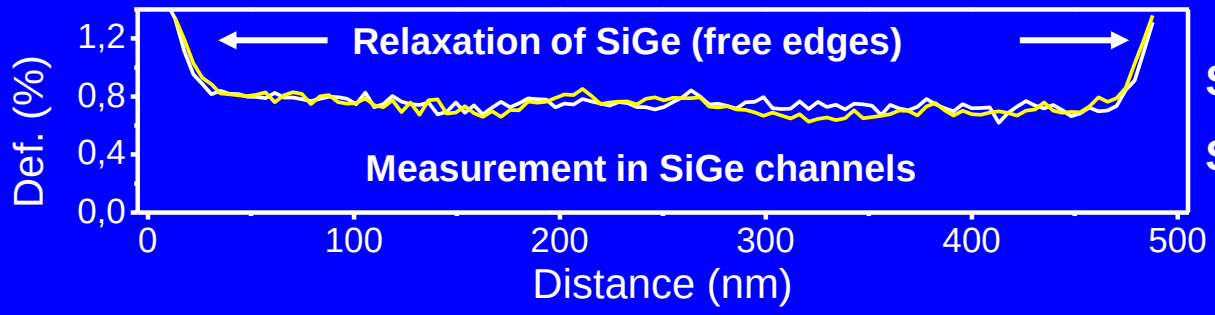
Relax. of SiGe due to free edges



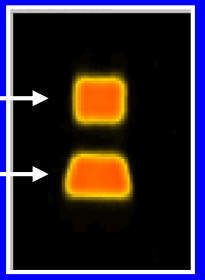
C1
C2
C3



EDX - Si



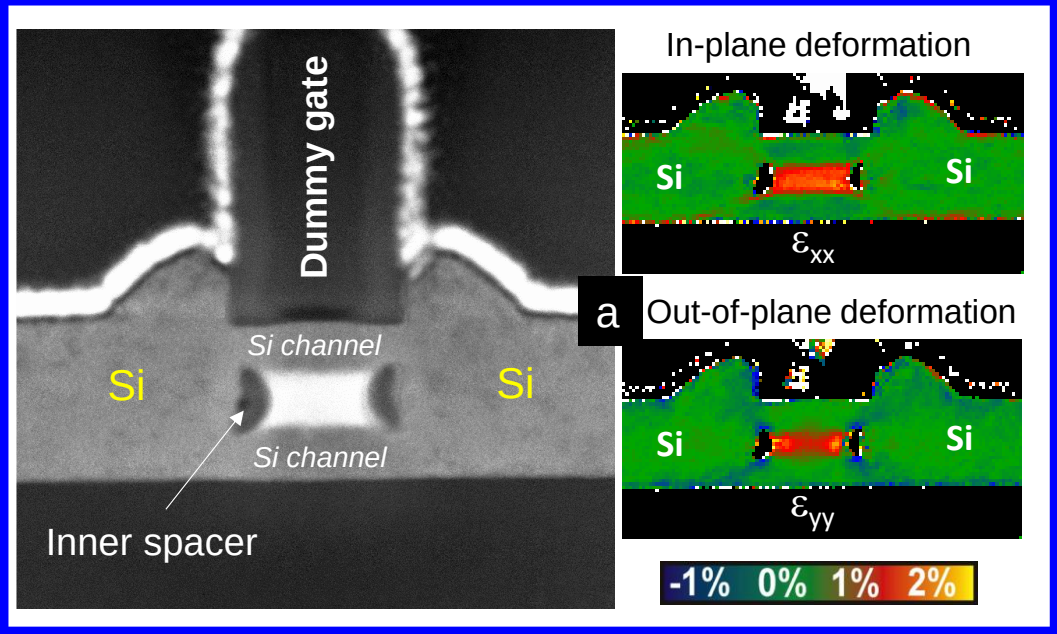
S1
S2

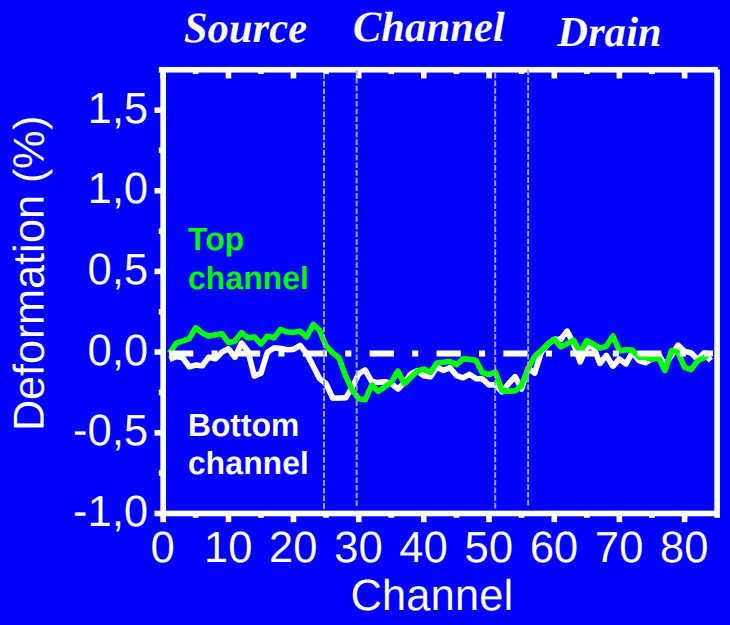


EDX - Ge

Si Source/drain data

In-plane (ε_{xx}) PED deformation maps of stacked-wire transistor. Here, inner spacer and Si source/drain are considered.

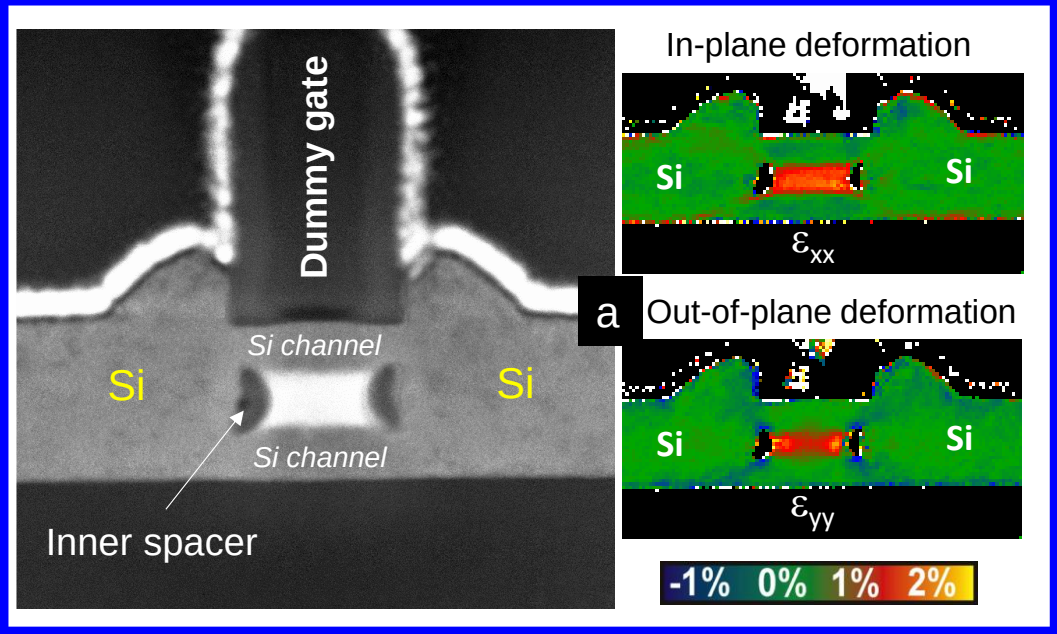


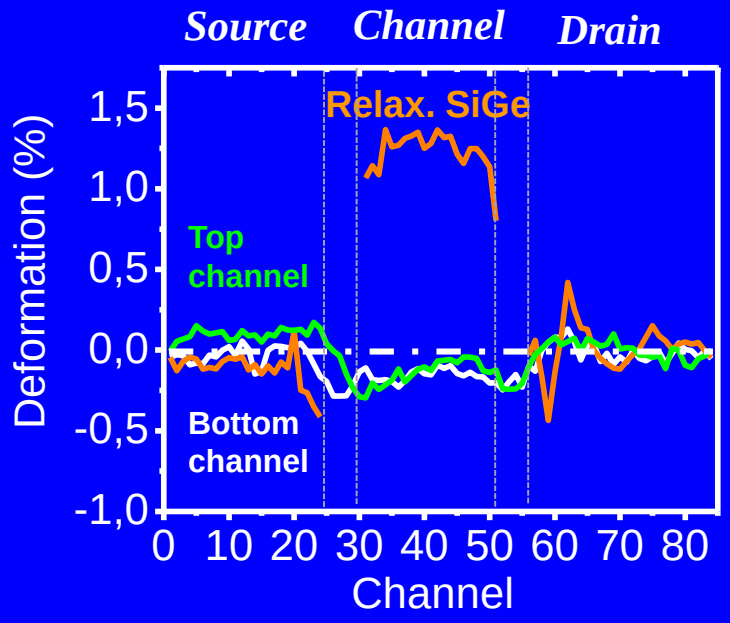


The silicon channels as well as the source and drain are unstrained
→ A deformation close to 0% is observed

Si Source/drain data

In-plane (ε_{xx}) PED deformation maps of stacked-wire transistor. Here, inner spacer and Si source/drain are considered.



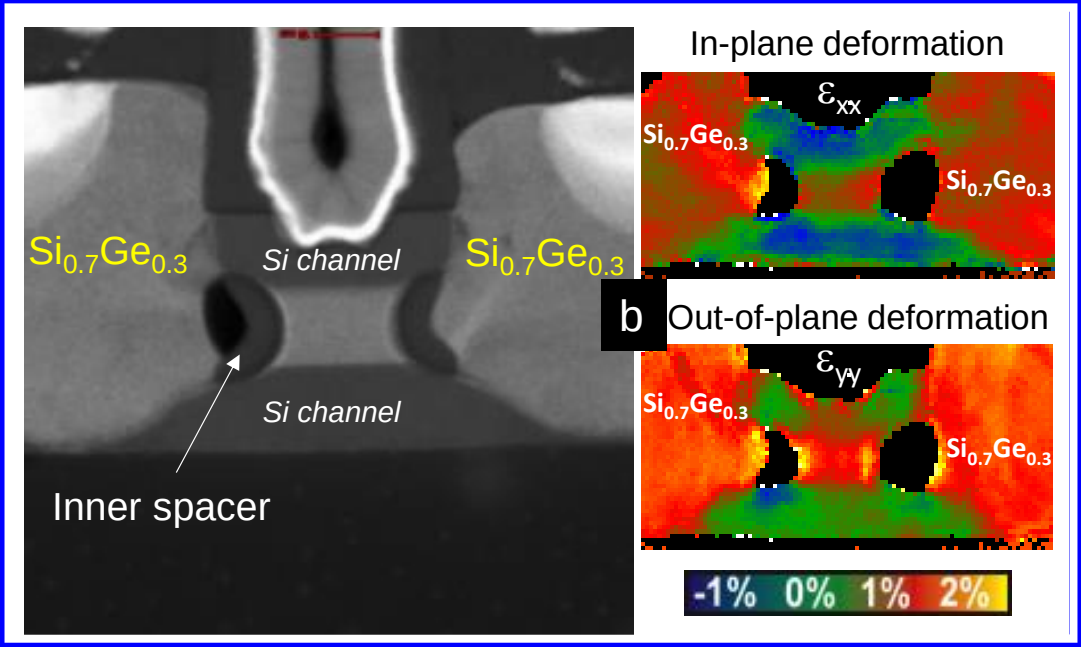


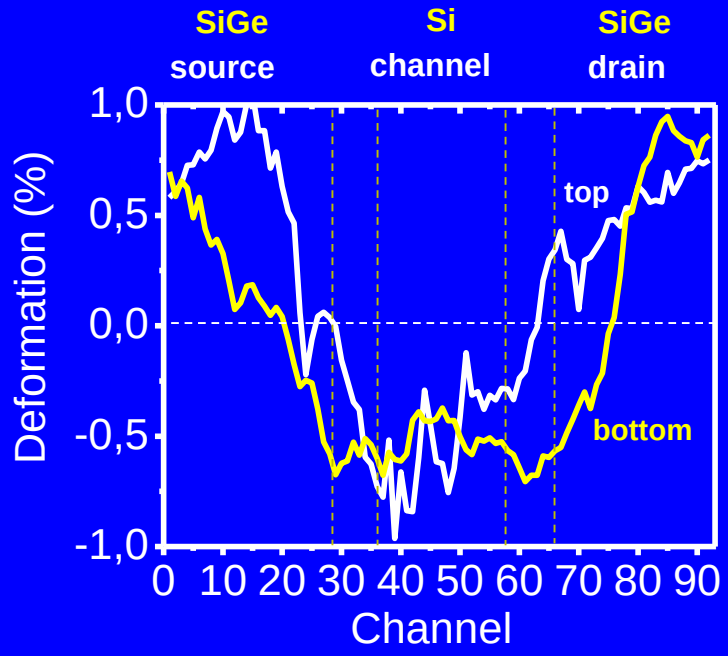
Full strain relaxation of sacrificial $Si_{0.7}Ge_{0.3}$ layer after the Fin recess

➡ **An initial strain (substrate-induced strain) is useless**

SiGe:B Source/drain data

In-plane (ε_{xx}) PED deformation maps of stacked-wire transistor. Here, inner spacer and SiGe source/drain are considered.



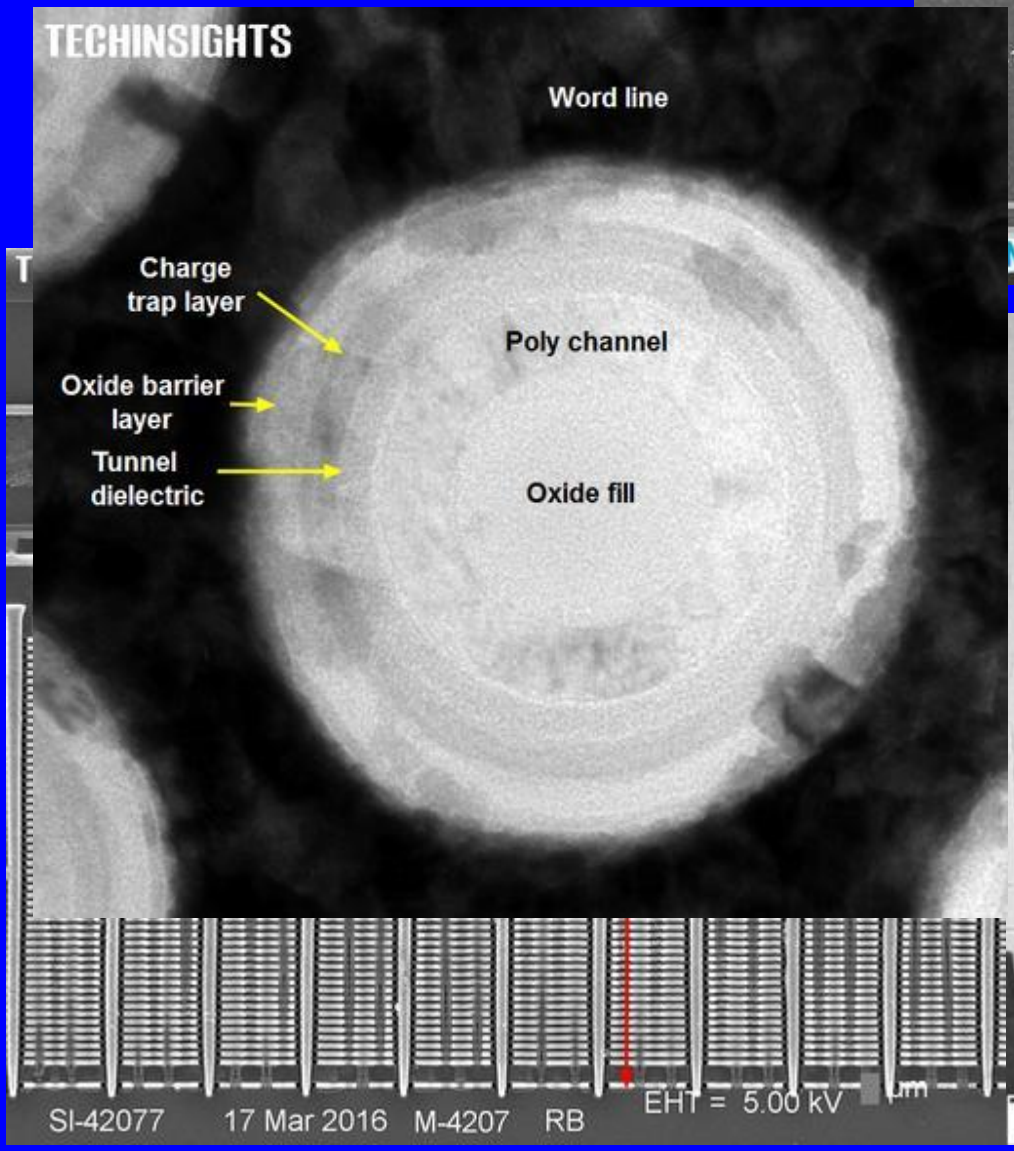


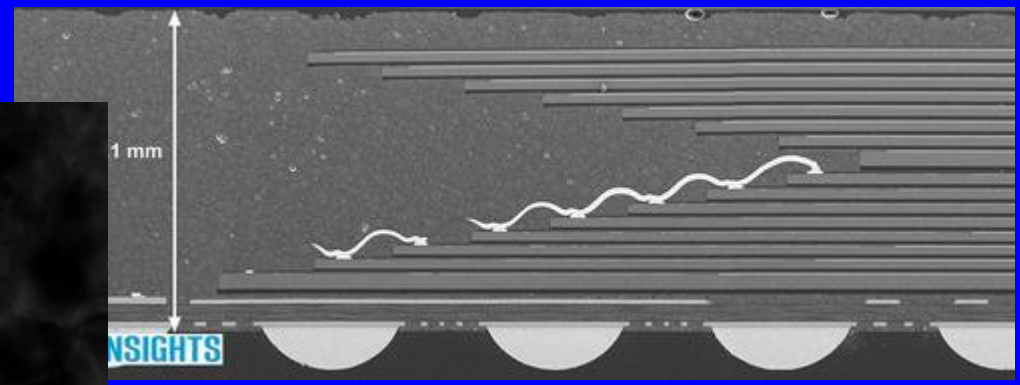
➡ **Optimized engineering of process-induced stress techniques such as SiGe S/Ds (for *p*-FET) can be efficient in 3D stacked-NWs devices**

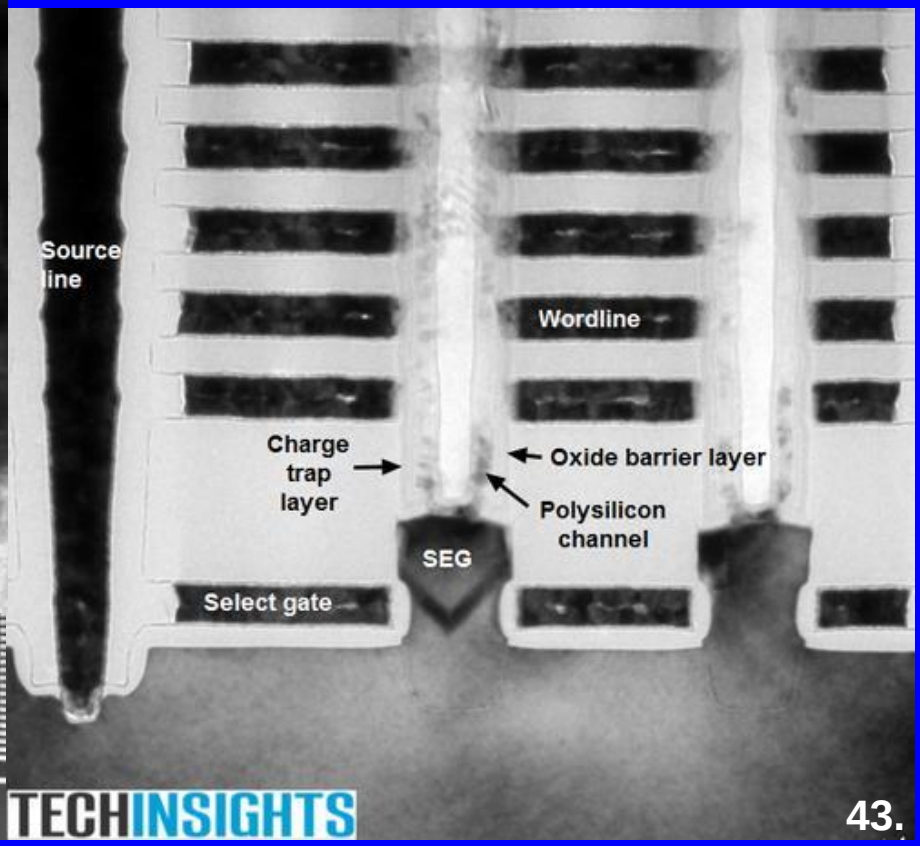
Outline

- Performance/Design consideration
- Device Fabrication
  - Inner spacer
  - SiGe S/D
- Strain Characterization
  - Precession Electron Diffraction
- **Perspectives**
- Summary and Conclusion

Today u-dense nanowire in industry (poly Si)







Next step …

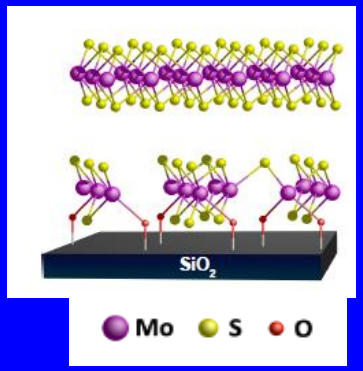
- To switch to crystalline nanowires?
- To mix 3D logic & 3D memories ?
- Both ?

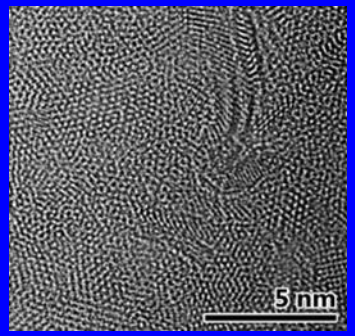
Replace Si by 2D materials?

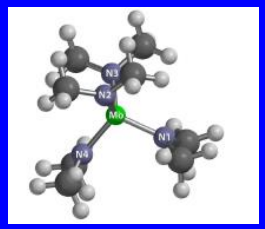
Feasibility of Mo(W)S2 synthesis ALD demonstrated

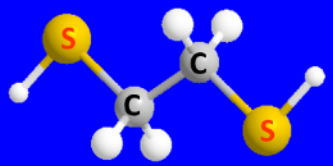
Screening of dedicated precursors, H2S free

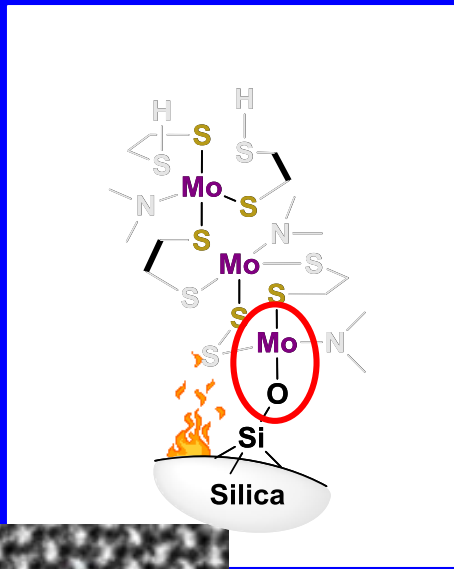
$MoS_{3,3}C_{4,7}H_{12}N$

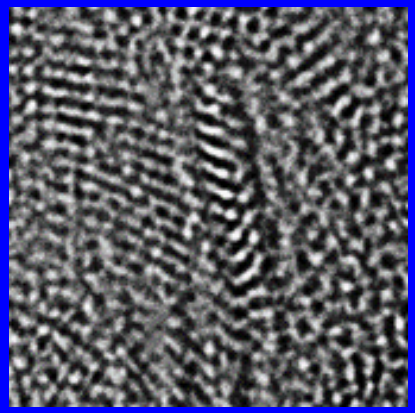




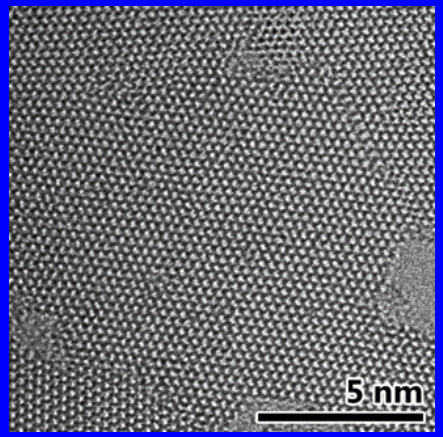


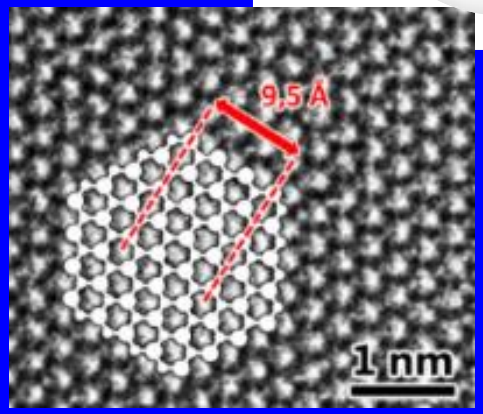






450°C





800°C

leti imac CPE

S.Cadot et al J. Vac. Sci. Technol. A, Nov/Dec 2017, 061502

Summary

- Fabrication of vertically stacked Nanosheet MOSFETs (RMG process) are now demonstrated (inner spacers, SiGe:B S/D, 44/48 CPP)
- Horizontal GAA Nanosheet also have the advantage of being fabricated with minimal deviation from FinFET (FF) devices in contrast to vertical NWs which require more disruptive technological changes
- Strain characterization at different steps of fabrication (PED)
  Efficiency of process-induced strain (SiGe S/D) → significant compressive strain (~0.5 to 1%) in top and bottom Si *p*-channels
- Design flexibility: Nanosheet transistors offers more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width.

Thank You for your attention

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