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Impact of strain on the performance of Si nanowires transistors at the scaling limit: A 3D Monte Carlo / 2D Poisson Schrodinger simulation study

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Abstract— In this work we investigate the correlation between channel strain and device performance in various n-type Si-NWTs. We establish a correlation between strain, gate length and cross-section dimension of the transistors. For the purpose of this paper we simulate Si NWTs with a <110> channel orientation, four different ellipsoidal channel cross-sections and five gate lengths: 4nm, 6nm, 8nm, 10nm and 12nm. We have also analyzed the impact of strain on drain-induced barrier lowering (DIBL) and the subthreshold slope (SS). All simulations are based on a quantum mechanical description of the mobile charge distribution in the channel obtained from a 2D solution of the Schrödinger equation in multiple cross sections along the current path, which is mandatory for nanowires with such ultra-scale dimensions. The current transport along the channel is simulated using 3D Monte Carlo (MC) and drift-diffusion (DD) approaches.

Keywords— *CMOS, electrostatics, nanowire transistors, performance, quantum effects, TCAD, 3D Monte Carlo.*

I. INTRODUCTION

Excellent electrostatic integrity offered by gate all around Nanowire Transistor (NWT) [1]-[2], makes them one of the most prominent candidates to extend Moore's law beyond the 7nm mark and to achieve the ultimate CMOS scaling limits [3]. While it may be possible to enhance charge transport in NWTs by using high mobility materials such Ge, GaAs, InGaAs, and InAs [4], currently silicon remains the material of choice for chip manufacturing. In silicon-based transistors the main option to improve the device performance is to enhance the mobility in the Si based NWTs by introducing strain in the channel [5].

Although strain engineering is a mature technology used to improve CMOS performance, more work is needed to analyse the strain induced enhancement beyond the 7nm node in conjunction with quantum confinement effects [6]. In our recently publications [3][7], we establish a correlation between gate length, geometry and electrostatic driven performance in ultra-scaled Si nanowire transistors (NWT). Our results show that the elliptical cross-section is the best nanowire shape in term of electrostatic confinement. In this paper we extend our work by investigating the effect of strain on charge transport and drive current. We employ the well-established 3D ensemble Monte Carlo (EMC) simulation technique where quantum corrections to the carrier charge

density, necessary at such small nanowire diameters, are accurately taken into accounted by using 2D Poisson-Schrodinger solutions normal to the direction of transport. Four elliptical Si NWTs with different cross-sectional area and with uniaxial strain varying in the range of 0GPa-2GPa are simulated.

II. METHODOLOGY AND MODEL DESCRIPTION

The Monte Carlo method is well suited for capturing the non-equilibrium carrier transport in nano-scale devices [5], [8]–[10]. We employ the GSS 'atomistic simulator' GARAND [11], which includes a three dimensional (3D) self-consistent ensemble quantum-corrected Monte Carlo transport solver. The simulator is capable of handling both electron and hole transport in a variety of materials and nanostructures. The 3D EMC simulations provide accurate physical treatment of the non-equilibrium transport in ultra-scaled channel transistors and result in accurate prediction of the On-State transistor performance (e.g. the ON current - I_{ON}). The initial conditions are pre-calculated using quantum-corrected DD simulations with the quantum mechanical (QM) correction based upon the self-consistent 2D Poisson-Schrodinger solution in each cross-section perpendicular to the transport direction [3], [7], [12], [13]. The QM corrections are fixed and applied throughout the MC transport simulation, maintaining a self-consistent but time-varying electrostatic potential and field distributions. This quantum corrected potential defines the driving force that determines classical particle propagation. The simulator accounts for all the important electron scattering mechanisms, including acoustic phonon, optical phonon, ionized impurity and surface roughness scattering processes [5], The strain induced and confinement related valley splitting is taken into account and carrier statistics are evaluated using a fully degenerate Fermi-Dirac (FD) model that includes the Pauli-Exclusion Principle [14]. A diagram with a brief description of the simulation flow is presented in Fig.1.

III. STRUCTURE OF THE NANOWIRES

The simulated NWTs considered in this paper have four elliptical cross-section areas: 5nm×7.2nm, 4.16nm×6nm, 3.3nm×4.8nm and 2.5nm×3.69nm, equivalent to NWTs with

circular cross section area with diameters 6nm, 5nm, 4nm, and 3nm respectively. Fig. 2 shows the 3D structure of the elliptical cross-section NWT simulated in this work together with the corresponding materials.

Key device parameters are listed in Table 1. In order to make a fair comparison between the set of NWTs, we have kept the aspect ratio, semi-minor to semi-major axis, constant y/z=0.69 in all cases. The direction of transport is along the <110> crystallographic orientation. All NWTs simulated in this paper have effective oxide thickness, EOT= 0.8nm, gate lengths up to 14 nm, spacer thickness of 5nm, source/drain doping peak of 2×10^{20} cm^{-3} and channel doping of 10^{15} cm^{-3}. Table 2 shows the correlation between the dimension of the nanowire and the pitch width. The pitch width is calculated based on assumption of elliptical shape of the wire. We normalized all currents by the ellipse circumference (A/μm).
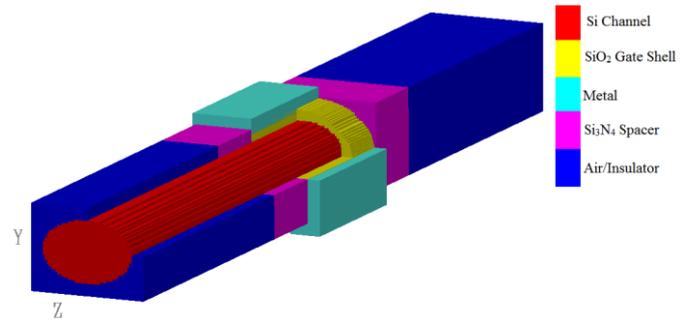

Fig. 2 3D schematic view NWT and material information for the elliptical template of Si NWT.

Table 1 Key device parameters of the Si NWTs.

T_{oxide} (nm)	0.8
Gate length (nm)	6-14
Spacer thickness (nm)	5.0
S/D peak doping (cm^{-3})	2×10^{20}
Channel doping (cm^{-3})	10^{15}
Substrate orientation	001
Nanowire orientation	110
Aspect ratio (y/z)	0.69
Cross-section y(nm)×z(nm)	5×7.2, 4.16×6, 3.3×4.8, 2.5×3.69.

Table. 2. Nanowire cross-section dimensions and the pitch width which is calculated based on approximation of ellipse circumference.

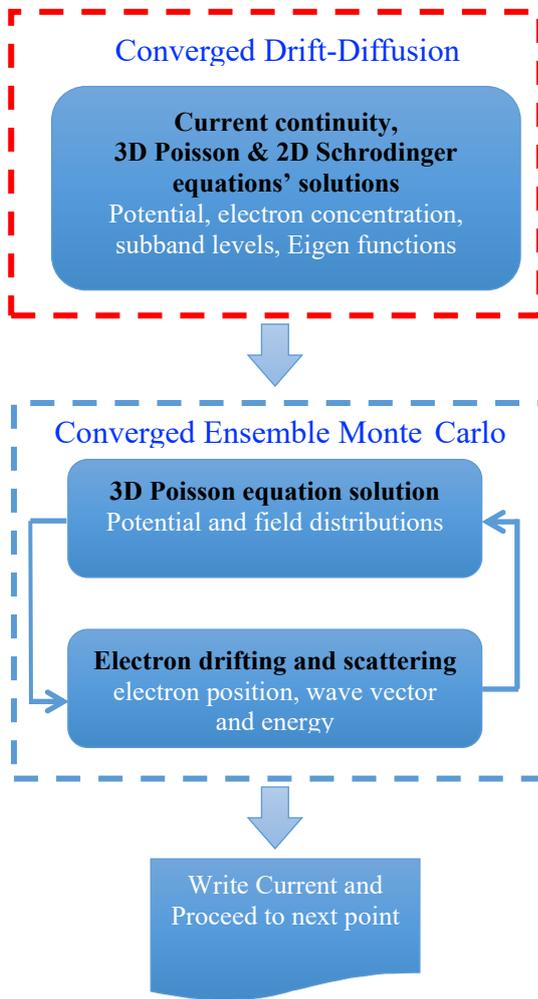| Dimensions (Y×Z)	Pitch
5nm × 7.2nm	0.01952 μm
4.16nm × 6nm	0.01609 μm
3.3nm×4.8nm	0.01286 μm
2.5nm×3.69nm	0.00981 μm

Fig. 1. Simulation flow describing the EMC approach adopted in this work.

IV. RESULTS AND DISCUSSIONS

Fig 3 shows I_D-V_G characteristics for two Si NWTs. The first wire has 3.3nm×4.8nm cross-section and the second one has 5nm×7.2nm dimensions. Moreover, for the 3.3nm×4.8nm NWT, the I_D-V_G characteristics are shown following simulation without stress and with the application of 1.0GPa tensile uniaxial stress. The results are compared with the simulated I_D-V_G characteristics for the largest cross-section (5nm×7.2nm) nanowire without stress, where the current have been normalized by the equivalent pitch. The I_D-V_G characteristics for all the devices have also been aligned by fitting the work-function to give an identical leakage current of I_{off} = 6×10^{-10} (A/μm). The data presented in Fig.3 show that introducing strain in the channel improves the drive current by 48 %. Secondly, as expected, the larger cross-section nanowire has higher I_{ON} current in comparison to the smaller nanowire that is also unstressed. However, introducing 1.0GPa stress in smaller cross-section nanowire delivers around 30% higher ON-current in comparison to the larger cross section NWT.

More detailed analysis in terms of device performance can be obtained from the data presented in Fig. 4, which shows I_D-V_G characteristics for all four devices at four different applied strain levels. Similar to the results discussed above strain can

improve drive currents by 20%-50%. It must be emphasised that the NWT with 3.3 nm x 4.8 nm cross section with 2.0 GPa stress delivers current twice as large as the the nanowire with a 5nm x 7.2nm and no applied stress. From the results for the other NWTs with cross-sections of 2.5nm x 3.69 nm and 4.16 nm x 6 nm, it is clear that all NWTs with larger diameter have better Ion. This is an important conclusion and will affect the design optimisation process.

Fig. 5 reveals the dependence of the threshold voltage on the gate length at 5 different strain conditions. Overall the V_T decreases with decreasing the gate length. Also the gradient of V_T increases moving towards shorter gate lengths while the strain decrease V_T by 11% at shorter gate length and up to 15% at long gate length.

Another indicator for the short channel effects is the DIBL (see Fig. 6). As expected the DIBL increases with decreasing the gate length, for NWT 2.5nm x 3.69 nm DIBIL varies from 27mV/V to 5mv/V for gate lengths 6nm and 14nm respectively while it gradually decrease from 80mmV/V to 17mV/V when the gate length varies from 6nm to 14nm for NWT 5nm x 7.2nm cross section. Also the device with the larger cross-section shows higher DIBL compared to all other cases.

The 2D charge distribution for all devices is presented in the Fig. 7. It is clear from the picture that total amount of charge in the wire increases with decreasing the cross-section. Also, at the smallest wire even though that the shape is elliptical the charge distribution has shape close to spherical distribution.
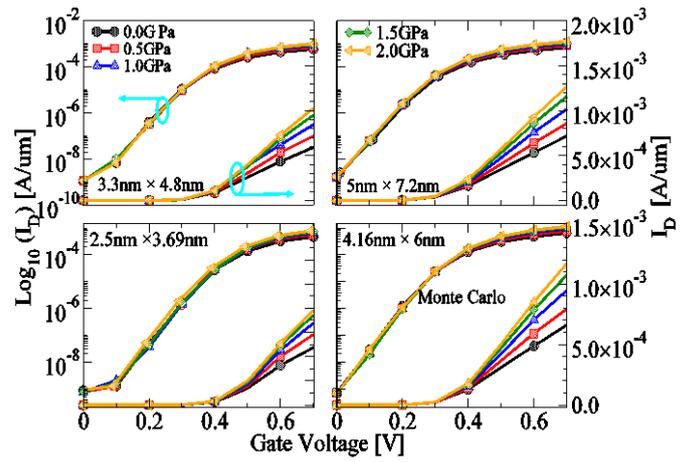

Fig.4 I_D-V_G curves for four different applied strain on elliptical Si NWT with four different cross-section dimensions: 5nm×7.2nm, 4.16nm×6nm, 3.3nm×4.8nm, and 2.5nm × 3.69nm. All results are normalized by pitch length.

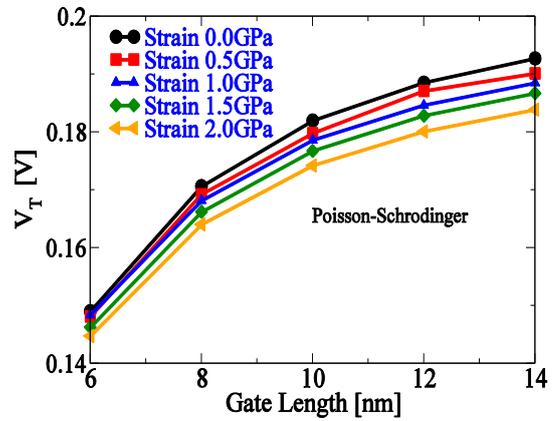Fig.5 Dependence of the V_T on gate length (L_G) for four applied strain in NWT with 3.3nm×4.8nm cross-section.
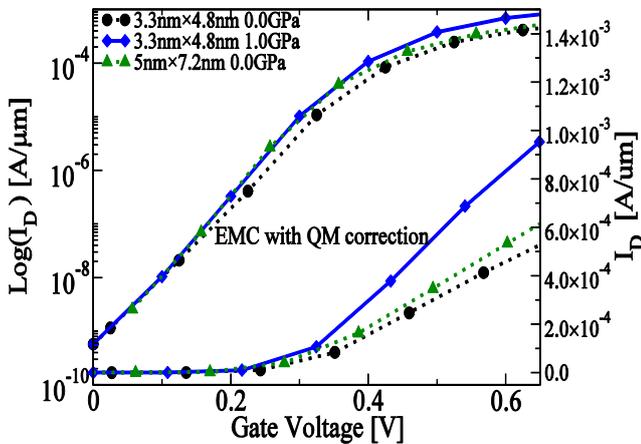

Fig3 I_D-V_G characteristics for 3.3nm×4.8nm cross-section with and without strain compared with unstrained 5nm×7.2nm normalized by (equivalent pitch) and aligned at leakage current (I_{off}) 6x10^{-10}A/um by employed Poisson-Schrödinger with MC.
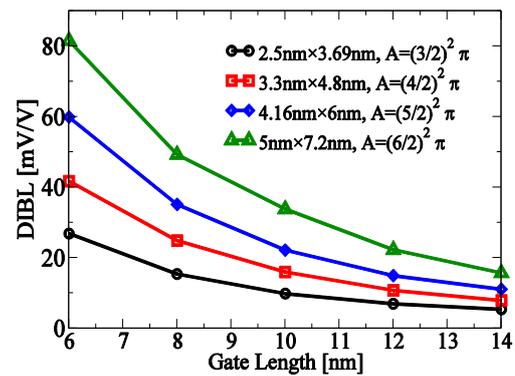

Fig.6 Impact of gate length on the DIBL for different and gate length (LG) for four different cross-section dimensions: 5nm×7.2nm, 4.16nm×6nm, 3.3nm×4.8nm, 2.5nm×3.69nm.
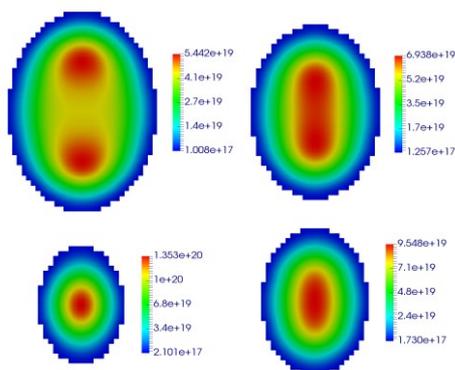
Fig.7 2D charge distributions in the middle of the channel for elliptical wires with cross- of 5nm×7.2nm, 4.16nm×6nm, 3.3nm×4.8nm, 2.5nm×3.69nm.

V.   CONCULUIONS

In this work we reported the correlation between channel strain, gate length and cross-section dimensions of n-type Si NWTs performance. We have demonstrated that introducing stain in the channel enhances the drive current. Also, introducing 2.0GPa strain in a nanowire with 4nm (3.3nm×4.8nm) cross-section could deliver around 50% higher I_{ON} current when compared to of unstrained 6nm (5nm×7.2nm) nanowire. Moreover, we have shown that the DIBL decreases with increasing gate length and the V_T has the opposite trend, V_T reduces with decreasing gate length. Overall, our work shows that combination of strain and device cross-section could improve the device performance at such ultra-scaled NWT's dimensions which are discussed above.

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