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High and low-field contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework

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***Abstract*—We compute the contact resistances at low drain bias in Trigate and FinFET devices with widths and heights in the 4 to 24 nm range, using a Non-Equilibrium Green's Function approach. Electron-phonon, surface roughness and Coulomb scattering are taken into account. The analysis of the quasi-Fermi level profile reveals that the areas under the spacers are major contributors to the contact resistance at low field, due to the poor electrostatic control over the carrier density under the spacers. The impact of design parameters (cross-section and doping profile) on the contact resistance is analyzed and the simulations are compared to experimental data. At high drain bias, the contributions of phonons and impurities scattering in the source and drain are also computed and discussed.**

I. Introduction

As the gate length L of field-effect transistors is reaching the sub-20 nm range, the contact resistances are increasingly limiting the electrical performances of the devices [1], [2], [3], [4]. In the low field (low V_{ds}) regime, the "apparent" contact resistance R_c can be defined as the extrapolation to zero gate length of the total resistance of the device, $R(L) = V_{ds}/I_{ds}$, where I_{ds} is the drain current and V_{ds} the source-drain voltage. At low V_{ds}, this contact resistance is dominated by i) the quality of the metal-semiconductor contact, ii) the transport through the lowly doped regions of the devices such as the spacers, and iii) the "ballistic" resistance of the channel [5], [6] (usually mixed into the apparent contact resistance as it is independent on the gate length). In the high V_{ds} regime, the resistance is no more linear with respect to the gate length, so R_c cannot be computed from the same quasi-equilibrium techniques. In this work, we compute components ii) and iii) of the contact resistance at low and high field in Fully-Depleted Silicon-on-Insulator (FDSOI) Trigate and FinFET devices in a Non-Equilibrium Green's Functions (NEGF) framework [7], [8]. At low field, the contact resistance is computed with a $R(L)$ extrapolation further supported with a quasi-Fermi level analysis. The impact of some technological parameters (doping profile and channel cross-section) on the contact resistance is then investigated. This low field study is validated by comparison with electrical measurements on Trigate devices fabricated at CEA-LETI. Finally some components of the source and drain resistance are computed at high drain bias.

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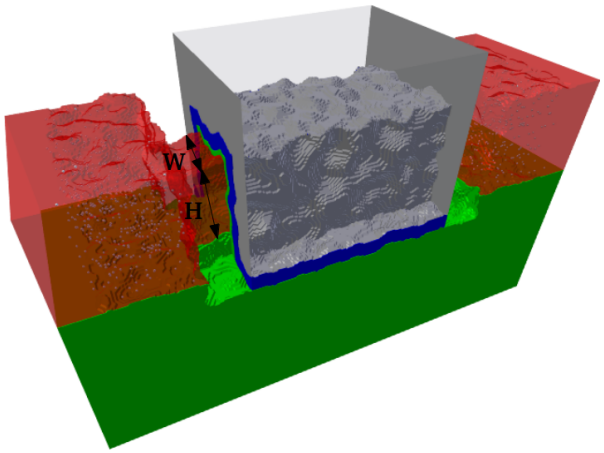

Fig. 1. A $W = 10 \times H = 10$ nm Trigate device, with overgrown source and drain contacts. Silicon is in red, SiO_2 in green, HfO_2 in blue and the gate in gray. The dots in the contacts are single dopant impurities. The spacers are 6 nm long.

II. Simulation methodology and devices

The channel is a rectangular [110] oriented silicon nanowire with width W and height H in the 4 to 24 nm range, etched in a (001) SOI layer [9]. It is lying on a 25 nm thick buried oxide (BOX) and a n-doped Si substrate (donor concentration $N_d = 10^{18}$ cm^{-3}). The gate stack is made of 0.8 nm of SiO_2 and 2.2 nm of HfO_2. The gate is separated from the bulk source and drain contacts by 6 nm long Si_3N_4 spacer regions (see Fig. 1). Point-like dopants are added to the source and drain according to the different target distributions plotted in Fig. 2, in order to capture impurity scattering in these regions. Surface roughness, Remote Coulomb Scattering (RCS) in the channel, and electron-phonon interactions are also included in

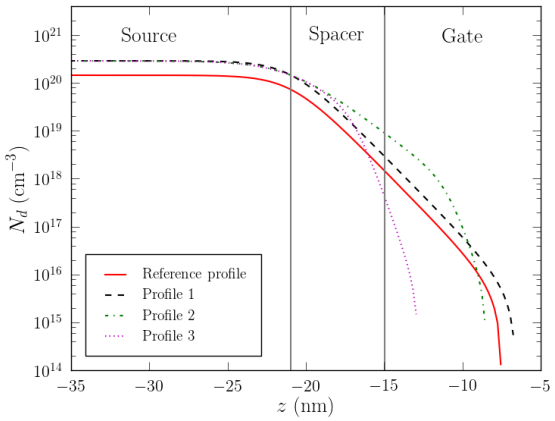

Fig. 2. Target doping profiles in the source of Fig. 1 (doping profiles are symmetric in the drain), used to generate random dopants distributions.

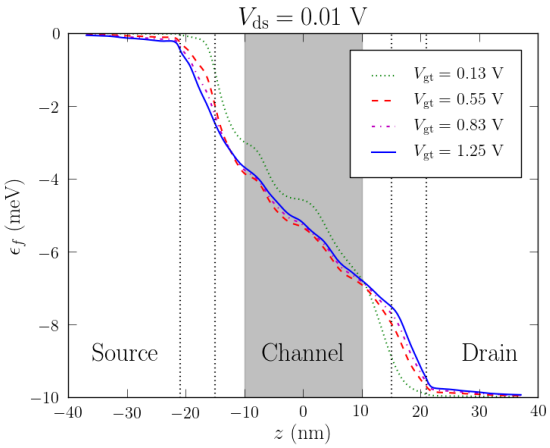

Fig. 3. Quasi-Fermi level in a 30 nm long device (Fig. 1 with the reference doping profile of Fig. 2), at different gate overdrives, with $V_{ds} = 10$ mV.

the simulations [10]. The current is computed with a NEGF code in the effective mass approximation.

III. Contact Resistance Extraction and Quasi-Fermi Level Analysis

In the low drain bias regime, the resistance $R(L)$ of the devices is linear with L in the 20-100 nm range and can therefore be extrapolated to $L = 0$ to obtain the contact resistance R_c. We use the methodology detailed in [11] to extract R_c with limited noise on sets of devices with $L = 30$, 60 and 90 nm.

The physical origin of the contact resistance is further investigated with quasi-Fermi level analysis, which highlights where the potential drops in the system. In the low field limit, the local distribution function remains close to a Fermi-Dirac equilibrium function. We can define the quasi-Fermi level $\epsilon_f(z)$ as the chemical potential that reproduces the NEGF density:

$$n_{1\mathrm{d}}(z) = \int dE\ D_{1\mathrm{d}}(z,E) f([E - \epsilon(z)]/kT) \qquad (1)$$

With $f(x) = 1/(1+e^x)$ the reduced Fermi function, $n_{1\mathrm{d}}(z)$ $D_{1\mathrm{d}}(z,E)$ the NEGF carrier density and density of states per unit length. The quasi-Fermi level is plotted in Fig. 3 for a 10×10 nm Trigate with gate length $L = 30$ nm, at different gate overdrives. The potential drop is almost negligible in the highly-doped region source and drain regions and shows much higher steps under the spacers. These regions are thus major contributors to the contact resistance, due to the lack of electrostatic control of the gate on these parts of the device. It is interesting to note that the regions under the source and drain spacers exhibit equal drops, which means that the source and drain contact resistances are symmetric at low field.

Another point of interest is that the quasi Fermi level is almost linear under the gate (gray region in Fig. 3), which indicates that the transport remains diffusive in the channel. The mobility extracted from the slope of the quasi Fermi level is very close to the one extracted from the slope of $R(L)$.

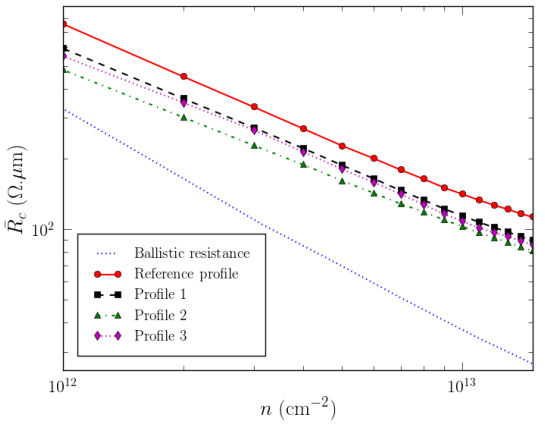

Fig. 4. The contact resistance $\bar{R}_c = R_c(W + 2H)$ as a function of the carrier density n in the channel for the different doping profiles of Fig. 2.

Hence the concept of mobility remains valid in a 30 nm long channel [12].

IV. Influence of Technological Parameters

A. Doping profile

Devices with different realistic doping profiles from small underlap to overlap (Fig. 2) have been studied and their different contact resistances are plotted in Fig. 4. Slower decay of the doping profile under the spacers slightly decreases the contact resistance because it increases the carrier density under the spacers.

B. Channel cross-sections

The contact resistances for different nanowires with $W = H$ cross-sections are plotted in Fig. 5. The contact resistances are roughly proportional to the cross sectional area $S = WH$. This results from the fact that under the spacers doping and poor electrostatic control by the gate lead to volume accumulation, as opposed to surface inversion in the channel, where the resistance is basically proportional to $W_{\mathrm{eff}} = W + 2H$. In

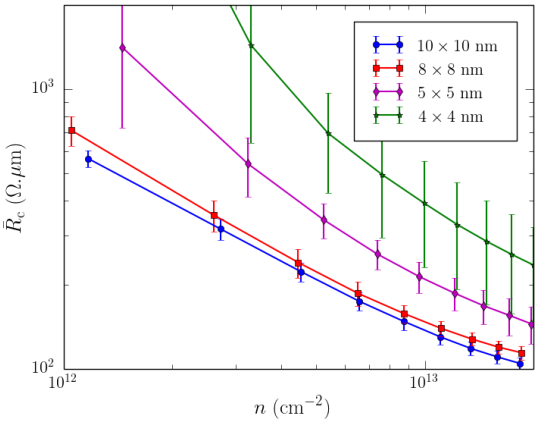

Fig. 5. The contact resistance $\bar{R}_c$ as a function of n for different nanowire devices with square cross-sections ($W = H$), with the "Reference" doping profile of Fig. 2. The bars correspond to the standard deviation computed on eight different samples.

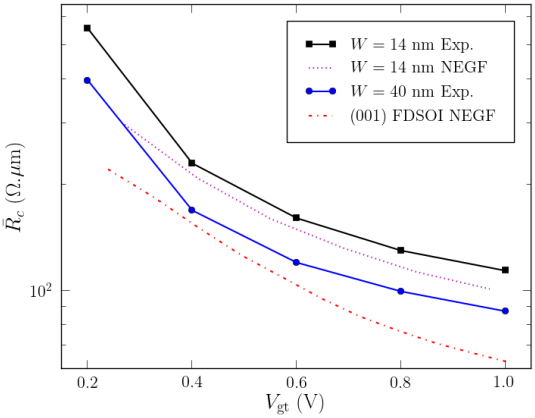

Fig. 7. Measured contact resistance in $W = 40 \times H = 12$ nm and $W = 14 \times H = 12$ nm Trigate devices, as a function of gate overdrive. They are compared with simulations for a planar (001), 12 nm thick FDSOI device and for a $W = 14 \times H = 12$ nm Trigate device.

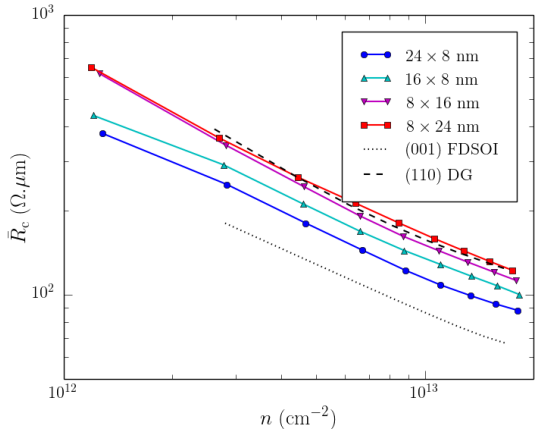

Fig. 6. The contact resistance $\bar{R}_c$ as a function of n for different nanowire cross-sections $W \times H$. The doping profile is the "Reference" profile of Fig. 2. The data are compared with the reference (001) FDSOI device ($H = 8$ nm, $W \to \infty$) and (110) double gate (DG) device ($H \to \infty$, $W = 8$ nm).

order to assess local variability, the standard deviation has been computed on a set of 8 samples. The variability increases a lot with decreasing S, because the relative fluctuations on the number of dopants under the spacers are more important for small wires.

The contact resistances of nanowires with different rectangular cross-sections are plotted in Fig. 6. The contact resistance of devices with $H >> W$ tend to the contact resistance of the symmetric double gate devices, while for devices with $W >> H$ they tend to the contact resistance of the planar FDSOI devices.

V. Comparison with experimental data

The simulations are compared with experimental data on two set of Trigate devices fabricated at CEA/LETI [13], a set of $W = 40 \times H = 12$ nm devices and the other with $W = 14 \times H = 12$ nm, both featuring 9 nm thick spacers. The contact resistances are extracted from experimental data with the same $R(L)$ method as in the simulations in the $L = 50 - 200$ nm range. The experimental contact resistances are compared in Fig. 7 to simulations performed for these specific devices. The experimental data and the simulations show similar $1/V_{gt}^{\beta}$ dependence. For the $W = 14$ nm device the comparison between experiments and simulations is quantitatively good, given that the simulations miss the metal/semiconductor contact resistance, which is supposed to appear as a small rigid shift. Experimental contact resistances for the $W = 40$ nm device lie, as expected, between the simulations for the $W = 14$ nm devices and for the planar devices.

VI. High field contact resistances

At high V_{ds} the device is driven out of equilibrium, and non linear effects appear due to the presence of carriers with high kinetic energy in the channel. As illustrated Fig. 8, these hot carriers make the principal contribution to the current and relax very slowly by emission of optical phonons. In this regime, quasi-equilibrium concepts like the quasi-Fermi level are not valid, because the distribution function is not close to a Fermi-Dirac function. Also, the resistance is not linear with respect to the gate length, so that we cannot use the $R(L)$ method any more to extract the contact resistance. The description of the method used to calculate the high-field contact resistance and its justification are beyond the scope of this paper and will be discussed elsewhere. We give some preliminary results to picture the physics of the contact resistances at high field.

In this study NEGF calculations were performed on $W = 10 \times H = 10$ nm Trigate devices with 20 nm gate length. The contributions of scattering by phonons and discrete impurities in the source and drain were computed at low field and are plotted Fig. 9. They were then extracted on the same device at $V_{ds} = 0.8$ V and the results are plotted Fig. 10 for comparison. The contact resistances on the drain side increases a lot with

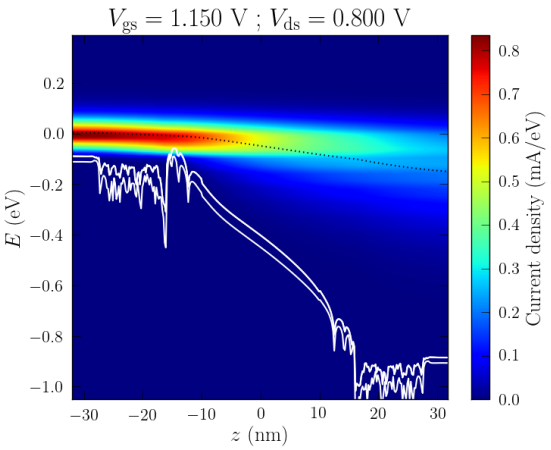

Fig. 8. Spectral density of current along the nanowire axis at $V_{ds} = 0.8$ V and in strong inversion for a $W = 10 \times H = 10$ nm Trigate device with 20 nm gate length. The red lines are the conduction band profiles of the X, Y, and Z valleys. The dotted line is the average energy of carriers which contribute to the current.

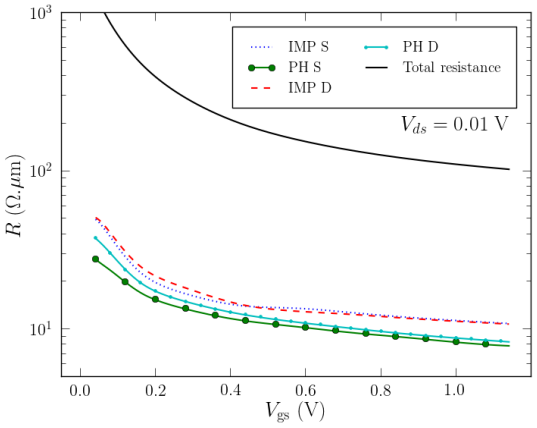

Fig. 9. Contributions of scattering by phonons (PH) and by impurities (IMP) in the source (S) and drain (D) to the total resistance at $V_{ds} = 0.01$ V in a $W = 10 \times H = 10$ nm Trigate device with 20 nm gate length. The total resistance includes the channel resistance.

the electric field, so that the source and drain contributions are not symmetric anymore at high field [14]. The drain side is hence the major contributor to the contact resistance at high field, due to both impurities and phonons scattering, the latter being the main limiting mechanism in the high inversion regime.

VII. Conclusion

The contact resistances R_c of Trigate and FinFET devices have been computed with Non-Equilibrium Green's Functions. At low drain bias, the impact of doping and channel cross-section on R_c highlights the importance of the design of the source/drain. Indeed, the region under the spacers can be a very resistive part in sub-30 nm devices, due to the poor electrostatic control over these areas. Finally, we have deembedded the different contributions (phonons, surface roughness and

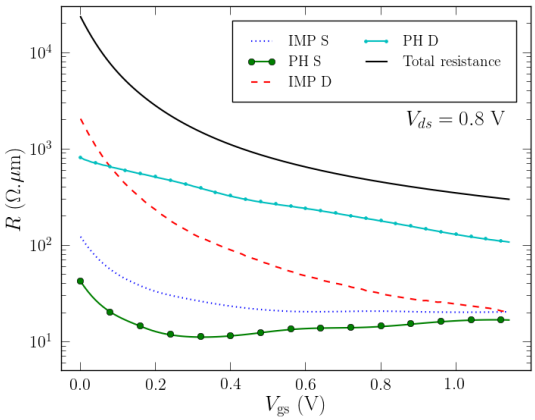

Fig. 10. Contributions of scattering by phonons (PH) and by impurities (IMP) in the source (S) and drain (D) to the total resistance at $V_{ds} = 0.8$ V in a $W = 10 \times H = 10$ nm Trigate device with 20 nm gate length. The total resistance includes the channel resistance.

impurity scattering) to the contact resistance at low and high drain bias. Whereas at low field the source and drain contacts play symmetric roles, it is not the case at high field. The drain side indeed makes the largest contribution to the resistance due to the strong enhancement of electron-phonon scattering.

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