Process Variability for Devices at and beyond the 7 nm Node

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Advanced CMOS devices are increasingly affected by various kinds of process variations. Whereas the impact of statistical process variations such as Random Dopant Fluctuations has for several years been discussed in numerous publications, the effect of systematic process variations which result from non-idealities of the equipment used or from various layout issues has got much less attention. Therefore, in the first part of this paper, an overview of the sources of process variability is given. In order to assess and minimize the impact of variations on device and circuit performance, relevant systematic and statistical variations must be simulated in parallel, from equipment through process to device and circuit level. Correlations must be traced from their source to the final result. In this paper the approach implemented in the cooperative European project SUPERAID7 to reach these goals is presented.

Introduction

A key problem for the fabrication and performance of semiconductor devices is that variations of the device feature sizes and of the dopant distributions do not scale in the same way as their nominal values. Already from simple statistics it is known that for a statistical quantity which scales for small a number N of particles in proportion to N, then the relative variation of that quantity scales in proportion to $1/\sqrt{N}$. For example in case of a threshold voltage adjustment implant with a dose of $5 \cdot 10^{11}$ cm^{-2}, at average 2 ions are implanted into a transistor channel of 20 nm length and width. With ion implantation being a statistical process this means that the actual number of ions implanted into the transistor channel will differ from device to device, in that case critically affecting threshold voltage and other electrical parameters. This is the simplest example for statistical process variations which result from the granularity of matter for aggressively scaled devices, and was one of the key reasons which ruled out bulk transistors with doped channels for advanced technology nodes. Statistical process variations such as these Random Dopant Fluctuations have been discussed for several years in numerous publications, e.g. (1) (2). Additionally, non-idealities of the equipment used in semiconductor processing and also layout effects cause systematic variations of the device geometry or the dopant profiles. In turn, aggressively scaled transistors are subject to various kinds of variations. It is important to know if (systematic) variations of different transistors are caused by the same source, because in this case such variations would correlate, which is important for the

1

impact on circuit behavior. Moreover, rather similar problems exist for interconnects and must also be considered for the assessment and optimization of circuit behavior.

In this paper first a very short overview of the sources of variations is given, especially with regard to advanced devices and interconnects at the 7 nm node and beyond. Then, the hierarchical simulation system being developed in the cooperative European project SUPERAID7 (3) is presented, especially regarding aspects critical for advanced three-dimensional devices. Examples simulated are presented to illustrate the impact of variations.

Sources of Process Variations

Sources of statistical and systematic process variations were discussed earlier in some detail e.g. in (4). In the following, a short overview is given, and some effects especially important for the 7 nm node and below are discussed.

<u>Statistical Variations</u>

Important statistical variations frequently discussed in the literature, e.g. in (1) and (5), respectively, are Random Dopant Fluctuations (RDF), Metal Grain Granularity (MGG), and Line Edge Roughness (LER), as illustrated in Figure 1. MGG and LER must also be considered for interconnects, as illustrated in Figure 2. It is important to note that since these variations are of purely statistical nature their effects on transistors or interconnects do not correlate with each other or with any of the systematic variations mentioned below, unless two neighboring structures would both be affected by the roughness of the same line or the same metal grain.
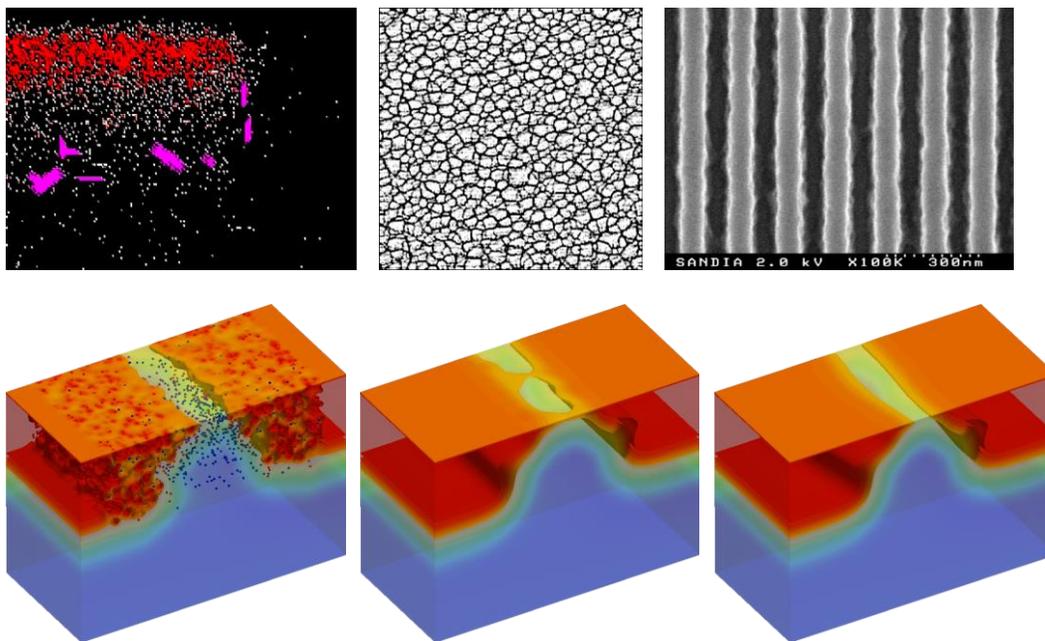
Figure 1. Example for stochastic process variations in a CMOS transistor. From left to right: Random Dopant Fluctuations (RDF), Metal Grain Granularity (MGG), and Line Edge Roughness (LER) for statistical process variations (from Univ. Glasgow).

2
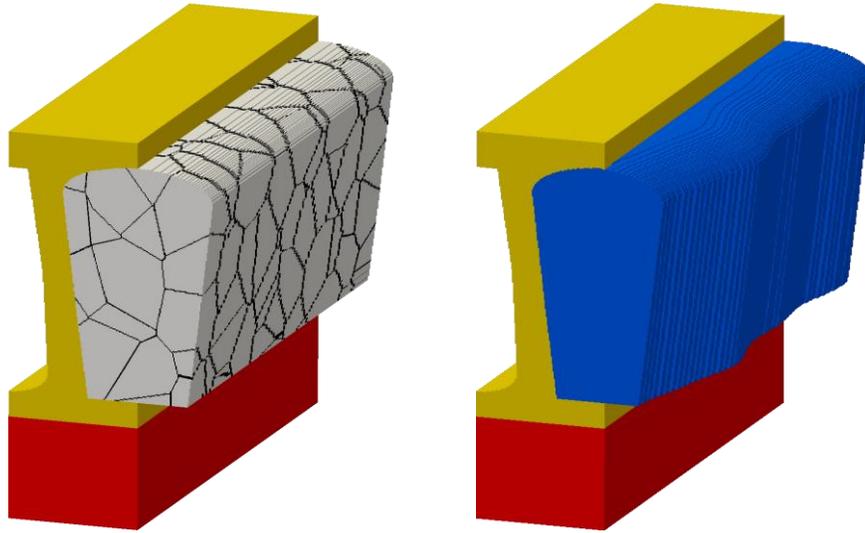
Figure 2. Example for stochastic process variations in an interconnect structure. Left: Copper granularity which can introduce resistance variations in short range interconnects; right: LER which can introduce resistance variations in short range interconnects (from Synopsys).

<u>Systematic Variations</u>

Systematic variations are caused by non-idealities of process equipment, by pattern or by layout effects, as outlined earlier (4). One of the most critical effects is the variation of the focus position (distance between the last lense or last mirror and the photoresist) and of the illumination dose in lithography steps, which among others cause variations of the feature sizes printed in the photoresist, the so-called "critical dimensions" CD, see Figure 3 (left). E.g. for focus variations of ±20 nm, which is not much for a mechanical system, the CD printed in the photoresist changes by up to some nm. The assessment and optimization of the acceptable range of focus and dose, their so-called "process window", is an integral part of the development of advanced equipment and processes for lithography, both optical and Extreme Ultraviolet (EUV). It is important to note that even symmetric distributions of focus and dose lead due to simple physical reasons to highly asymmetric distributions of the CD (6). As illustrated in that reference both a process step and a device architecture may also act as a filter, converting a symmetric distribution of a variation into an asymmetric one, or vice versa: Whereas the simulations for a bulk CMOS transistor with pockets resulted in a nearly normal Gaussian distribution of the threshold voltage, for FDSOI NMOS a highly asymmetric distribution of the threshold voltage similar to that of the CD was predicted.

For devices at and beyond the 7 nm node, as addressed in the SUPERAID7 project and in this paper, either EUV or Multiple Patterning lithography is applied. In case of Multiple Patterning an additional complication arises because either one original mask level is broken up into two (or four in case of Quadruple Patterning) incremental mask levels, each of them with variations which do not correlate with each other (7), or in case of Self Aligned Double Patterning significant differences arise for inner and outer lines, as discussed below. This has significant impact on circuit design.
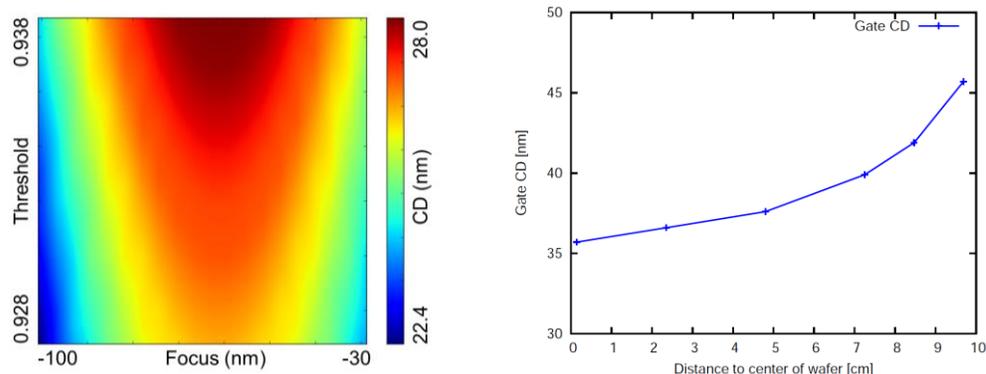
Figure 3. Examples for equipment-induced systematic process variations. Left: Simulated variation of the feature sizes ("critical dimension" CD, displayed as color code) created in the photoresist during optical lithography, caused by variations in focus and illumination dose. Qualitative and quantitative results depend on details of the equipment, mask, photoresist and process employed; right: Simulated dependence of the gate CD value on the position on the wafer for an exemplary etching process employing an inductively coupled plasma (ICP) reactor (from IISB).

The main variations in Self Aligned Double Patterning result from the spacer deposition and etching processes employed (8). As discussed earlier (4), deposition and etching steps are subject to a large number of variations which are specific for the process in question and which result e.g. from inhomogeneities in the spatial distribution of ions and neutrals in the plasma, gas flow, temperature and pressure distributions, spatial variations of target erosion, or pattern effects. They can generally be addressed by suitable equipment simulation programs which calculate mesoscopic parameters like etching and deposition rates depending on position on the wafer and other quantities, which are then used in feature-scale topography simulators. In Figure 3 (right) an example of the dependence of the (gate) CD on the position on the wafer is shown.

Compared with lithography and other topography steps, implantation and annealing steps are less affected by systematic process variations. Here, especially the impact of patterns on the reflectivity of the wafer and non-reproducibility of temperature profiles in Flash and Spike Annealing processes are important. Moreover process-induced and pattern dependent stress affects carrier mobility.

Hierarchical Simulation of the Impact of Process Variations

Advanced CMOS devices at and beyond the 7 nm node generally employ a three-dimensional structure to enable better control and switching behavior. Figure 4 shows examples which are being addressed in the benchmark work carried out as part of the SUPERAID7 project. Concluding from earlier results on fully depleted FinFETs the size, shape and orientation of the surfaces of the channel area is especially critical for the drive current, whereas the distance of the central part of the volume from the gate electrodes is especially important for the leakage current. In turn, for the simulation of such devices it is mandatory to well predict the device geometry and its process-induced variations. The simulation sequence must in principle start from equipment simulation, followed by (feature scale) process and device simulation, and finally enable circuit simulation via the

extraction of appropriate compact models. Relevant process variations must be introduced into this sequence whenever they occur, and their impact be traced through all following process steps and stages of the simulation. All simulation modules must be capable to well describe the variations newly introduced at that process step or stage of simulation. This is illustrated in Figure 5 by naming the modules "Statistical ….". Moreover, in many cases they must be executed repeatedly in order to trace the impact of the variations which resulted from earlier process steps or earlier stages of the simulation. The impact of stochastic variations like RDD, MGG or LER can be simulated in parallel via a suitable set of device simulations. In contrast to this, for the treatment of correlations caused by systematic variations it is mandatory to store within the simulation sequence the value of the varying process parameters (e.g. the focus in a lithography step) together with the results of all the subsequent simulation steps. In turn, the result of the hierarchical variability simulation must consist of a data set where all the systematic variation sources considered are the independent variables, and the final simulation results are stored for all values of these independent parameters. This approach was discussed in more detail earlier (4).
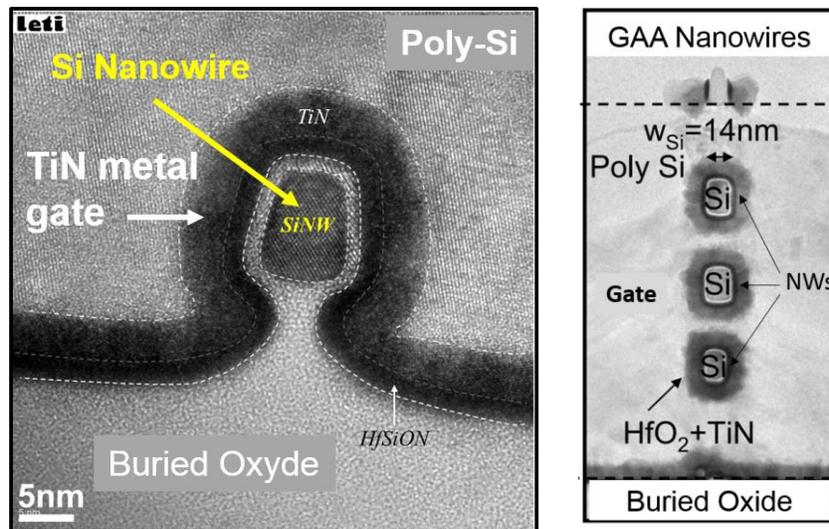
Figure 4. Examples for device architectures used in the SUPERAID7 benchmarks: (a) ΩGate nanowire transistor (9); (b) stacked Gate-All-Around nanowires (10) (from CEA/Leti).

Obviously, a brute-force implementation of this approach is not possible, because the effort would scale with the product of the instances of all varying parameters considered. E.g. assuming that ten sources of process variations would need to be dealt with, and each of them would be discretized by just 5 values, then $5^{10} = 9765625$ full simulation runs would need to be carried out just for the systematic variations. Therefore it is mandatory to drastically reduce this set of simulations, by identifying the most relevant sources of variations upfront and then employing suitable design-of-experiment techniques. Moreover, it is essential to implement a proper interface between the process simulation runs needed to trace the impact of the systematical (equipment and layout) variations on device geometry and doping and the device level simulation of the stochastic variations like RDD, MGG or LER: It is in no way possible to perform a simulation split at device level for each result of the process simulation split. This problem is being handled at the level of compact models, as discussed below.

5
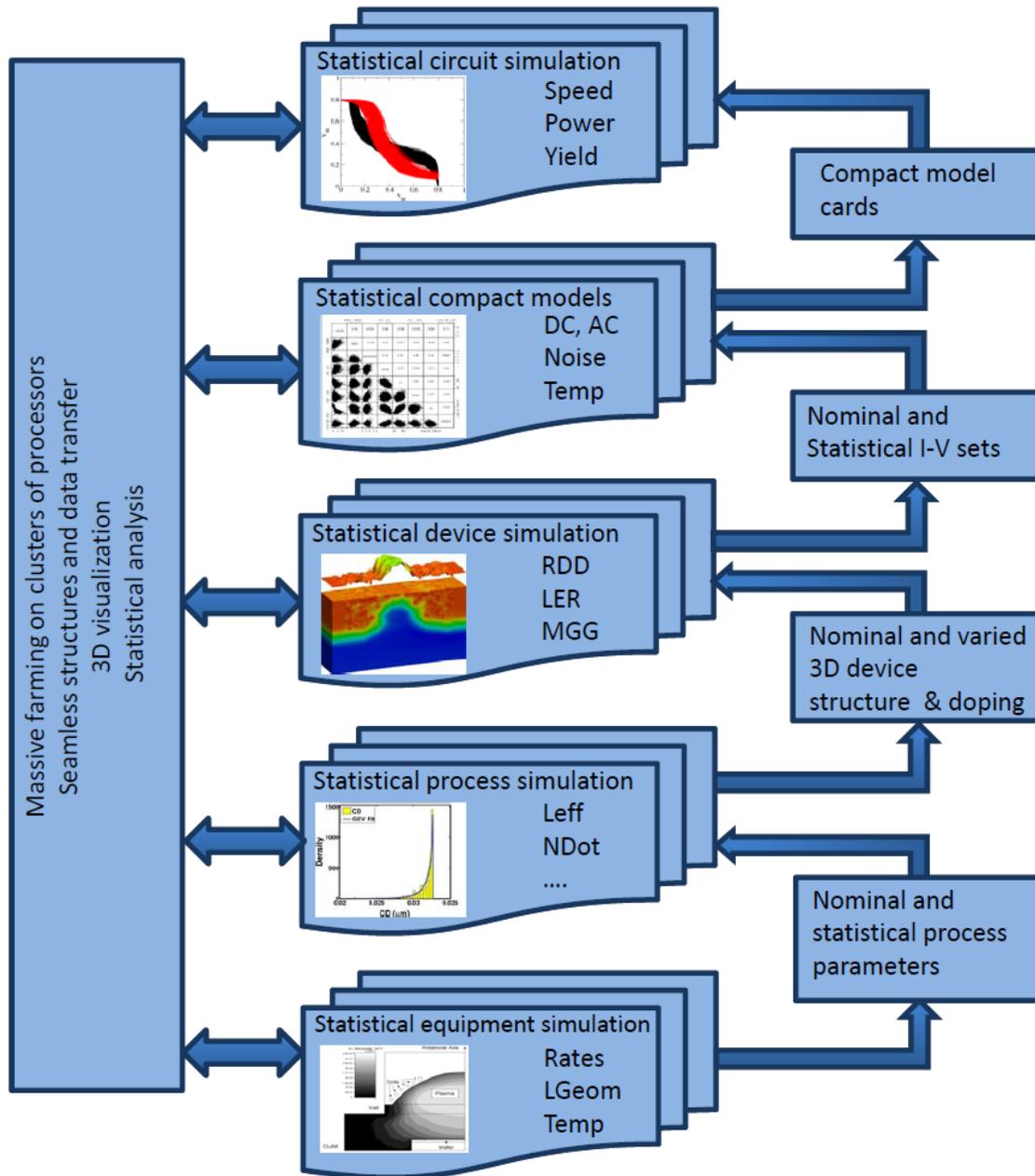
Figure 5. Impacts of variations to be considered at various levels of simulation.

Process Simulation of Systematic Variations

As discussed above, most systematic variations result from non-idealities of a certain piece of process equipment, and can be described by appropriate equipment simulation programs. However, except for lithography, where it is not possible to separate between equipment and process simulation, it is not appropriate to directly integrate equipment simulation into the overall simulation software. Rather, parameters such as etching rates depending on angle of incidence and position on the wafer are first extracted from equipment simulation and then used as input for feature scale process simulation. This also enables the treatment of equipment-based variations in feature scale process simulation.

In lithography simulation usually the equipment level (illumination source, mask, imaging system) and the wafer level (photoresist and layers / geometries below) are considered together, solving in some way Maxwells' equations to calculate the energy deposited in the photoresist. Together with subsequent simulations of resist exposure this also allows to rigorously treat the impact of all process variations caused by lithography, see the numerous publications in this field, for example (11) and (12).

The accurate simulation of geometries and their variations, which is necessary for three-dimensional devices as shown in Figure 4, requires the intimate coupling between feature-scale simulations for all lithography, deposition and etching steps involved. In turn, the development of an integrated topography simulator is one of the core activities of the SUPERAID7 project. Background tools from IISB and TU Wien for the simulation of lithography (Dr.LiTHO (13)), etching and deposition have been closely integrated, and new models for specific etching and deposition steps have been implemented. Figure 6 gives an example for the influence of the photoresist shape, which resulted from lithography, on the structure etched into the underlying layer. Simply starting from the resist footprint would lead to erroneous results. Current multi patterning steps are considerably affected by variations in the lithography, etching and deposition steps used, with their propagation strongly depending on details of processing, device and circuit architecture, and circuit layout. In Litho-Etch-Litho-Etch and Litho-Freeze-Litho-Etch double patterning, where a mask level is broken down into two mask levels each with twice the pitch, the results of the second incremental lithography step depend on the resists modifications caused by the first incremental step, and due to the split up of the mask the variations introduced in both incremental steps do not correlate with each other (7). In Self Aligned Double patterning (SADP) as used for the generation of fins, first a lithography step is used to structure a carbon hard mask. Subsequently, spacers are deposited and etched back, and then the hard mask is removed. In turn, two mask lines are generated instead of one, and their width mainly depends on the deposition process employed. This sequence is rather insensitive to usual variations of the CDs generated in the lithography step (8). However, the nominal widths of the final mask lines generated, the difference between outer and inner lines and their process variability strongly depend on the etching and deposition processes employed, as illustrated in Figure 7. Among others, differences in the open view angles frequently cause different widths of inner and outer lines.

Development of models or software for ion implantation and diffusion/annealing has not been foreseen within SUPERAID7. Instead, these steps have been simulated with the well established Sentaurus Process tool (14), especially because except for RDF (and pattern effects) no variations resulting from these processes have to be considered.
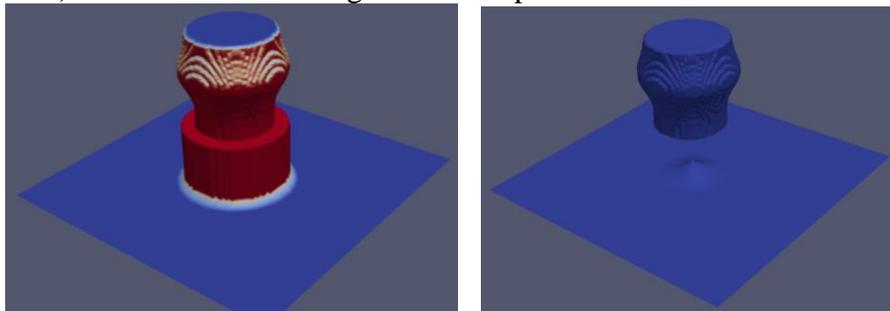
Figure 6. Example for integrated topography simulation (lithography and etching): Influence of real resist shape on directional (left) and isotropic (right) etch process (from IISB).
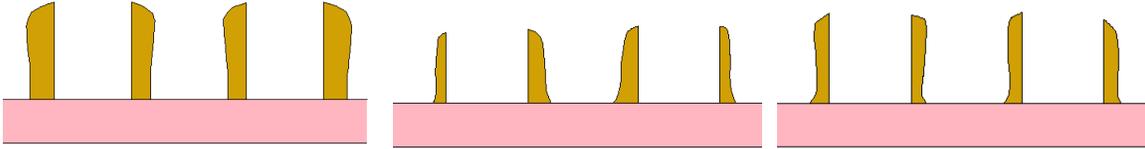
Figure 7. Example for cross-section of fin pattern generated by SADP. Left: Non-conformal deposition followed by perfectly anisotropic etching; middle: Conformal deposition followed by chemical dry etching; right: Non-conformal deposition followed by chemical dry etching (from IISB).

Variability-Aware Device and Interconnect Simulation

In the simulation flow illustrated in Figure 5, the device structures fabricated are simulated with the variability-aware device simulator GARAND (15). In order to meet the requirements of very small device cross sections and variations such as surface roughness, several improved physical models for confined carrier transport in nanowires are being developed at CEA/Leti, Glasgow University, Synopsys and TU Wien. Figure 8 shows the results of quantum mechanical calculations of the electron dynamics in presence of surface potential variations caused by surface roughness, using the so-called Wigner approach. After 400 fs evolution, the systems reach stationary states. High productivity drift-diffusion simulations employing GARAND are required to enable the large number of device simulation runs needed to investigate the impact of statistical variability, such as RDF and surface roughness. Corrections to the drift diffusion approach used are extracted from more sophisticated device modeling work, and implemented as enhancements of GARAND.
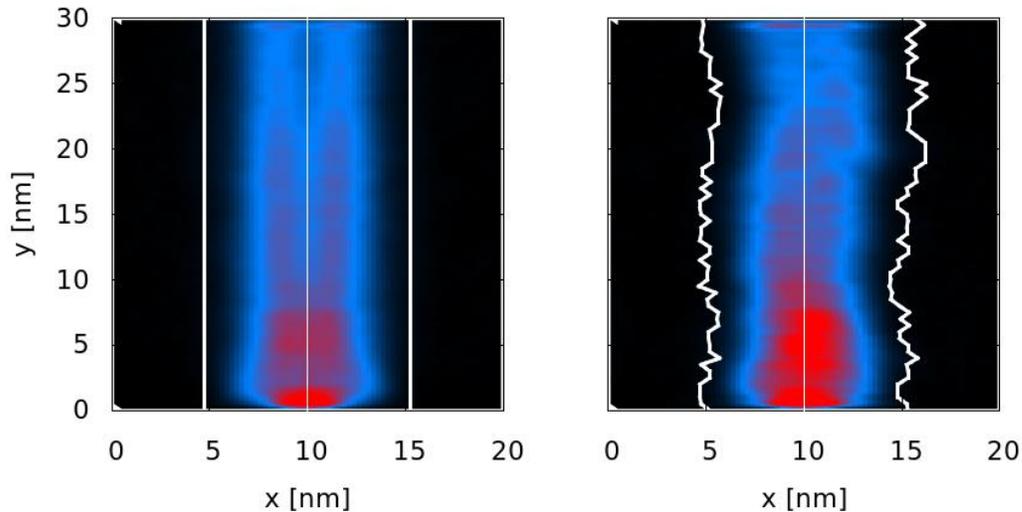
Figure 8. Electron density in ideal (left) and rough (right) wires. Quantum repulsion keeps the density away from the boundaries (from TU Wien).

Additionally, an interconnect simulator prototype has been developed for use in the SUPERAID7 project in order to study the interplay between global process-induced variability and local statistical variability in advanced interconnects suitable for 10 nm CMOS technology and below including the use of air-gaps. The simulator handles the simulation of capacitances and resistance variations of the complex interconnect configurations occurring in the first three layers of interconnects, which are greatly impacted by

8

global process variability and by local statistical variability. Effects of metal granularity and wire scaling have been included. Scattering models have been implemented which allow one to capture electron transport in scaled interconnects in the presence of metal granularity. Basic compact models for RC equivalent circuits have been extracted and made available in a format compatible with SPICE-like simulators. Figure 9 shows an example interconnect structure for a 14 nm FinFET based double inverter used as a testbed, namely a sample metal grain granularity (left) and the electric field streamlines calculated (right).
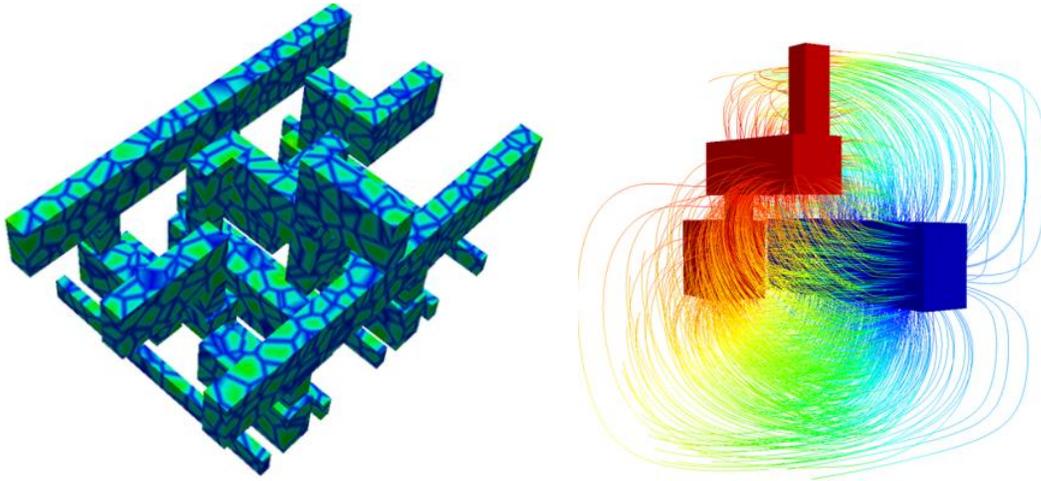
Figure 9. Interconnect structure for the 14nm FinFET-based double inverter used as test-bed. The impact of statistical variability is highlighted in the form of Metal Line Granularity left). The electric field streamlines between two wires, as obtained by 3D simulation are also shown (right) (from Synopsys).

Variability-Aware Compact Modeling

The development of variability-aware compact models for three-dimensional devices as illustrated in Figure 4 has included three main tasks: First, suitable compact models have been developed for such transistors. Second, as mentioned above interconnect compact models have been extracted for RC equivalent circuits. Third, a methodology has been developed to extend the compact models to include the impact of the process variations addressed.

Nominal Compact Models for Three-dimensional Transistors

Due to the inherent limitations of compact models available at the beginning of the SUPERAID7 project, a new compact model suitable for nanowires has been developed at CEA/Leti. This new model named Leti-NSP is a surface-potential-based model dedicated to advanced CMOS technologies based on 3D device architectures, and now allows for the simulation of FinFETs, trigate MOSFETs and also vertically nanowire/nanosheet MOSFETs with an excellent accuracy. All development steps have been validated using several numerical simulations and experimental data. In Leti-NSP, quantum confinement effects are considered via a correction of the oxide capacitance accounting for the effect of carrier effective mass on the charge centroid position and with a classical correction of the flatband voltage. In order to validate quantum confinement effects, the software TB

SIM (16) has been used to solve the Poisson-Schrödinger equations in GAA nanosheet MOSFETs. An example for this validation is shown in Figure 10. The model has among others been presented at IEDM 2016 (17).
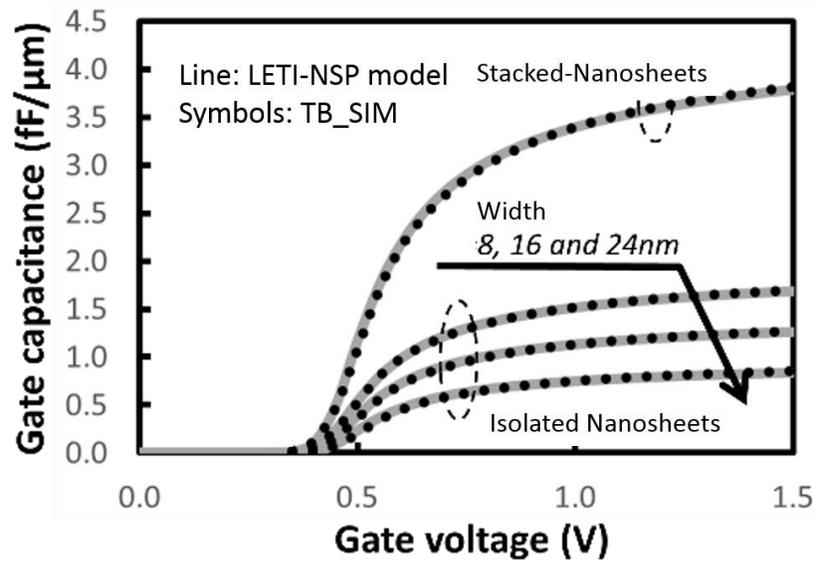
Figure 10. Gate capacitance vs. gate voltage of single and stacked GAA nanosheet MOSFET with several values of width W for the validation of quantum confinement correction (from CEA/Leti).
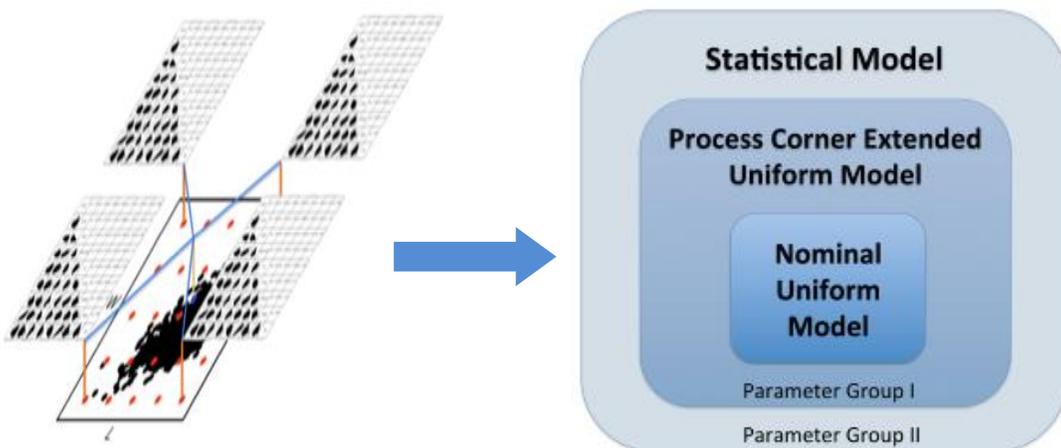
Figure 11. Hierarchical variability-aware compact modelling extraction and generation. (from GSS/Synopsys)

Compact Model Extensions to Include Process Variations

   To complete the hierarchical simulation approach presented, the variability-aware compact modeling approach presented earlier (18) has been used and adapted at Synopsys to utilize the other simulation steps mentioned above. The extraction strategy illustrated in Figure 11 consists of three steps: First, a comprehensive compact model is extracted for the nominal device. Second, a response surface process variation model using a minimum set of parameters is extracted to describe the dependence of parameters which define the device, including gate length and width, on the systematic process variations

considered. This extraction is based on the results of the TCAD process simulations carried out. Third, the statistical compact model is extracted using corresponding process corners and a second, different set of model parameters.

Finally, using this hierarchical compact model extraction approach together with LETI-NSP (17) both the device without variations ("uniform device") and the impact of several kinds of variations can be described. Fig. 12 shows the $I_D V_G$ characteristics of a statistical ensemble of 100 nMOS devices.
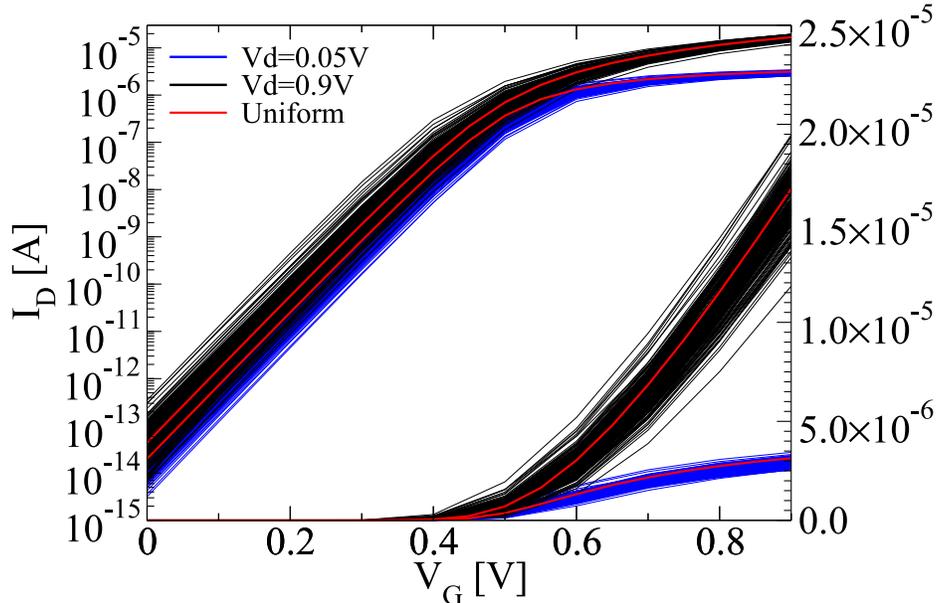
Figure 12. I_D-V_G characteristics of a statistical ensemble of 100 nMOS devices. The red line is uniform device I_D-V_G characteristics (from Synopsys).

Outlook

Further model and software improvements of the integrated three dimensional topography simulator and the variation-aware device simulator are on the way. The compact model extraction approach is being further extended, among others with respect to process-induced variations of the device geometries which cannot be described by a few simple physical parameters, such as channel length and nanowire width. The overall software system is being benchmarked against experimental data of the project partner CEA/Leti.

Conclusions

Hierarchical variability-aware simulation spanning from equipment through process and device to circuit level is needed to assess and minimize the impact of systematical and statistical process variations on circuits and devices. Especially for highly three-dimensional devices the impact of equipment-induced variations on device topography and performance must be included.

Acknowledgments

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