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SUPERAID7

Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7nm Node

D1.11: Variability simulation within SUPERAID7, impact of process variations to advanced More Moore devices and circuits

	Name	Organisation	Date
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Contents

Abstract

The results obtained in the SUPERAID7 project have been disseminated in a large number of Open Access publications. Rather than selecting some of them and to some extent duplicating already freely available information, in this deliverable the individual publications from SUPERAID7 are positioned within the scope of the project and put into perspective with each other. In this way it is intended to give a very good overview of the overall results obtained and to efficiently guide the reader to those papers which address topics he is especially interested in. In view of the wide scope of the SUPERAID7 project which ranges from equipment to circuit simulation, the document is structured according to the simulation level which is primarily addressed by the paper in question.

1. Introduction

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled More Moore, process variability has got ever more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data.

Within the SUPERAID7 project a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits down to the 7 nm node and below has been established, including interconnects. The tool combines commercial software from Synopsys and GSS (which is since May 2016 part of Synopsys) with tools from all project partners, largely improved within the project. This has needed improved physical models and new compact models, suitable for the device architectures addressed and able to include the process variations to be considered. Device architectures addressed include especially TriGate/ΩGate FETs and stacked nanowires. The software developed has been benchmarked utilizing background and sideground experiments of the partner CEA/Leti.

Whereas the project results are being exploited internally at the project partners, via further research projects and especially via the SUPERAID7 partner Synopsys, dissemination of the project result to the scientific community and to potential users in industry is also very important, especially for the universities and research institutes involved in the project. In consequence, a large number of publications were made at leading international conferences and in important scientific journals. Preference was given to publications paths which provide Gold Open Access. Other publications have been made available via Green Open Access.

In this public deliverable, the individual publications from SUPERAID7 are positioned within the scope of the project and put into perspective with each other. In this way it is intended to give a very good overview of the overall results obtained and to efficiently guide the reader to those papers which address topics he is especially interested in.

2. SUPERAID7 Papers Positioned Within the Scope of the Project

In the following, the papers published from SUPERAID7 are listed, linked to the simulation level they refer to, from equipment/process simulation to compact models and related benchmarks. For each paper its scope and position within the project is summarized, partly using or revising the abstract published in the paper.

Among others, a considerable part of the SUPERAID7 papers has been published in the SISPAD conference series: On one hand side, this is the most important conference series worldwide dedicated to TCAD, and therefore provides an excellent forum for the presentation and discussion of results from SUPERAID7. On the other hand side, the proceedings of the SISPAD conference are available in Gold Open Access via www.sispad.info. Some other conferences like IEDM, and some of the most important journals like the IEEE Transactions on Electron Devices do not provide Gold Open Access, and therefore limit open publication to Green Open Access, as implemented for those papers in SUPERAID7.

2.1 Equipment/Process Simulation

The simulation of process equipment and process flows is a key objective of the SUPERAID7 project, because systematic variations such as focus and dose variations in lithography have their source at equipment level. Therefore, first equipment simulation must be employed to calculate the impact of variations of equipment setting or of the position in a process equipment – or on a wafer – on the results of the process step for which the equipment is being used. Afterwards, the impacts of these variations of process results must be traced throughout the whole remaining process flow, until finally the resulting variation of the geometry, dopant distribution or other quantities which define the device are known. It is important to state that throughout the process flow further source of variations may come into play, resulting in devices which are affected by several different kinds of systematic variations.

Concerning equipment and process simulation, work in SUPERAID7 has focused on the improvement of tools for the simulation of deposition and etching, and on the integration of lithography, deposition and etching simulation into an overall topography simulation tool, which subsequently transfers the structures generated into the well-established Sentaurus Process tool from Synopsys. The following papers from SUPERAID7 primarily deal with these areas:

Z. Belete et al., Modeling of Block Copolymer Dry Etching for Directed Self-Assembly Lithography, Proc. of SPIE 10589 (2018) 105890U

In this paper the etching simulation tool developed in SUPERAID7 is adapted and applied to understand the etch behavior of Ps-b-PMMA, a standard material used for structure generation via Directed Self-Assembly (DSA).

X. Klemenschits et al., Unified Feature Scale Model for Etching in SF_6 and Cl Plasma Chemistries, in: Proceedings 2018 Joint International EUROSOI-ULIS Workshop

In this paper a novel unified feature-scale model for inductive plasma etching is presented, in order to enable the simulation of novel gate stacks for advanced nodes as addressed in SUPERAID7.

X. Klemenschits, S. Selberherr, L. Filipovic, Modeling of Gate Stack Patterning for Advanced Technology Nodes: A Review, Micromachines 12 (2018) 631

In this review paper the fundamental methods, used to describe topology changes in patterning processes, and their respective benefits and limitations are discussed, especially regarding the transport of molecular entities using numerical particle ray tracing. Furthermore, the modeling of surface chemistry and the modelling of gate stack patterning are discussed.

E. Baer et al., The Effect of Etching and Deposition Processes on the Width of Spacers Created during Self-Aligned Double Patterning, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 83

This paper deals with the simulation of self-aligned double patterning as used for the patterning of fins for FinFET transistors. The impact of the lithography, deposition and etching processes on the fin width and on its variation is discussed.

J.K. Lorenz et al., Process Variability for Devices at and beyond the 7 nm Node, in: Proceedings of the 18th Symposium on Advanced CMOS-Compatible Semiconductor Devices, Ed. J.A. Martino, J.P. Raskin, S. Selberherr, H. Ishii, F. Gamiz, B.Y. Nguyen, A. Yoshino, The Electrochemical Society, ECS Transactions 85-8, 2018, p. 113

This invited paper presented at the 233rd ECS Symposium gives an overview of the systematic variations which are important for highly three-dimensional devices as addressed in SUPERAID7, and demonstrates especially the simulation of structure generation for such devices. Beyond this it briefly sketches the overall hierarchical simulation flow implemented in SUPERAID7, from equipment simulation to compact model extraction.

J.K. Lorenz et al., Process Variability for Devices at and beyond the 7 nm Node, ECS J. Solid State Science Technol. 7 (2018) P595

This paper is an extension of the invited paper presented at the 233rd ECS meeting, mentioned above. The main additional result is the presentation of main elements of the simulation of the process from the second SUPERAID7 benchmark, especially the identification of the systematic variations most relevant for that process.

J. Lorenz et al., Process Variability–Technological Challenge and Design Issue for Nanoscale Devices, Micromachines 1 (2019) 6

The paper focuses on technological challenges, especially issues resulting from the structuring processes needed to generate the three-dimensional device structures for different architectures. Furthermore, the feasibility of a full simulation of the impact of relevant systematic and stochastic variations on advanced devices and circuits is demonstrated. Therefore the paper is also mentioned in the section on compact model extraction below. The paper was accepted for publication at the end of 2018, and published in the first issue of 2019.

2.2 Device Simulation

The modeling and simulation of the performance of three-dimensional nanoscale transistors raises many challenges in terms of accurate and efficient physical models, their implementation and their usage to predict and understand device behavior. For the treatment of systematic and especially of statistical variability, it is important to use very efficient models implemented in robust tools, in order to enable the conduction of the large sets of simulations required for variation studies. A well established approach is to start from efficient models such as Drift Diffusion, and to enhance them by suitable corrections based on rigorous approaches, including especially quantum mechanical effects.

In view of the complexity of the problem, all SUPERAID7 partners except for Fraunhofer IISB (which focused on the equipment/process simulation and on compact model work) made dedicated contributions to enhance models and software needed for the simulation of statistical variations of three-dimensional nanoscale devices. This has also led to a large number of Open Access publications, which are summarized below, grouped according to the time of publication.

Papers published in 2016

T. Al-Ameri et al., Impact of Strain on the Performance of Si Nanowires Transistors at the Scaling Limit: A 3D Monte Carlo / 2D Poisson Schrodinger Simulation Study, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 213

In this work the correlation between channel strain and device performance in various n-type Si-NWTs is investigated. A correlation between strain, gate length and cross-section dimension of the transistors is established. All simulations are based on a quantum mechanical description of the mobile charge distribution in the channel obtained from a 2D solution of the Schrödinger equation in multiple cross sections along the current path, which is mandatory for nanowires with such ultra-scale dimensions. The current transport along the channel is simulated using 3D Monte Carlo (MC) and drift-diffusion (DD) approaches.

L. Bourdet et al., High and Low-field Contact Resistances in Trigate Devices in a Non-Equilibrium Green´s Functions Framework, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 291

We compute the contact resistances at low drain bias in Trigate and FinFET devices with widths and heights in the 4 to 24 nm range, using a Non-Equilibrium Green's Function approach. Electron-phonon, surface roughness and Coulomb scattering are taken into account. The analysis of the quasi-Fermi level profile reveals that the areas under the spacers are major contributors to the contact resistance at low field, due to the poor electrostatic control over the carrier density under the spacers. The impact of design parameters (cross-section and doping profile) on the contact resistance is analyzed and the simulations are compared to experimental data. At high drain bias, the contributions of phonons and impurities scattering in the source and drain are also computed and discussed.

T. Sadi et al., One-Dimensional Multi-Subband Monte Carlo Simulation of Charge Transport in Si Nanowire Transistors, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 23

A newly-developed one-dimensional multi-subband Monte Carlo (1DMSMC) simulation module is employed to study electron transport in nanowire structures. The 1DMSMC simulation module is integrated into the GSS TCAD simulator GARAND coupling a MC electron trajectory simulation with a 3D Poisson–2D Schrödinger solver, and accounting for the modified acoustic phonon, optical phonon, and surface roughness scattering mechanisms. We apply the simulator to investigate the impact of various physical effects on the mobility in silicon nanowire field-effect transistors (NWTs), and emphasize the importance of using 1D models that include correctly quantum confinement and allow for a reliable prediction of the performance of NWTs at the scaling limits.

Z. Zeng et al., Size-dependent Carrier Mobilities in Rectangular Silicon Nanowire Devices, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 257

In this contribution, we perform quantum calculations of the size-dependent carrier mobilities in gate-all around rectangular SiNWs with leading dimension up to 50 nm, in the non-equilibrium Green's functions (NEGF) framework. We find that when the smallest width or height falls in the sub-10 nm range, nearest neighbor corner channels tend to merge and form "side channels" with much lower mobilities. On top of the numerical results, we have derived a simple model, which bridges square NW devices with thin film devices, and describes the size dependence of the carrier mobilities in rectangular SiNWs in a wide range of dimensions.

Z. Zeng et al., Carrier Scattering by Workfunction Fluctuations and Interface Dipoles in high-κ/Metal Gate Stacks, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 369

The introduction of a high-κ/metal gate stack in metal-oxide-Semiconductor field-effect transistors can cause a significant degradation of the mobility, especially at weak inversion densities. This degradation is commonly ascribed to remote Coulomb scattering (RCS, i.e., charges trapped at the SiO_2/HfO2 interface). However, very large densities of RCS charges are usually needed to reproduce the experimental data. In this work, we explore alternative scattering mechanisms by quantum calculations of the carrier mobilities. We consider, in particular, metal grain workfunction fluctuations and local dipoles at the SiO2/HfO2 interface. Similarly to RCS, both scattering mechanisms are found to reduce the carrier mobility significantly at low carrier densities. However, the mobility exhibits a different dependence on the thickness of high-κ layer, which provides a way to identify the dominant mechanism.

Papers published in 2017

T. Al-Ameri et al., Simulation Study of Vertically Stacked Lateral Si Nanowires Transistors for 5 nm CMOS Applications, J. Electron Dev. Soc. 5 (2017) 466

In this paper, we present a simulation study of vertically stacked lateral nanowires transistors (NWTs), which may have applications at 5-nm CMOS technology. Our simulation approach is based on a collection of simulation techniques to capture the complexity in such ultra-scaled devices. Initially, we used drift-diffusion methodology with activated Poisson–Schrodinger quantum corrections to accurately capture the quantum confinement in the cross-section of the device. Ensemble Monte Carlo simulations are used to accurately evaluate the drive current capturing the complexity of the carrier transport in the NWTs. We compared the current flow in single, double, and triple vertically stacked lateral NWTs with and without contact resistance. The results presented here suggest a consistent link between channel strain and device performance. Furthermore, we propose a device structure for the 5-nm CMOS technology node that meets the required industry scaling projection. We also consider the interplay between various sources of statistical variability and reliability in this paper.

T. Al-Ameri et al., Simulation Study of Vertically Stacked Lateral Si Nanowires Transistors for 5-nm CMOS Applications, J. Electron Dev. Soc. 5 (2017) 466

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V.P. Georgiev et al., Experimental and Simulation Study of a High Current 1D Silicon Nanowire Transistor using Heavily Doped Channels, IEEE Transactions on Nanotechnology, 16(5), 727-735 IEEE Transactions on Nanotechnology, 16(5) 2017

The experimental results from 8 nm diameter silicon nanowire junctionless field-effect transistors with gate lengths of 150 nm are presented that demonstrate on-currents

up to 1.15 mA/µm for 1.0 V and 2.52 mA/µm for 1.8 V gate overdrive with an off-current set at 100 nA/µm. On- to off-current ratios above 108 with a subthreshold slope of 66 mV/dec are demonstrated at 25 oC. Simulations using drift-diffusion which include density-gradient quantum corrections provide excellent agreement with the experimental results. The simulations demonstrate that the present silicon-dioxide gate dielectric only allows the gate to be scaled to 25 nm length before short-channel effects significantly reduce the performance. If high-K dielectrics replace some parts of the silicon dioxide then the technology can be scaled to at least 10 nm gatelength.

P. Ellinghaus et al., Wigner Analysis of Surface Roughness in Quantum Wires, International Wigner Workshop (IW2), Book of Abstracts, 2017, p. 40

Surface roughness (SR) is the low field electron mobility limiting mechanism in confined structures. Classical (Monte Carlo) transport models describe SR effects in terms of position independent scattering probability An alternative approach is based on the first principle Wigner function simulations of the SR interface. The analysis provides a deep insight in the processes governing time-dependent, quantum electron dynamics in presence of SR and the induced quantum transport effects.

J. Weinbub et al., Wigner-signed Particles Study of Double Dopant Quantum Effects, International Wigner Workshop (IW2), Book of Abstracts, 2017, p. 50

We investigate the quantum effects induced by two attractive dopants positioned on the electron path in a structure which resembles a two-dimensional quantum wire. We use Wigner simulations to analyze effects of correlation and interference imposed by the two dopants. The main conclusion is, that, the evolving electron system maintains coherence, giving rise to a correlation pattern the electron density which is placed after the position of the dopants.

T. Al-Ameri et al., Does a Nanowire Transistor Follow the Golden Ratio, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 57

The signatures of isotropic charge distributions are observed, showing the same attributes as the golden ratio (Phi) described in art and architecture. A simulation study of ultra-scaled n-type silicon nanowire transistors (NWT) for the 5nm CMOS application is presented. The results reveal that the amount of mobile charge in the channel is determined by the device geometry and could also be related to the golden ratio (Phi). A link between the main device characteristics, such as a drive and leakage current, and cross-sectional shape and dimensions of the device is established. The correlation between the main Figure of Merit (FoM) and the device variability and reliability is discussed.

J.-C. Barbé et al., Stacked Nanowires/Nanosheets GAA MOSFET From Technology to Design Enablement, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 5

GAA nanowires (NW) transistors are promising candidates for sub 10 nm technology nodes. They offer optimal electrostatic control, thereby enabling ultimate CMOS device scaling. Horizontally stacked they are a natural extension of today's mainstream technology. Considering enlarged NWs in Nanosheets (NS) allows to target the best compromise in power and performance for future applications. In this paper we will first briefly introduce the technology and then review what can bring advanced simulation focusing on both mobility and contact resistance. Further work on compact modeling and benchmarking is referred to in sections 2.4 and 2.5 below.

Z. Zeng et al., A Simple Interpolation Model for the Carrier Mobility in Trigate and Gate-All-Around Silicon NWFETs, IEEE, Trans. Electr. Dev. 64 (2017) 2485:

We compute the electron and hole mobilities in Trigate and gate-all-around silicon nanowires (SiNWs) within the nonequilibrium Green’s Function framework. We then

derive a simple model for the dependence of the mobility on the SiNW width and height. This model interpolates between the square SiNW and thin film limits. In order to provide a complete description of the mobility in SiNW devices,we calculate the phonon, surface roughness, and remote Coulomb-limited mobilities of square nanowires and of thin films with side or thickness t = 5, 7, and 10 nm. The mobility of arbitrary rectangular SiNWs with width W = t or height H = t can then be reconstructed from these partial mobilities using Matthiessen's rule. We show that these models successfully reproduce the trends measured on n- and p-type devices with different widths and orientations.

P. Ellinghaus et al., Analysis of Lense-governed Wigner Signed Particle Quantum Dynamics, Phys. Status Solidi RRL 11 (2017) 1700102

We present a Wigner signed particles analysis of the lense governed electron state dynamics based on the quantitative theory of coherence reformulated in phase space terms. The signed particle model of Wigner evolution enables physically intuitive insights into the processes maintaining coherence. Both, coherent processes and scattering-caused transitions to classical dynamics are unified by a scattering-aware particle model of the lense-controlled state evolution. Our approach bridges the fairly new theory of coherence with the Wigner signed particle method.

Papers published in 2018

C. Medina-Bailon et al., Study of the 1D Scattering Mechanisms´ Impact on the Mobility in Si Nanowire Transistors, in: Proceedings of EUROSOI-ULIS 2018, 2018, p. 17

The extensive research of aggressively scaled nanoelectronic devices necessitates the inclusion of quantum confinement effects and their impact on performance. This work implements a set of multisubband phonon and impurity scattering mechanisms within the Kubo-Greenwood formalism in order to study their impact on the mobility in Si nanowire transistors (NWTs). This 1D treatment has been coupled with a 3D Poisson-2D Schrödinger solver, which accurately captures the effects of quantum confinement on charge dynamics. We also emphasize the importance of using the 1D models to evaluate the geometrical properties on mobility at the scaling limit.

M. Nedjalkov et al., Stochastic Analysis of Surface Roughness Models in Quantum Wires, Comp. Phys. Comm. 228 (2018) 30

We present a signed particle computational approach for the Wigner transport model and use it to analyze the electron state dynamics in quantum wires focusing on the effect of surface roughness. Usually surface roughness is considered as a scattering model, accounted for by the Fermi Golden Rule, which relies on approximations like statistical averaging and in the case of quantum wires incorporates quantum corrections based on the mode space approach. We provide a novel computational approach to enable physical analysis of these assumptions in terms of phase space and particles, and discuss the physical consequences.

T. Al-Ameri et al., Correlation between the Golden Ratio and Nanowire Transistor Performance, Appl. Sci. 8 (2018) 54

This paper is an extension of a related paper published at SISPAD 2017, see above. It was observed that the signatures of isotropic charge distributions in silicon nanowire transistors (NWT) displayed identical characteristics to the golden ratio (Phi). In turn, a simulation was conducted regarding ultra-scaled n-type Si (NWT) with respect to the 5-nm complementary metal-oxide-semiconductor (CMOS) application. The results reveal that the amount of mobile charge in the channel and intrinsic speed of the device are determined by the device geometry and could also be correlated to the golden ratio (Phi). This paper highlights the issue that the optimization of NWT geometry could reduce the impact of the main sources of statistical variability on the Figure of Merit (FoM) of devices. In the context of industrial early successes in

fabricating vertically stacked NWT, ensemble Monte Carlo (MC) simulations with quantum correction are used to accurately predict the drive current. This occurs alongside a consideration of the degree to which the carrier transport in the vertically stacked lateral NWTs are complex.

S. Berrada et al., Quantum Transport Investigation of Threshold Voltage variability in Sub-10nm Junctionless Si Nanowire FETs, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 244

In this paper, we use the Non-Equilibrium Green's Function formalism to study the dependence of the threshold voltage variability on the cross-section shape and the gate length in JunctionLess Field Effect Transistors. Each configuration, i.e. gate length and cross-section, was investigated using a statistical ensemble of 100 samples. We found that the variability in threshold voltage is increased independently of the cross-section shape when the gate length is shrunk down to 5 nm. We attribute this results to the higher wave function "randomization" in longer gate lengths.

J. Lee et al., The Impact of Dopant Diffusion on Random Dopant Fluctuation in Si nanowire FETs: A Quantum Transport Study, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 280

In this work, we perform statistical quantum transport simulations with 3 x 3 nm^2 Si nanowire (NW) field effect transistors (FETs) to investigate the impact of dopant diffusion on random dopant fluctuation. First, we use an effective mass Hamiltonian for the transport where the confinement and transport effective masses are extracted from the tight-binding band structure calculations. The dopant diffusion along the transport direction from the source/drain regions to the channel region is modeled by the Gaussian doping profile. To generate random discrete dopants, we adopt a rejection scheme consideringthe 3-dimensional atomic arrangement of the NW structures. Our statistical simulation results show that the diffused dopants into the channel region cause large variability problems in Si NW FETs.

C. Medina-Bailon et al., Impact of the Effective Mass on the Mobility in Si Nanowire Transistors, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 297

In the simulation based research of aggressively scaled CMOS transistors, it is mandatory to combine advanced transport simulators and quantum confinement effects with atomistic simulations which accurately reproduce the electronic structure at the nanometer scale. This work investigates the impact of cross-section dependent effective masses, obtained from atomistic simulations, on the mobility in Si nanowire transistors (NWTs). For the transport simulations, we use the Kubo-Greenwood formalism with a set of multisubband phonon, surface roughness, and impurity scattering mechanisms.

J. Lee, O. Badami, H. Carrillo-Nunez, S. Berrada, C. Medina-Bailon, T. Dutta, F. Adamu-Lema, V.P. Georgiev, A. Asenov, Variability predictions for the next technology generations of n-type SixGe1-x nanowire MOSFETs. *Micromachines*, 9(12), 643.

Using a state-of-the-art quantum transport simulator based on the effective mass approximation, we have thoroughly studied the impact of variability on SixGe1-x channel gate-all-around nanowire metal-oxide-semiconductor field-effect transistors (NWFETs) associated with random discrete dopants, line edge roughness, and metal gate granularity. Performance predictions of NWFETs with different cross-sectional shapes such as square, circle, and ellipse are also investigated. For each NWFETs, the effective masses have carefully been extracted from $sp^3d^5s^*$ tight-binding band structures. In total, we have generated 7200 transistor samples and performed approximately 10,000 quantum transport simulations. Our statistical analysis reveals

that metal gate granularity is dominant among the variability sources considered in this work. Assuming the parameters of the variability sources are the same, we have found that there is no significance difference of variability between SiGe and Si channel NWFETs.

Papers published in 2019

T. Sadi et al., C. Simulation of the Impact of Ionized Impurity Scattering on the Total Mobility in Si Nanowire Transistors, Materials 12(1) (2019) 124

One simulation approach that delivers reliable mobility values at low-field near-equilibrium conditions for Nanowire transistors (NWTs) is the combination of the quantum confinement effects with the semi-classical Boltzmann transport equation, solved within the relaxation time approximation adopting the Kubo–Greenwood (KG) formalism, as implemented in this work. We consider the most relevant scattering mechanisms governing intraband and multi-subband transitions in NWTs, including phonon, surface roughness and ionized impurity scattering, whose rates have been calculated directly from the Fermi's Golden rule. In this paper, we couple multi-slice Poisson–Schrödinger solutions to the KG method to analyze the impact of various scattering mechanisms on the mobility of small diameter nanowire transistors. As demonstrated here, phonon and surface roughness scattering are strong mobility-limiting mechanisms in NWTs. However, scattering from ionized impurities has proved to be another important mobility-limiting mechanism, being mandatory for inclusion when simulating realistic and doped nanostructures, due to the short range Coulomb interaction with the carriers. We also illustrate the impact of the nanowire geometry, highlighting the advantage of using circular over square cross section shapes. The paper was accepted for publication at the end of 2018, and published in the first issue of 2019.

2.3 Interconnect Simulation

Another important subject of the project was the development of models and tools for the simulation of the fabrication, the performance and the reliability of interconnects. The simulation of the fabrication of interconnects is includes in the activities on equipment and process simulation, dealt with in section 2.1. Interconnect performance has been addressed as part of the work on compact modeling, see below in section 2.4. The dedicated work, and publications on interconnects listed below, refer to interconnect reliability.

L. Filipovic et al., Modeling Electromigration in Nanoscaled Copper Interconnects, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 161

This paper present an approach to modeling grain boundaries and material interfaces in nanoscaled copper interconnects. The novelty in the approach is the treatment of microstructure interfaces using a binary parameter, which is further used to define interface-specific material properties for copper resistivity and electromigration modeling. The models show that the inclusion of microstructure effects results in increased resistance and vacancy migration, and ultimately in a higher EM-induced stress.

L. Filipovic et al., Modeling the Influence of Grains and Material Interfaces on Electromigration, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 83

In this paper an efficient approach to properly treat grain boundaries and material interfaces when modeling electromigration in copper nano-interconnects is presented. Using this method even very coarse meshes were able to reasonably reproduce the

vacancy concentration of thin copper interconnects, including the microstructure. However, using a grid spacing greater than one half the grain boundary thickness resulted in underestimates of the induced stress.

2.4 Compact Models

The development of compact models and their extraction has been one of the core parts of the SUPERAID7 project. The related activities span from the integration between the various simulation levels addressed in the project across the development of compact models capable to address highly three-dimensional devices and to include both systematic and statistical process variations to the application of this hierarchical simulation flow and compact models to relevant device architectures. In turn, besides the four papers mentioned in this section, some publications mentioned in the other sections also include aspects of the compact modeling work.

L. Wang et al., TCAD Proven Compact Modelling Re-centering Technology for Early 0.x PDKs, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 157

Well-calibrated predictive TCAD simulations are employed to generate target data for compact models for better pre-V1.0 PDK development. A reliable re-centering technology has been developed which can accurately migrate the global and local variability and the corresponding corners. FinFETs calibrated to published data by Intel at the 14nm technology node are employed as test-bed devices.

O. Rozeau et al., NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs, in: Proceedings International Electron Devices Meeting (IEDM) 2016 O. Rozeau et al., NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs, in: Proceedings International Electron Devices Meeting (IEDM) 2016

In this work, a predictive and physical compact model for NanoWire/NanoSheet (NW/NS) Gate-All-Around (GAA) MOSFET is presented. Based on a novel methodology for the calculation of the surface potential including quantum confinement, this model is able to handle arbitrary NW/NS cross-section shape of stacked planar and vertical GAA MOSFETs (circular, square, rectangular). This Nanowire Surface Potential (NSP) based model, validated both by numerical simulations and experimental data, is demonstrated to be very accurate in all operation regimes of GAA MOSFETs.

J.-C. Barbé et al., Stacked Nanowires/Nanosheets GAA MOSFET From Technology to Design Enablement, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 5

Besides work on device simulation and benchmarking referred to in sections 2.2 and 2.5, respectively, this paper deals with compact modeling fed by both TCAD capturing electrostatics of the device and above mentioned advanced simulation for mobility.

J. Lorenz et al., Process Variability–Technological Challenge and Design Issue for Nanoscale Devices, Micromachines 1 (2019) 6

Besides the technological challenges referred to in section 2.1, the feasibility of a full simulation of the impact of relevant systematic and stochastic variations on advanced devices and circuits is demonstrated..

2.5 Benchmarks

The eight papers listed below deal with experiments, characterization and related simulation work, carried out mainly by the SUPERAID7 partner CEA/Leti. Whereas experiments were largely taken from background and sideground work, the resources from SUPERAID7 ena-

bled the adaptation and usage of that results for the purposes of the project. Results from SUPERAID7 were partly used to support the experimental work discussed here.

S. Barraud et al., Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain, in: Proceedings International Electron Devices Meeting (IEDM) 2016

We report on vertically stacked horizontal Si NanoWires (NW) *p*-MOSFETs fabricated with a replacement metal gate (RMG) process. For the first time, stacked-NWs transistors are integrated with inner spacers and SiGe source-drain (S/D) stressors. Recessed and epitaxially re-grown SiGe(B) S/D junctions are shown to be efficient to inject strain into Si *p*-channels. The Precession Electron Diffraction (PED) technique, with a nm-scale precision, is used to quantify the deformation and provide useful information about strain fields at different stages of the fabrication process. Finally, a significant compressive strain and excellent short-channel characteristics are demonstrated in stacked-NWs *p*-FETs.

B. Cardoso Paz et al., New Method for Individual Electrical Characterization of Stacked SOI Nanowire MOSFETs, in: Proceedings 2017 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)

A new systematic procedure to separate the electrical characteristics of advanced stacked nanowires (NWs) with emphasis on mobility extraction is presented. The proposed method is based on I-V measurements varying the back gate bias (VB) and consists of three basic main steps, accounting for VB influence on transport parameters. Lower mobility was obtained for the top GAA NW in comparison to bottom Ω-NW. Temperature dependence of carrier mobility is also studied through the proposed method up to 150°C.

B. Cardoso Paz et al., Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires, in: Proceedings 2017 Joint International EUROSOI-ULIS Workshop

This work presents the performance and transport characteristics of vertically stacked p-MOSFET SOI nanowires (NWs) with inner spacers and epitaxial growth of SiGe raised source/drain. Electrical characterization is performed for NWs with [110] and [100] channel orientations, as a function of both fin width (WFIN) and channel length (L). Results show a good electrostatic control and reduced short channel effects (SCE) down to 15nm gate length. Improved effective mobility is obtained for [110]-oriented NWs due to higher sidewall mobility contribution.

J.-C. Barbé et al., Stacked Nanowires/Nanosheets GAA MOSFET From Technology to Design Enablement, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 5 (see also section 2.2 above)

Besides work on device simulation and compact modeling referred to above in sections 2.2 and 2.4, respectively, in this paper the capability of the model to capture actual hardware data as well as to benchmark the different architectures in competition down to 5 nm technology node is demonstrated.

S. Barraud, V. Lapras, M. Samson, B. Previtali, J. Hartmann, N. Rambal, C. Vizioz, V. Loup, C. Comboroure, F. Triozon, N. Bernier, D. Cooper, M. Vinet, Stacked-Wires FETs for Advanced CMOS Scaling , Proceedings 2017 International Conference on Solid State Devices and Materials (SSDM 2017)

We present recent progress on vertically stacked-wires MOSFETs with a replacement metal gate process for CMOS scaling beyond FinFET technology. Key technological challenges (such as 3D integration process including inner spacer, mobility, and strain engineering engineering) will be discussed in relation to recent research results.

S. Barraud et al., Performance and Design Considerations for Gate-All-Around Stacked-NanoWires FETs, in: Proceedings International Electron Devices Meeting (IEDM) 2017

This paper presents recent progress on Gate-All-Around (GAA) stacked-NanoWire (NW) / NanoSheet (NS) MOSFETs. Key technological challenges will be discussed and recent research results presented. Width-dependent carrier mobility in Si NW/NS and FinFET will be analyzed, and intrinsic performance and design considerations of GAA structures will be discussed and compared to FinFET devices with a focus on electrostatics, parasitic capacitances and different layout options. The results show that more flexibility can be achieved with stacked-NS transistors in order to manage power-performance optimization.

B. Cardoso Paz et al., Electrical Characterization of Vertically Stacked p-FET SOI Nanowires, Solid-State Electronics 141 (2018) 84

This work presents the performance and transport characteristics of vertically stacked p-type MOSFET SOI nanowires (NWs) with inner spacers and epitaxial growth of Si-Ge raised source/drain. The conventional procedure to extract the effective oxide thickness (EOT) and Shift and Ratio Method (S&R) have been adapted and validated through tridimensional numerical simulations. Electrical characterization is performed for NWs with [110]- and [100]-oriented channels, as a function of both fin width (W_{FIN}) and channel length (L). Results show a good electrostatic control and reduced short channel effects (SCE) down to 15 nm gate length, for both orientations. Effective mobility is found around two times higher for [110]- in comparison to [100]-oriented NWs due to higher holes mobility contribution in (110) plan. Improvements obtained on I_{ON}/I_{OFF} by reducing W_{FIN} are mainly due to subthreshold slope decrease, once small and none mobility increase is obtained for [110]- and [100]-oriented NWs, respectively.

B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, Methodology to Separate Channel Conductions of Two Level Vertically Stacked SOI Nanowire MOSFETs, Solid-State Electronics 149 (2018) 62

This work proposes a new method for dissociating both channel conductions of two levels vertically stacked inversion mode nanowires (NWs) composed by a Gate-All-Around (GAA) level on top of an Ω-gate level. The proposed methodology is based on experimental measurements of the total drain current (IDS) varying the back gate bias (VB), aiming the extraction of carriers' mobility of each level separately. The methodology consists of three main steps and accounts for VB influence on mobility. The behavior of non-stacked Ω-gate NWs are also discussed varying VB through experimental measurements and tridimensional numerical simulations in order to sustain proposed expressions of mobility dependence on VB for the bottom level of the stacked structure. Lower mobility was obtained for GAA in comparison to Ω-gate. The procedure was validated for a wide range of VB and up to 150°C. Similar temperature dependence of mobility was observed for both Ω-gate and GAA levels.

3. Conclusions

A large number of papers has been published from the SUPERAID7 project at leading international conferences and in important scientific journals. All these publications have been made available via Gold Open Access or at least via Green Open Access. In this deliverable the publications have been positioned within the scope of the project and put into perspective with each other. This should give a very good overview of the overall results obtained and efficiently guide the reader to those papers which address topics he is especially interested in.