This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688101.

ICT Project No 688101

SUPERAID7

Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7nm Node

D1.8: Public Workshop on Variability

	Name	Organisation	Date
Edited	Jürgen Lorenz	Fraunhofer IISB	27.09.2018

Contents

Abstract

As part of its dissemination actions SUPERAID7 organized a workshop on Monday September 3, 2018, in Dresden, Germany, linked to the ESSDERC and ESSCIRC conferences held there from September 4 to 16. During the last years it has developed as a standard practice that several workshops are held the day before or after these conferences, either at or close to the conference venue. Usually some of these workshops are directly linked and/or organized by European projects. This time, there were four full-day workshops held, plus three full-day tutorials.

The workshop organized by SUPERAID7 was named “SUPERAID7 - Process variations from equipment effects to circuit and design impact“, which reflected well the scope of the project. It consisted of eight presentations from SUPERAID7 and one external industrial keynote presentation which linked to the ECSEL project Way2GoFast. In total it was attended by about 20 people.

1. Introduction

For several years and until 2015, several tutorials were held on the day before the combined ESSDERC and ESSCIRC conferences, whereas several workshops were held the day after, covering areas addressed by either of these two conferences, in order to reach conference participants and to give them the opportunity to attend the workshops and tutorials with minimum extra travelling costs. Usually a large fraction of these workshops has been organized by European RTD projects. Since ESSDERC/ESSCIRC 2016, both the tutorials and the workshops are held the day before the conference. In turn, participants can no more attend both a workshop and a tutorial. However, the possibility to switch from one event to the other still exists, at least unofficially.

Due to the merger of the ESSDERC/ESSCIRC tutorial day and the workshop day into one, it was discussed within the SUPERAID7 consortium whether it was still appropriate to organize the SUPERAID7 workshop linked to these conferences, as originally planned. It was finally decided to stick to that initial planning, especially because via ESSDERC a link to the technology and device community could be made, whereas via ESSCIRC an additional link to the circuit and design community would be available.

2. Goals, agenda and outcomes of the SUPERAID7 workshop

The objective of the workshop was to present the concept and selected results of the project to the public. In view of this, besides the welcome presentation given by the SUPERAID7 project coordinator J. Lorenz eight presentations were made by representatives from SUPERAID7, namely an overview of the project, five topical presentations dealing with SUPERAID7 work at process, device (models and simulation), interconnect and circuit level, one on Design-Technology Co-Optimization in SUPERAID7 and beyond, and finally a presentation linking experiments and simulation. The technical presentations were started with a talk from ST on the analysis of statistical variability within the Way2GoFast project. ST is one of the members of the Industrial and Scientific Advisory Board of SUPERAID7.

The workshop was attended by about 20 people. This number can hardly be set in relation to the overall attendance in ESSDERC/ESSCIRC, because on one hand side also the tutorials were held in parallel, and on the other hand side two of the workshops (MOS-AK and SINANO/NEREID) have established communities which meet more or less regularly at ESSDERC/ESSCIRC.

3. Summary of workshop presentation and its dissemination via the WWW

This section gives a very brief summary of some aspects of the presentations and furthermore outlines the dissemination path and action.

3.1 Key messages from presentations

Some key messages from the presentations are listed in the order of the agenda:

- J. Lorenz, Fraunhofer IISB: Welcome and Orientation

  This short introduction referred to the EC funding and presented both the SUPERAID7 consortium and the agenda for the workshop.

- J. Lorenz, Fraunhofer IISB: Process variability and the SUPERAID7 approach

  J. Lorenz introduced variations and the SUPERAID7 objectives and shortly presented background work as the baseline of the project, together with new challenges to be addressed in SUPERAID7. He then showed project data and project structure, outlined the methodology used in the project, and illustrated this with three examples of key requirements to be taken on board. Finally, he drew conclusions, gave an outlook, and acknowledged the contributions of people involved and finally the EC funding.

- A. Juge, STMicroelectronics: Statistical variability analysis in 28 nm UTBB FD-SOI devices

  A. Juge briefly outlined the ECSEL project Way2GoFast and its main activities related to SUPERAID7. He then reported about work carried out within Way2GoFast on the characterization of statistical variability, calibration of Sentaurus Device and of GARAND, variability studies with GARAND, and finally about enhancements of the Leti UTSOI model. He finished his talk with conclusions and acknowledgements.

- E. Bär, Fraunhofer IISB: Variability-aware topography simulation

  E. Bär outlined the approach and the state-of-the-art for variability-aware topography simulation, put it into context within the project, and briefly introduced the interaction between and the integration of the various topography modules. He outlined exemplary models for etching and deposition, and presented various etching and deposition simulation examples including some effects of variability. Finally he draw conclusions and gave an outlook.

- V. Georgiev, University of Glasgow: Physical models for nanowire device simulation

  V. Georgiev located this topic with the SUPERAID7 project and introduced the goals and the strategy of this activity. He briefly discussed and illustrated the physical models and methods addressed within SUPERAID7, namely Drift-Diffusion, Kubo-Greenwood, Non-Equilibrium Green's Function NEGF, and Wigner Monte Carlo. Finally he drew conclusions and gave an outlook.

- L. Filipovic, TU Wien: Simulation of nanoscale interconnects

  L. Filipovic introduced the goals and the strategy of this activity and located this topic with the SUPERAID7 project. He discussed electron scattering in metals, esp. copper, the approach used to model it, and parameters used. Scattering mechanisms are electron-electron, surface roughness scattering, and scattering at grain boundaries. He then discussed electromigration reliability. Its simulation especially

needs accurate and efficient discretization and meshing. Finally he drew conclusions and gave an outlook.

- V. Georgiev, University of Glasgow: Variability-aware simulation of nanoscale devices

  V. Georgiev located this topic with the SUPERAID7 project and briefly discussed various kinds of statistical variability and their importance at various technology nodes, from device to circuit. He briefly included interconnect variability and time-dependent variability. He then presented various examples for the impact of statistical variability on nanowires. Finally he drew conclusions and gave an outlook.

- O. Rozeau, LETI: Leti-NSP model: SPICE model for advanced multigate MOSFETs

  In his introduction O. Rozeau outlined device architectures forecasted in the International Roadmap for Devices and Systems IRDS, which are the subject of the new Leti-NSP model. He outlined the concept of LETI-NSP, which starts from the two asymptotic cases of a nanosheet and of a circular nanowire. He presented the model implemented and compared it with TCAD including quantum confinement, showing very good agreement. He compared LETI-NSP with standard model requirements, which are largely met and need only few future enhancements. Code and manual are available. Finally he drew conclusions and outlined improvements planned for the next release.

- C. Millar, Synopsys: Simulation tools for DTCO of advanced technology nodes

  C. Millar located this topic with the SUPERAID7 project and outlined the overall concept for Design Technology Co-Optimization DTCO. He discussed the importance of the major technology issues addressed by DTCO depending on the technology nodes in question. He outlined DTCO tools and a typical pre-wafer DTCO flow. He presented a FinFET DTCO example, for which the Mystic tool is used for compact model extraction. He presented the results of the analysis of the response of a ring oscillator on variations of relevant technological results (like fin width). In his conclusion and outlook he among others mentioned that outputs from SUPERAID7 are already part of commercialized software and flows.

- S. Barraud, LETI: 3D devices: Experiment & simulation

  S. Barraud outlined the trends for further scaling of 3D FinFET and 2D FDSOI, and located device architectures within the SUPERAID7 workplan. He briefly discussed performance and design considerations for FinFETs, nanowires and nanosheets, especially regarding the trade-off between Short Channel Effect and effective width. He presented a process flow for GAA stacked wire FETs, implemented at LETI, and outlined the interaction with simulations carried out in SUPERAID7. He briefly discussed the strain and electrical characterization. In his conclusions he especially highlighted the advantages of horizontal GAA nanosheets.

- J. Lorenz, Fraunhofer IISB: Summary and discussion

  J. Lorenz largely came back to the conclusions already made in his introductory talk, again acknowledged the contributions of the SUPERAID7 team, and again acknowledged the funding from the EC. No further discussions was held in addition to those made directly at the individual presentations.

3.2 Publication at the WWW pages of ESSCIRC/ESSDERC and of SUPERAID7

Below and in the appendix, printouts of the material presented at the internet are shown, as follows:

- Fig. 1: Reference given at the public SUPERAID7 WWW page (as of September 27, 2018). The workshop presentations can be downloaded here.
- Fig. 2: References given at the WWW pages of ESSCIRC/ESSDERC 2018 (https://www.esscirc-essderc2018.org/workshops). In the box for SUPERAID7, “Program” links to the download of the program of the workshop, also displayed in Fig. 3.
- Appendix: The full set of the presentations given, as shown on the public WWW page of SUPERAID7. Two presentations had been very slightly modified during the internal release procedures at LETI and Synopsys.

Fig. 1: Reference to SUPERAID7 workshop given in the public SUPERAID7 WWW (at SUPERAID7 homepage www.superaid7.eu)

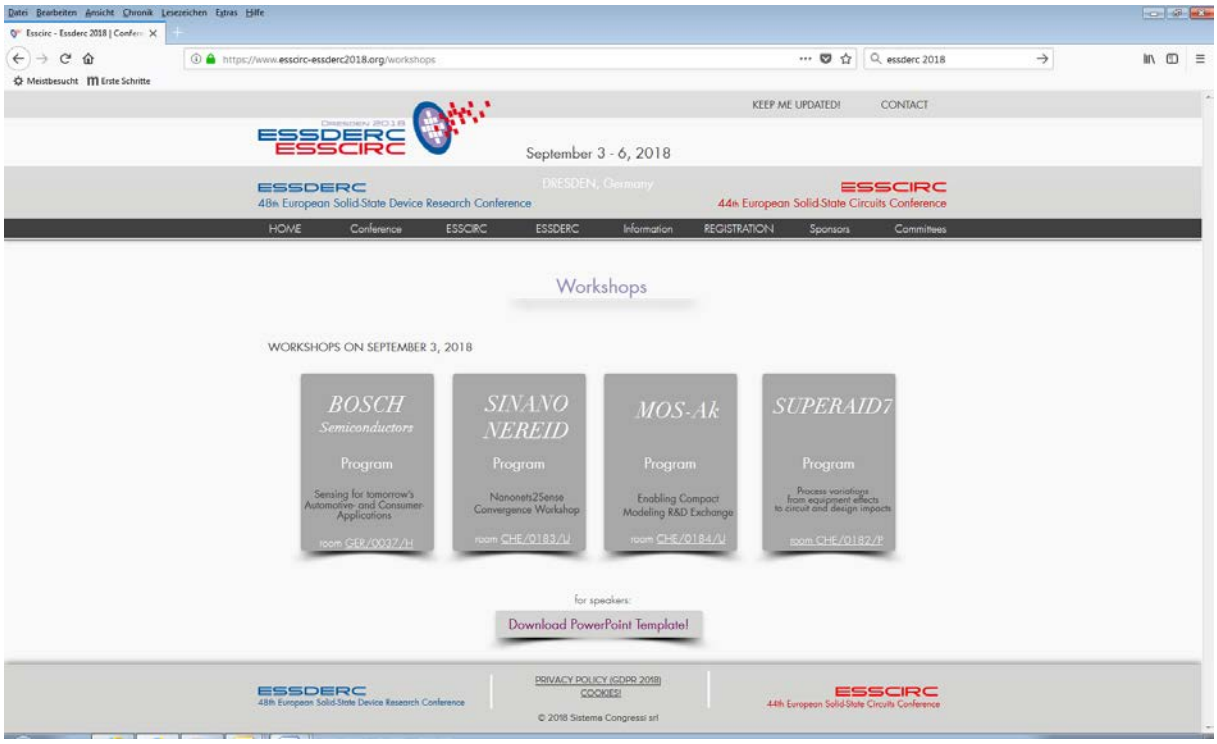
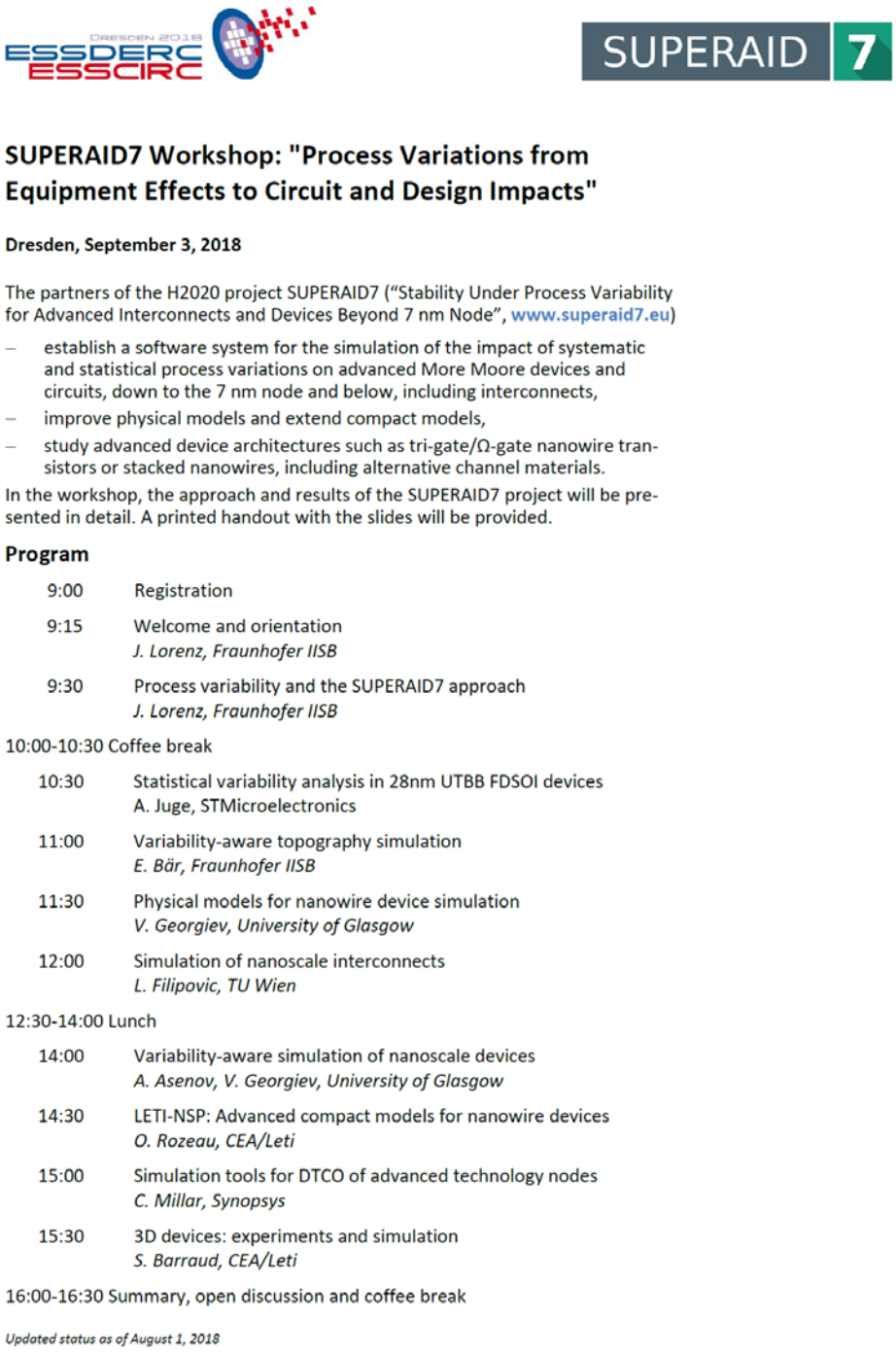


Fig. 2: References to workshops at ESSDERC / ESSCIRC WWW page



SUPERAID7 Workshop: "Process Variations from Equipment Effects to Circuit and Design Impacts"

Dresden, September 3, 2018

The partners of the H2020 project SUPERAID7 ("Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node", www.superaid7.eu)

- establish a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits, down to the 7 nm node and below, including interconnects,
- improve physical models and extend compact models,
- study advanced device architectures such as tri-gate/Ω-gate nanowire transistors or stacked nanowires, including alternative channel materials.

In the workshop, the approach and results of the SUPERAID7 project will be presented in detail. A printed handout with the slides will be provided.

Program

9:00	Registration
9:15	Welcome and orientation *J. Lorenz, Fraunhofer IISB*
9:30	Process variability and the SUPERAID7 approach *J. Lorenz, Fraunhofer IISB*

10:00-10:30 Coffee break

10:30	Statistical variability analysis in 28nm UTBB FDSOI devices A. Juge, STMicroelectronics
11:00	Variability-aware topography simulation *E. Bär, Fraunhofer IISB*
11:30	Physical models for nanowire device simulation *V. Georgiev, University of Glasgow*
12:00	Simulation of nanoscale interconnects *L. Filipovic, TU Wien*

12:30-14:00 Lunch

14:00	Variability-aware simulation of nanoscale devices *A. Asenov, V. Georgiev, University of Glasgow*
14:30	LETI-NSP: Advanced compact models for nanowire devices *O. Rozeau, CEA/Leti*
15:00	Simulation tools for DTCO of advanced technology nodes *C. Millar, Synopsys*
15:30	3D devices: experiments and simulation *S. Barraud, CEA/Leti*

16:00-16:30 Summary, open discussion and coffee break

Updated status as of August 1, 2018

Fig. 3: Workshop program downloaded from the ESSDERC / ESSCIRC WWW page

4 Conclusions

The SUPERAID7 project organized the workshop "SUPERAID7 - Process variations from equipment effects to circuit and design impact" linked to ESSCIRC/ESSDERC 2018 in Dresden, Germany. The workshop consisted of presentations from the project plus an invited external presentation from the SUPERAID7 ISAB member ST, and was attended by about 20 people. The presentations have been made available to the broad audience after the workshop via the SUPERAID7 WWW page.

Appendix: Workshop handout

The page numbers given below are the **pdf file page numbers**

SUPERAID7 Workshop: "Process Variations from Equipment Effects to Circuit and Design Impacts"

Dresden, September 3, 2018

The partners of the H2020 project SUPERAID7 ("Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node", **www.superaid7.eu**)

- establish a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits, down to the 7 nm node and below, including interconnects,
- improve physical models and extend compact models,
- study advanced device architectures such as tri-gate/Ω-gate nanowire transistors or stacked nanowires, including alternative channel materials.

In this workshop, the approach and results of the SUPERAID7 project are presented in detail.

Program

9:00 Registration

9:15 Welcome and orientation
J. Lorenz, Fraunhofer IISB

1

9:30 Process variability and the SUPERAID7 approach
J. Lorenz, Fraunhofer IISB

10:00-10:30 Coffee break

10:30 **2** Statistical variability analysis in 28 nm UTBB FDSOI devices
A. Juge, STMicroelectronics

11:00 **3** Variability-aware topography simulation
E. Bär, Fraunhofer IISB

11:30 **4** Physical models for nanowire device simulation
V. Georgiev, University of Glasgow

12:00 **5** Simulation of nanoscale interconnects
L. Filipovic, TU Wien

12:30-14:00 Lunch

14:00 **6** Variability-aware simulation of nanoscale devices
A. Asenov, V. Georgiev, University of Glasgow

14:30 **7** LETI-NSP: Advanced compact models for nanowire devices
O. Rozeau, CEA/Leti

15:00 **8** Simulation tools for DTCO of advanced technology nodes
C. Millar, Synopsys

15:30 **9** 3D devices: experiments and simulation
S. Barraud, CEA/Leti

16:00-16:30 Summary, open discussion and coffee **10**

Welcome and Orientation

Jürgen Lorenz
Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie IISB, Erlangen, Germany

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

H2020 Project SUPERAID7
Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm node

- Fundey by EC within the H2020 Programme
- Duration 01/2016-12/2018
- Overall funding 3377527.50 Euros, 363 PM
- Successor of FP7 project SUPERAID7 (10/2012 – 12/2015)
- Consortium of 2 research institutes, 2 universities, 1 software house

July 1, 2017 replaced by

Workshop Agenda

- This orientation
- Overview of SUPERAID7 project
- Keynote from member of Industrial and Scientific Advisory Board
- Seven presentations on key technical activities in SUPERAID7
- Summary and open discussion

- Copies of presentations (partly shortened) distributed at the beginning of the workshop

Workshop Agenda

9:00	Registration
9:15	Welcome and orientation *J. Lorenz, Fraunhofer IISB*
9:30	Process variability and the SUPERAID7 approach *J. Lorenz, Fraunhofer IISB*
10:00-10:30	Coffee break
10:30	Statistical variability analysis in 28nm UTBB FDSOI devices A. Juge, STMicroelectronics
11:00	Variability-aware topography simulation *E. Bär, Fraunhofer IISB*
11:30	Physical models for nanowire device simulation *V. Georgiev, University of Glasgow*
12:00	Simulation of nanoscale interconnects *L. Filipovic, TU Wien*
12:30-14:00	Lunch
14:00	Variability-aware simulation of nanoscale devices *A. Asenov, V. Georgiev, University of Glasgow*
14:30	LETI-NSP: Advanced compact models for nanowire devices *O. Rozeau, CEA/Leti*
15:00	Simulation tools for DTCO of advanced technology nodes *C. Millar, Synopsys*
15:30	3D devices: experiments and simulation *S. Barraud, CEA/Leti*
16:00-16:30	Summary, open discussion and coffee break

Updated status as of August 1, 2018

Process Variability and the SUPERAID7 Approach

Jürgen Lorenz
Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie IISB, Erlangen, Germany

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

Outline

- Introduction
- Background pillars and new challenges
- Consortium and project data
- SUPERAID7 project structure
- Methodology used
- Examples for impact of process variability
- Conclusions and Outlook

Introduction – Importance of Variations

- ITRS 2013 Modeling and Simulation chapter:
  - One of 7 “Near-term difficult challenges (2013-2020)” “Hierarchical simulation”, with issues among others
    - “Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations” and
    - “Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently”
  - One of 12 Technological Requirements: “Modeling for Design Robustness, Manufacturing and Yield”

⇒ SUPERAID7: Development of a software system for the simulation of the impact of all kinds of process variations (including their correlations) on devices and circuits

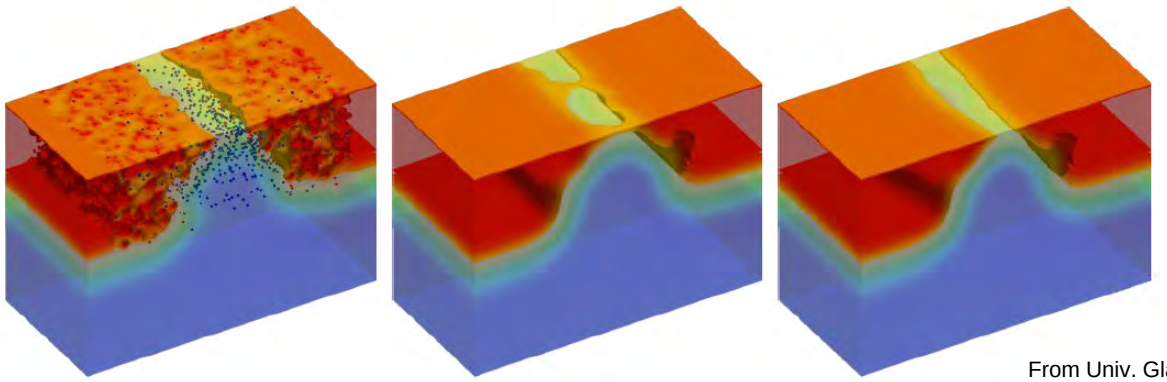
Introduction: Variations

- Numerous sources of process variations potentially influence the performance of active devices, interconnects and circuits:
  - Stochastical process variations resulting from the granularity of matter
  - Layout-induced process variations
  - Systematical variations resulting from non-idealities of process equipment
- Adequate assessment of the impacts of process variations requires to trace their effects from their source up to device / interconnect / circuit level
  - Same source of variations may influence various process results – e.g. sizes of different features, even in case of different nominal values
  - Correlations of variations of different process results must be traced and their impact on device and circuits assessed

Introduction: Stochastical Variations

- Stochastical variations caused by the granularity of matter
  - Random Dopant Fluctuations RDF
  - Line Edge Roughness LER
  - Metal Grain Granularity MGG

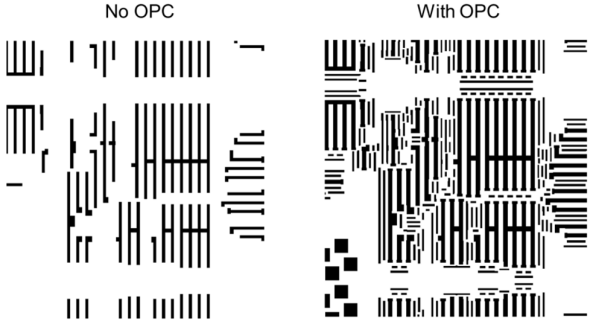
  discussed since long in the literature esp. for bulk devices



From Univ. Glasgow

Introduction: Layout-induced Process Variations

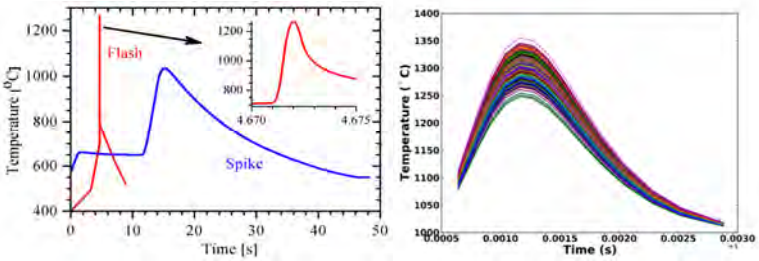
- Well known in the lithography community:
  - Printing of features influenced by other near-by features
  - Routinely considered in design: "Optical Proximity Correction" OPC
- So far hardly considered in other process steps, e.g.:
  - Pattern-dependent effects in deposition, etching (,CMP)
  - Pattern-dependent temperature profiles in millisecond / spike annealing, due to changes in reflectivity
  - …..



From Fraunhofer IISB

Introduction: Systematic Process Variations

- Caused by non-idealities / drifts of equipment parameters
  - Lithography esp. defocus, illumination dose / threshold
  - Deposition / etching: Variations across / between wafers due to inhomogeneity in gas flow and temperature distributions; source characteristics
  - For low-energy / Plasma Immersion Implantation: Variations in tilt and rotation angle ⇒ variations in residual channeling
  - Millisecond / flash annealing: Not completely reproducible temperature profiles



From Fraunhofer IISB

Background Pillars and New Challenges

- SW / model background:
  - Advanced physics-based programs for the simulation of lithography, deposition and etching (Fraunhofer IISB, TU Wien)
  - Statistical device simulator GARAND (originally GSS/GU), plus compact model extraction tools
  - Background models / modeling expertize for processes, devices and circuits (all partners)
  - Process integration results from advanced sub-10nm semiconductor technology (CEA/Leti)
  - Where appropriate: Use of commercial equipment / plasma simulation tools (e.g. Q-VT) and commercial process / device simulation tools (Sentaurus from Synopsys)

Background Pillars and New Challenges

- Preceding EU FP7 project SUPERTHEME (Circuit Stability Under process Variability and Electro-Thermal-Mechanical Coupling, 10/2012-12/2015)
  - Hierarchical simulation of the impact of process variations on bulk devices, including esp. *More than Moore* devices
  - Quantification of sources of process variations, by 4 equipment company partners
  - Highly three-dimensional devices necessary for sub-10 nm node not considered – except for idealized FinFET structure
  - See www.supertheme.eu

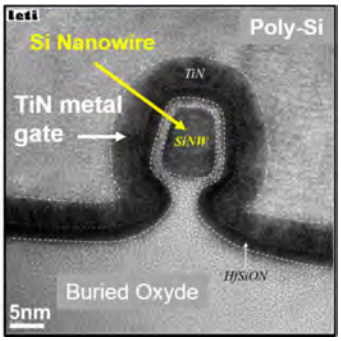
SUPERTHEME

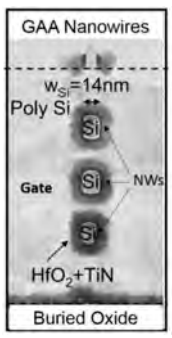
Background Pillars and New Challenges

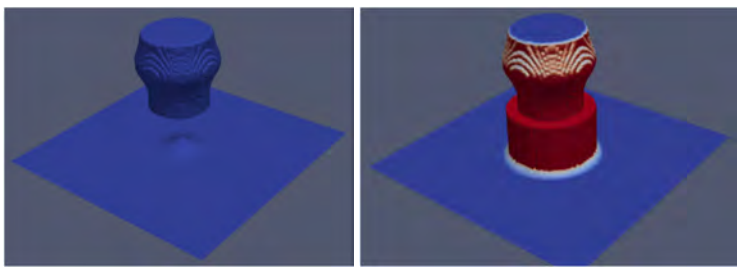
- New challenges for SUPERAID7 (I)
  - Sub-10nm devices such as (stacked) nanowires / nanosheets are highly three-dimensional and have non-ideal shapes

    ⇒ Accurate 3D simulation of topographies incl. their variability mandatory

    ⇒ Development of an integrated physics-based topography simulator (lithography/deposition/etching) necessary & one core activity in project



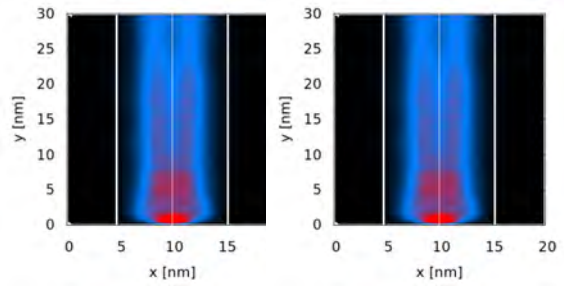




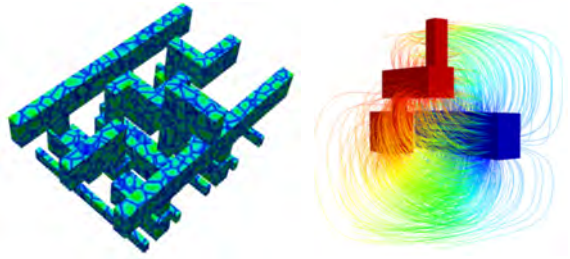
Left: SEM micrographs of nanowires (from LETI);
right: Coupled litho/etching simulation (from Fraunhofer IISB)

Background Pillars and New Challenges

- New challenges for SUPERAID7 (II)
  - Small feature sizes and /or rough interfaces necessitate refined and efficient modeling of quantum effects
    ⇒ Improved models for carrier transport in nanowires being developed: Confined carrier transport models
  - Interconnect performance, reliability and variability increasingly important for aggressively scaled devices
    ⇒ Development of physical models for interconnect simulation

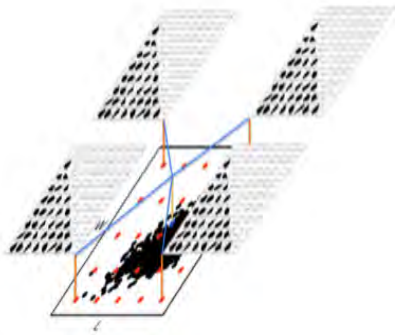


Electron density in ideal and rough nanowire (from TU Wien)


Interconnect structure for 14 nm FinFET based double inverter – Metal Line Granularity and electrical field lines (from Synopsys)

Background Pillars and New Challenges

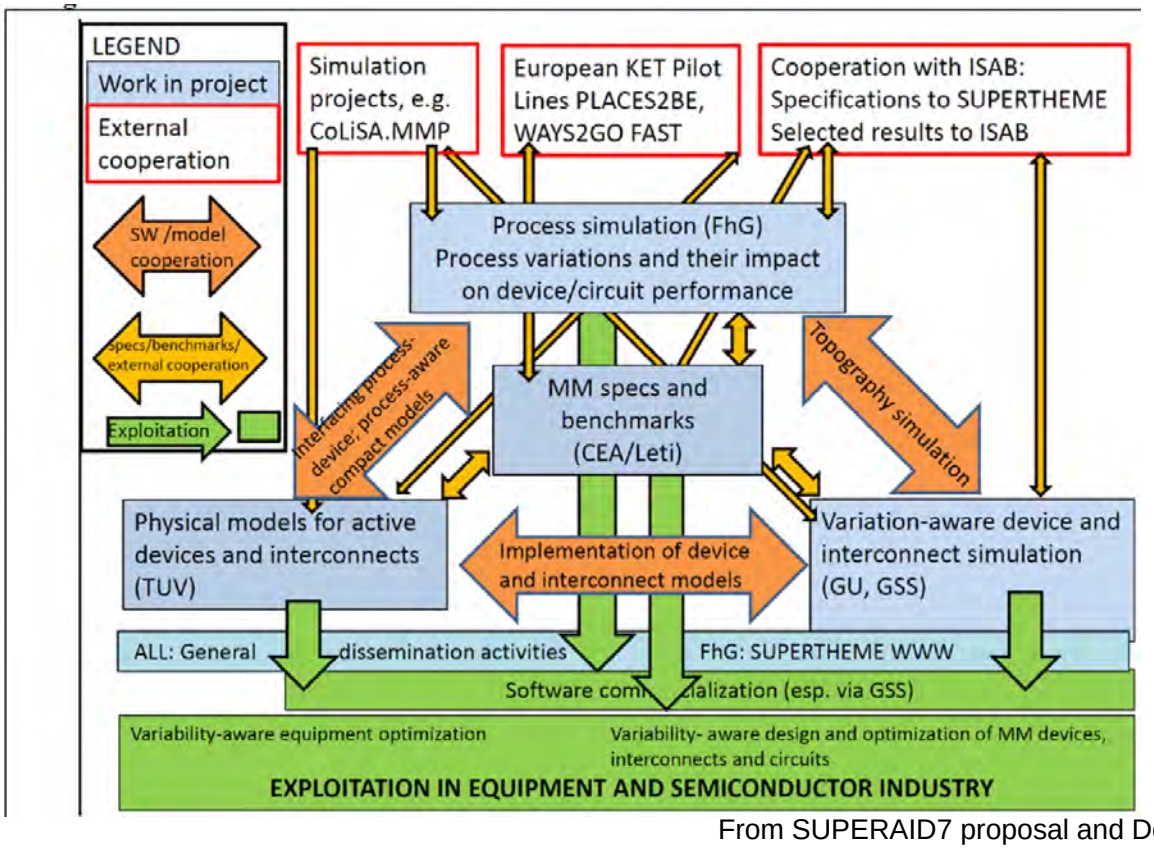
- New challenges for SUPERAID7 (III)
  - Existing compact models not applicable to highly three-dimensional device structures as addressed in SUPERAID7
    ⇒ Development /extension / use of new compact model LETI-NSP
  - Compact models to include variations of complicated device geometries
    ⇒ Traditional approach based on small set of simple geometrical parameters (e.g. 3*3 matrix of gate transistor length and width) no more applicable
    ⇒ Use varying process parameter itself as variable


From GSS/Synopsys

Consortium and Project Data

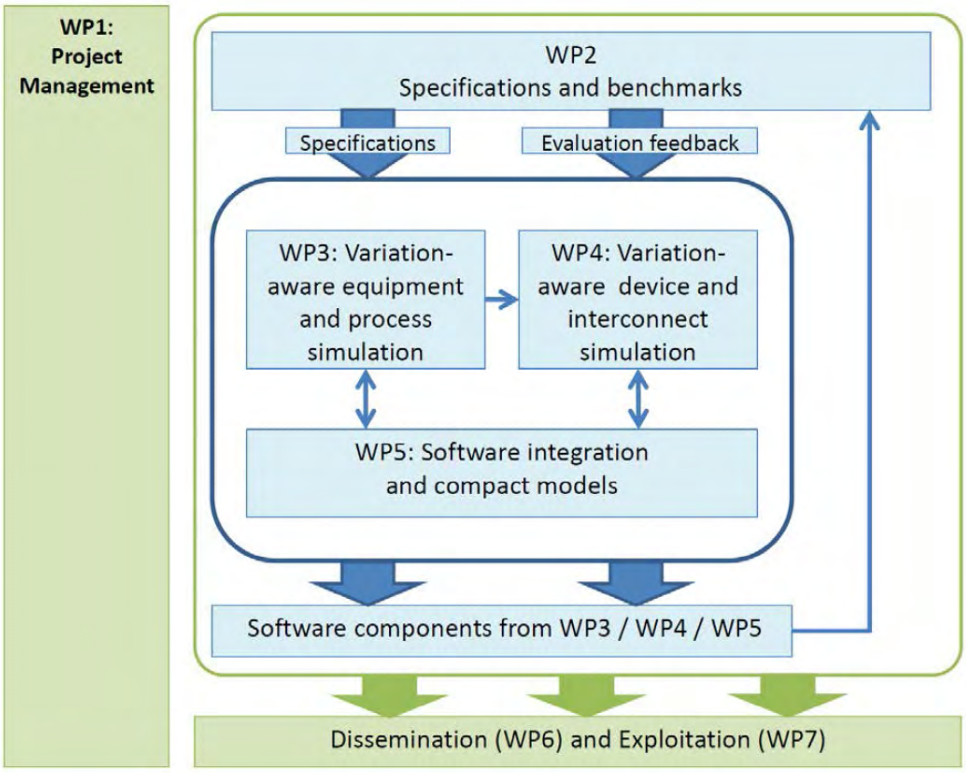
- Project partners
  - Research institutes: Fraunhofer IISB (coordinator), CEA/Leti
  - Universities: University of Glasgow, TU Wien
  - SW house: GSS – replaced July 2017 by Synopsys (due to take-over)
- Project duration: 01/2016 – 12/2018
- EC funding: 3377527.50 Euros from H2020 call ICT-25-2015 “Generic micro- and nano-electronic technologies
- See www.superaid7.eu

SUPERAID7 Project Structure



From SUPERAID7 proposal and DoA

SUPERAID7 Project Structure



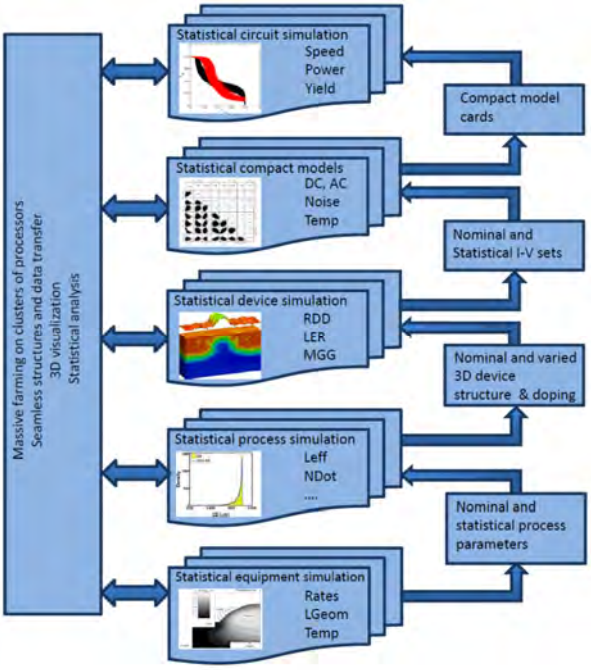
From SUPERAID7 proposal and DoA

Fraunhofer IISB

SUPERAID 7

Methodology Used: SW Architecture

- Equipment simulation: Use of external tools to derive variations of etching and deposition rates
- Process simulation: Development of a new integrated topography simulator. Use of Sentaurus Process for the doping steps
- Device simulation: Extension of statistical device simulator GARAND
- Prototype tool for interconnect simulation
- New compact model for 3D devices
- Extension of variability-aware compact modeling approach



Fraunhofer IISB

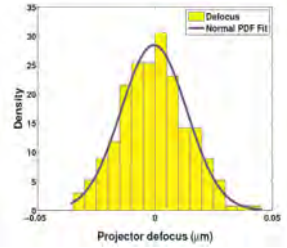
SUPERAID 7

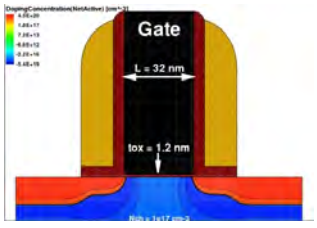
Methodology Used: Compact Model Extraction

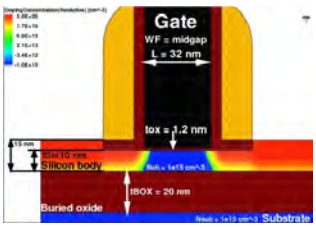
- Approach modified from procedure used in SUPERAID7 and published earlier:
  - LETI-NSP for compact modeling
  - For systematic variations: First identify those most relevant for device / circuit in question, considering each of them in isolation ⇒ limitation of DoE space from many to typically 2 or 3 parameters
  - Statistical compact model extraction as before: Three step extraction of statistical compact models including statistical variations (RDF, LER, MGG) for set of nominal devices, including the dependence on device geometry
  - Traditional approach: Convolution of statistical compact models with PDFs of relevant varying geometrical process results (e.g. gate length/width)
  - Modification: Variation of 3D device shape cannot always be described by physical parameters like length and width ⇒ partly include varying process inputs parameter into compact model extraction

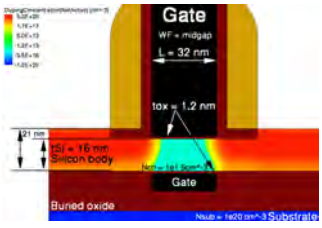
Example 1: Device Architectures as Filter for Variations

Impact of lithography focus variations on transistor performance





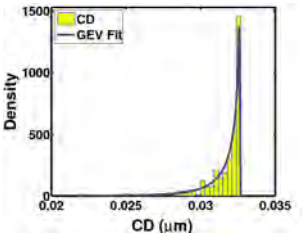


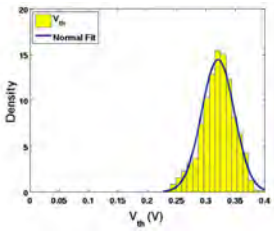


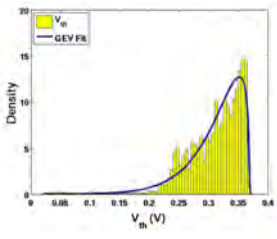
Focus variations ⬇ CD variations

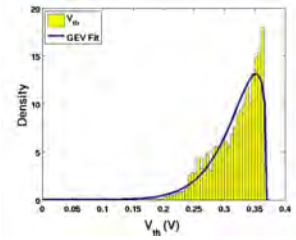
Device architecture: Bulk | SG FD SOI | DG FD SOI

acts as filter for CD variations and leads to variations e.g. of V_{th}





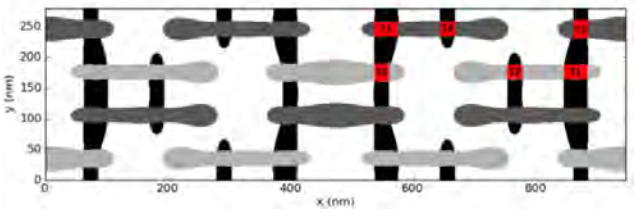


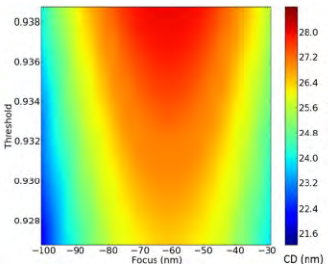


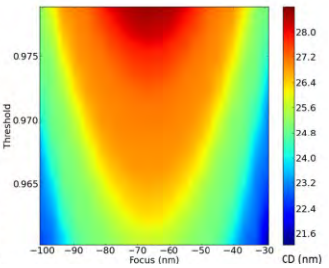
J. Lorenz et al., *Proc. 2009 Intl. Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, 2009, pp. 17-18.

Example 2: Impact of Correlations

- Impact of lithography defocus and dose/threshold variations on SRAM cell based on 20 nm / 25 nm gate length FinFET technology
  - LELE double patterning used
  - ⇒ Poly mask layer is split into two incremental mask layers, with statistically independent variations
  - ⇒ Variations correlate within transistor groups T1/T2/T6 and T3/T4/T5, but not between them. Example: PDF of gate length for T2 and T4.



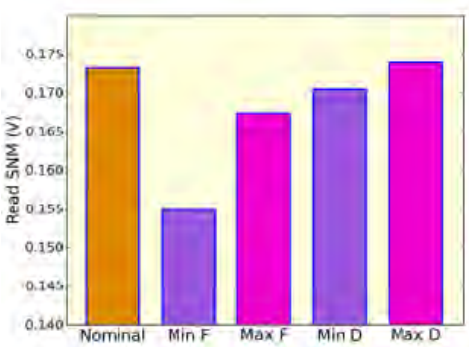


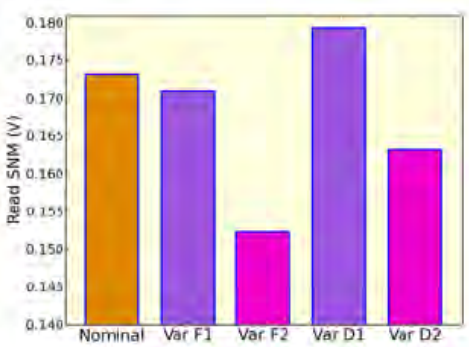


From P. Evanschitzky, A. Burenkov, J. Lorenz, Proc. SISPAD 2013

Example 2: Impact of Correlations

- Impact of lithography defocus and dose/threshold variations on SRAM cell based on 20 nm / 25 nm gate length FinFET technology
  - Different PDFs for channel lengths of the transistors
  - SRAM: Signal Noise Margin depending on variations and their correlations:
    - Left: Correlated variations – either all minimum or all maximum values
    - Right: Anticorrelated variations

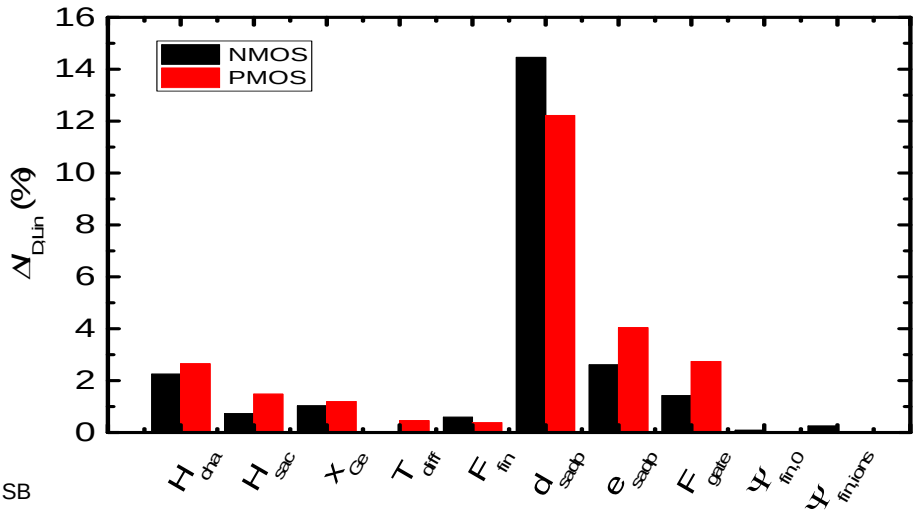




From P. Evanschitzky, A. Burenkov, J. Lorenz, Proc. SISPAD 2013

Example 3: Screening for most relevant systematic process variations

- Example for a nanowire process from CEA/LETI
  - Most relevant variations are SiGe mole fraction x_{Ge}, the fin SADP deposition factor d_{sadp} and the gate litho defocus.



From Fraunhofer IISB

Conclusions

- The impact of various kinds of systematical and stochastic variations on sub-10nm devices and circuits is important and needs to be assessed and minimized
- A hierarchical simulation approach is necessary and presented in this workshop to deal with the impact of variations, ranging from equipment simulation to statistical device simulation and compact model extraction
- Accurate and efficient process and device models are needed for variability studies
- The most relevant sources of variations must be identified and used in a DoE to minimize the complexity of simulation
- Systematic variations may influence several quantities in parallel, and partly cause correlations between these quantities. Such correlations must be considered in circuit simulation

SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

Outlook

- The importance of process variations and of the simulation and minimization of their impact will be further growing
- The approach presented in this workshop needs to be customized to the industrial process flow in question, especially regarding the large variety of systematic process variations which depend on details of the technology used.
- Work within SUPERAID7 and at its partners on the further extension of variation-aware compact models is ongoing

Acknowledgements

- Contribution of all colleagues at partners highly appreciated
- Valuable inputs from EC review team and from SUPERAID7 ISAB
- Funding from EC highly appreciated

The research leading to these results has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688101 SUPERAID7.

THANK YOU FOR YOUR ATTENTION!

Statistical Variability Analysis in 28nm UTBB FD-SOI devices

(Highlights from ECSEL JU Way2GoFast project)

André Juge[1], Plamen Asenov[2], Thierry Poiroux[3]

[1]STMicroelectronics, Crolles Site, 850 rue Jean Monnet, 38926 Crolles, France

[2]SYNOPSYS

[3]CEA-Leti, MINATEC Campus, 38054 Grenoble Cedex 9, France

SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

Outline

Presentation

Introduction to project Way2GoFast

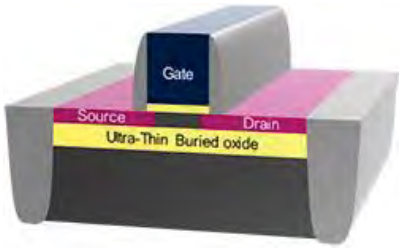
Statistical Variability analysis in 28nm FDSOI

Model for Circuit Design

Summary

ECSEL Way2GoFast project

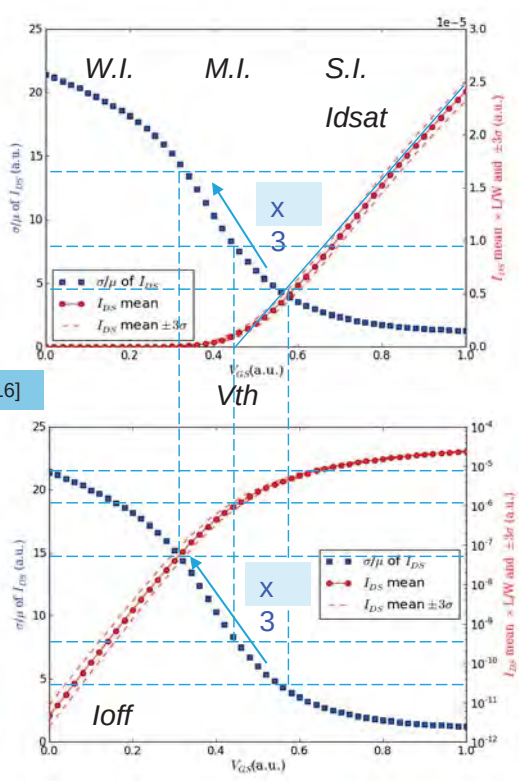
- UTBB FDSOI technology applications expand from Digital to mixed Digital-Analog-RF-mmW circuits
  - Market segments include Automotive, Connectivity, IoT, …



- Device Figures-of-merits (FoMs) addressed are multiple
  - Energy consumption remains as driving design parameter
  - Digital: Low dynamic power at given frequency, Low static power
  - Analog: Analog Gain, Variability (Matching, SCE), at low current
  - RF-mmW: High frequency response preserved at low voltage/low current

- Within ECSEL Way2GoFast project, during 2015 - 2017, 2 important developments were conducted in order to extend 28nm FDSOI technology applications to Low Power Digital-Analog-RF
  - Statistical Variability analysis, in cooperation with SYNOPSYS
  - Leti-UTSOI model enhancement for Low Power, in cooperation with CEA Leti

Variability Impact on Low Power Circuit Design



[SISPAD 2016]

- SV experiments in UTBB FDSOI
- Reduced Vdd or Id for Low Power
- Implies Near-Threshold operation
- SV impact x 3 from upper limit to lower limit of moderate inversion

- Objectives:
  - Device variability analysis
  - Model accuracy for circuit design throughout voltage range

Outline

Presentation

Introduction to project Way2GoFast

Statistical Variability analysis in 28nm FDSOI

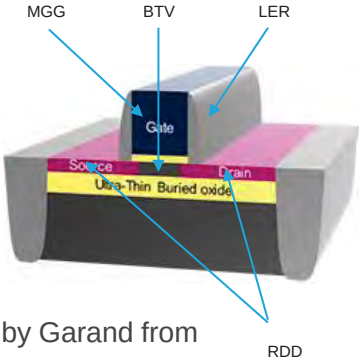
- **Characterization (Physical - Electrical)**
- TCAD device calibration (Physical - Electrical)
- GARAND device calibration
- Variability simulation with GARAND
- Device analysis

Model for Circuit Design

Summary

SV Characterization: Approach

- Objective
  - To rely on most complete and consistent data set
  - Physical and Electrical characterization techniques
- Physical
  - Line Width/Edge Roughness (LWR/LER)
  - Metal Grain Granularity (MGG). Grain size & Orientation.
  - Body Thickness Variation (BTV)
  - Some unknowns remain
    - Random Discrete Dopants (RDD) -> Discrete profile determined by Garand from calibrated continuous doping profiles
    - MGG work-function values -> calibrated through variability simulation process
    - Statistical impact of trapped charges at the interfaces of the thin body channel



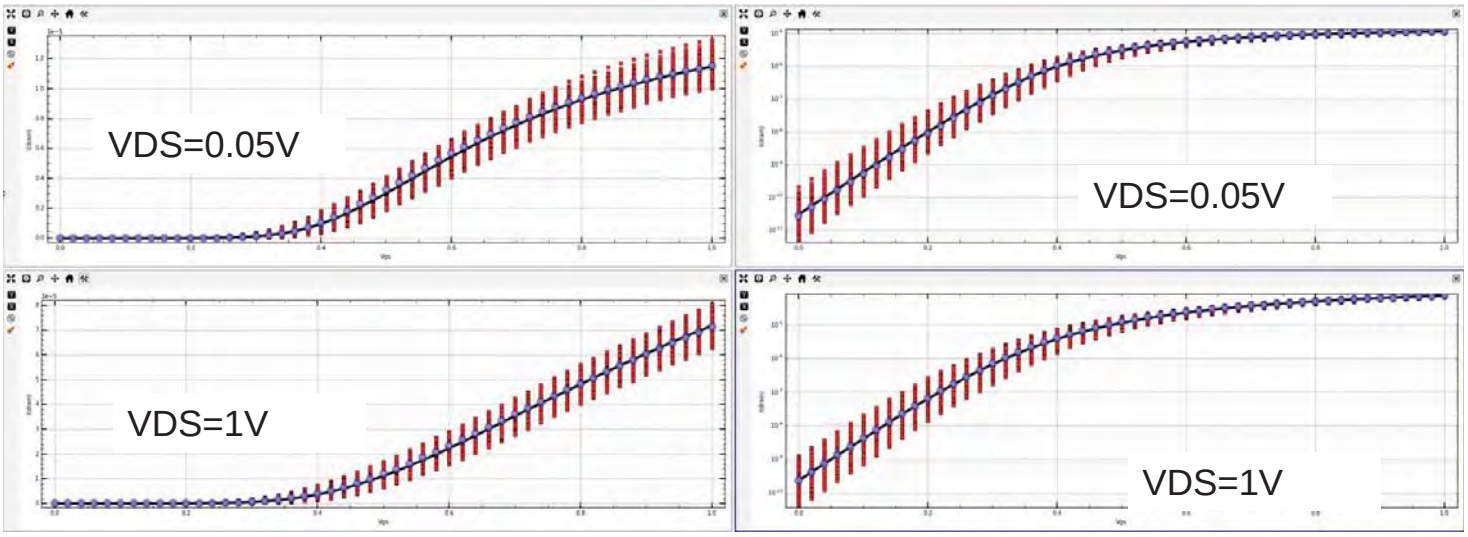
- Electrical
  - I(V) data from transistor array (256 pairs of DUT distributed in one direction), 1 die

SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

A.Juge & al. Statistical Variability analysis in 28nm FDSOI devices

Identification of median DUT

- One DUT selected as Golden from transistor array



Median

Golden DUT

Golden DUT closed to median I(V)
Small nMOS example

Outline

Presentation

Introduction to project Way2GoFast

Statistical Variability analysis in 28nm FDSOI

- Characterization (Physical - Electrical)
- **TCAD device calibration (Physical - Electrical)**
- Garand device calibration
- Variability simulation with Garand
- Device analysis

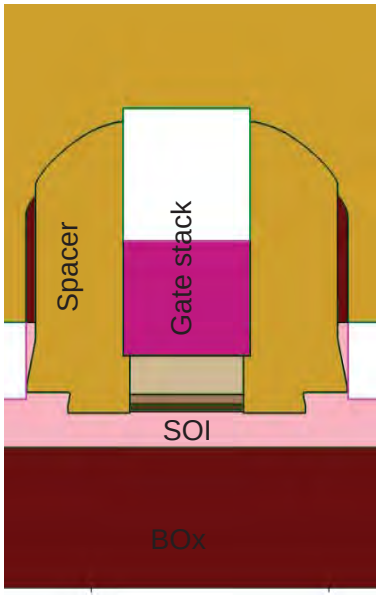
Model for Circuit Design

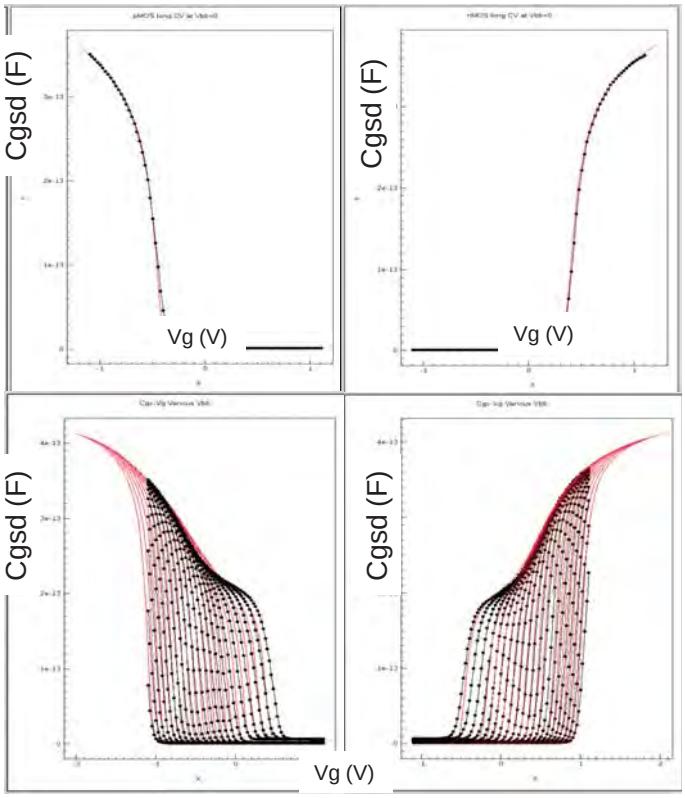
Summary

SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

A.Juge & al.
Statistical Variability analysis in 28nm FDSOI devices

Sentaurus Device calibration: Electrostatic

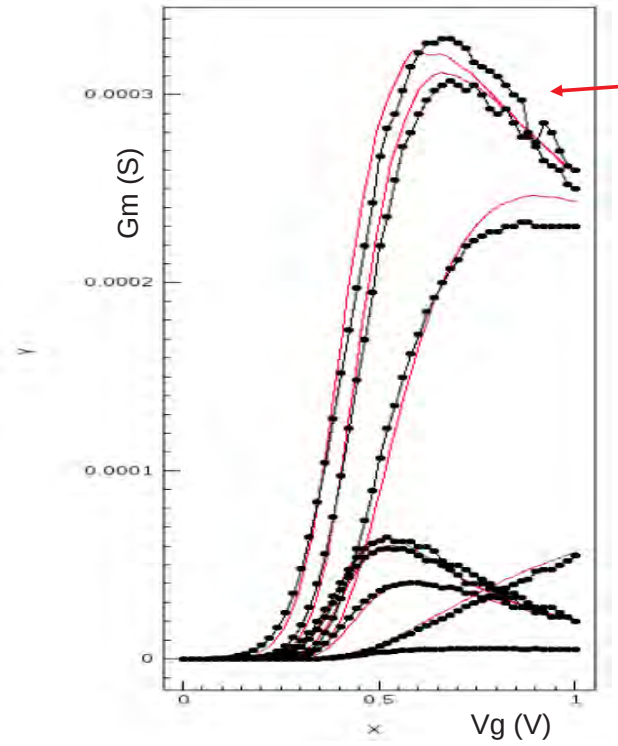




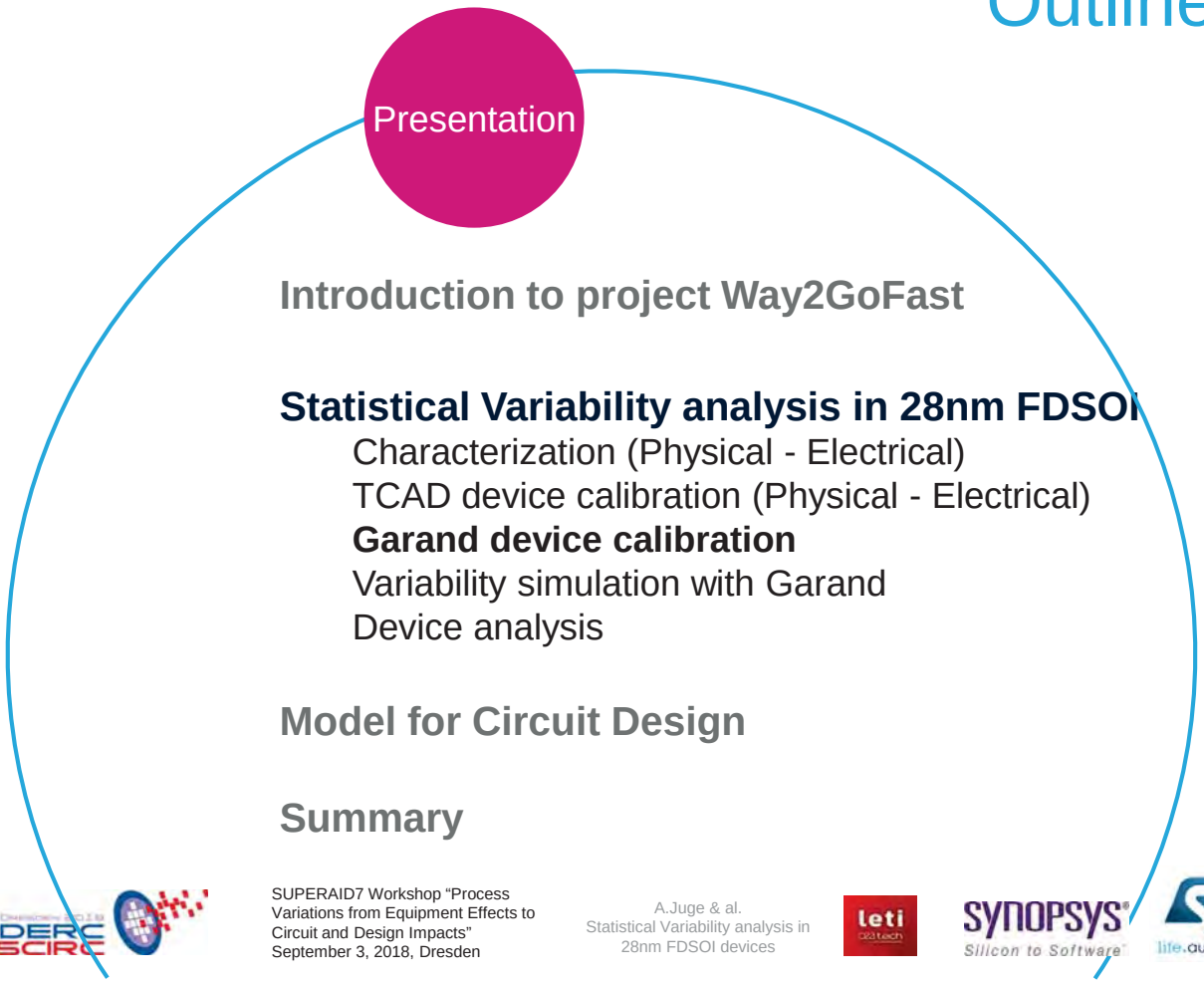
- CV at Vb=0
- Back and front inversion captured

Sentaurus Device Calibration: Transport

- Selected Models
  - Remote Coulomb Scattering
  - Remote Phonon Scattering
  - Ballistic mobility



Outline



Introduction to project Way2GoFast

Statistical Variability analysis in 28nm FDSOI

- Characterization (Physical - Electrical)
- TCAD device calibration (Physical - Electrical)
- **Garand device calibration**
- Variability simulation with Garand
- Device analysis

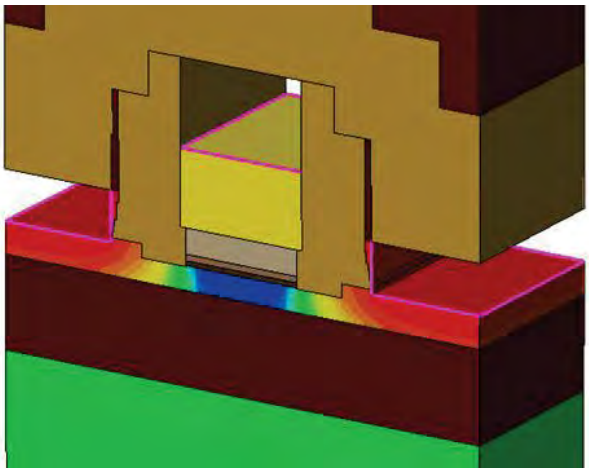
Model for Circuit Design

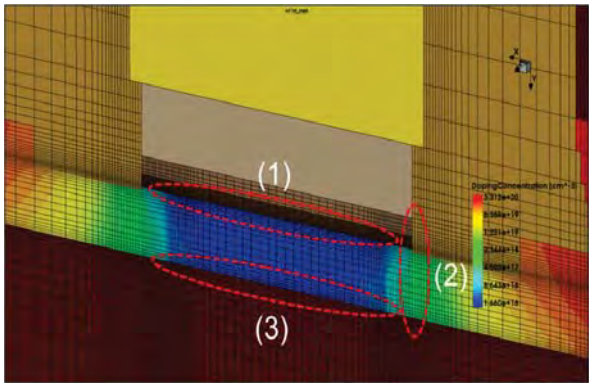
Summary

Simulation with Garand

- Device structure
  - Sentaurus 2D structure extended to 3D
  - Mesh refinement for regions (interfaces) exposed to LER and BTV
- Calibration strategy
  - Reference data: Device simulations from Sentaurus
  - Calibration Targets for Enigma tool
    - Charge distribution at middle of channel (density gradient DG)
    - Inversion charge Ninv vs Vgate voltage
    - Id (Vgate) at low and high Vd voltage for mobility fitting
  - Verification Cgg vs Vgate

Device structure





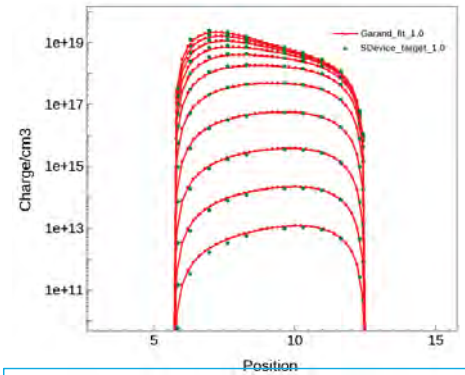
- Short gate length device extruded to 3D (left)
- Mesh refinement for regions exposed to LER and BTV (right)

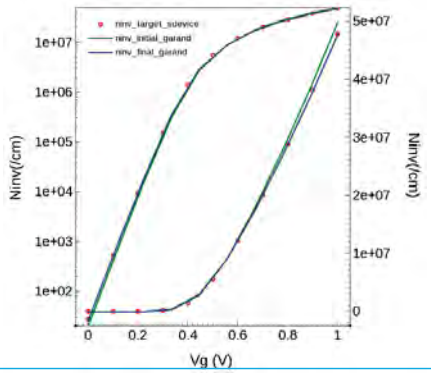
Created Automated Garand Calibration flow for FDSOI technologies

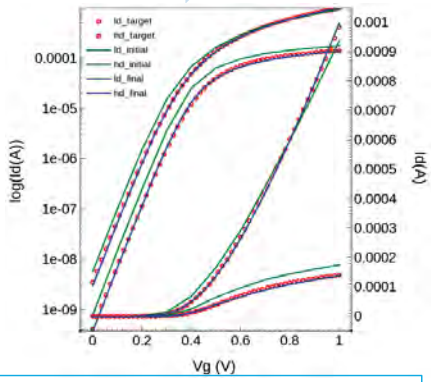
Quantum correction [DG] calibration

Inversion charge [Ninv vs. Vg] calibration

Mobility Calibration



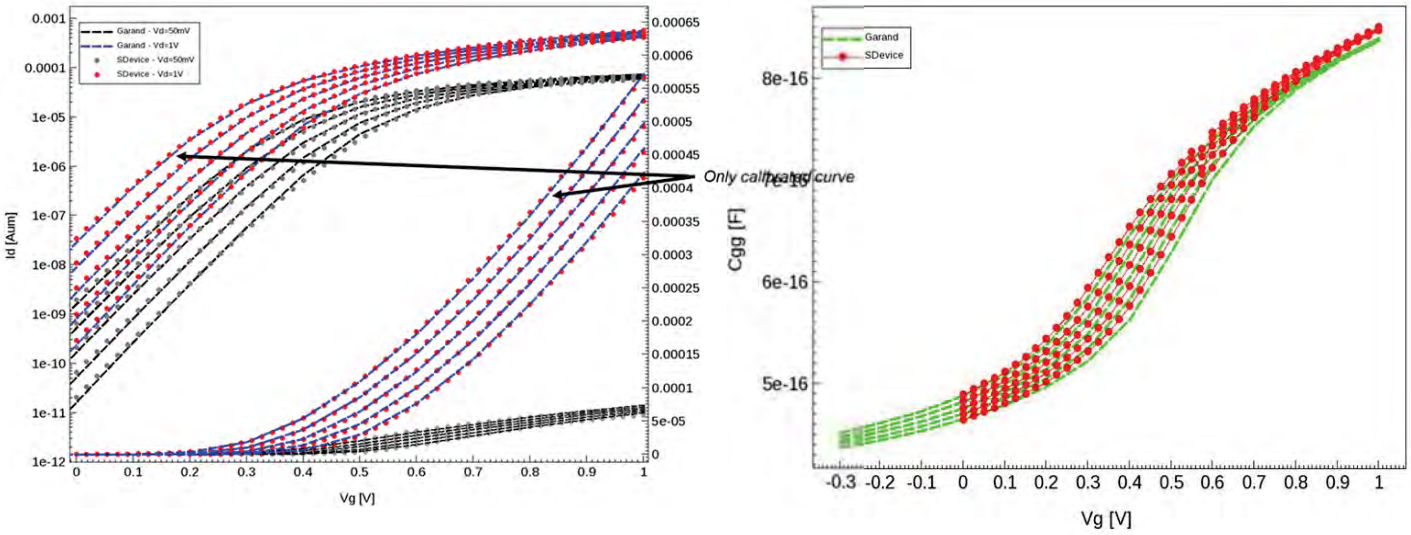




Developed during the project:

- Fully automated calibration for planar FDSOI technologies which enables Garand local variability analysis with an extremely low barrier-to-entry.
- Integrated into industry-standard framework tool Sentaurus Workbench.

Electrical inputs for Garand calibration



- Nominal DC calibration (Transport) over +/-1V BB *(Left)*
- Nominal AC verification (Electrostatic) over +/-1V BB *(Right)*

Outline

Presentation

Introduction to project Way2GoFast

Statistical Variability analysis in 28nm FDSOI

- Characterization (Physical - Electrical)
- TCAD device calibration (Physical - Electrical)
- Garand device calibration
- **Variability simulation with Garand**
- Device analysis

Model for Circuit Design

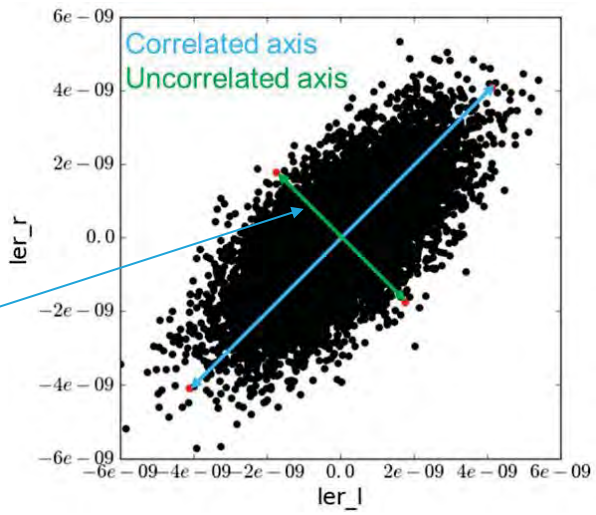
Summary

SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

A.Juge & al. Statistical Variability analysis in 28nm FDSOI devices

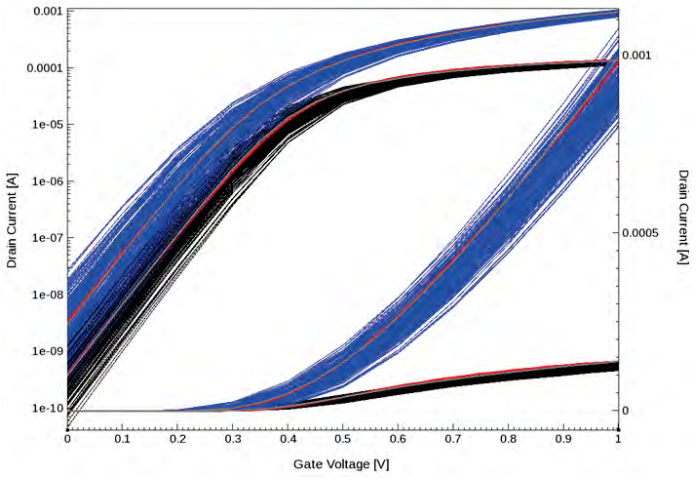
Local Variability inputs for Garand

Source	Parameter	comment
RDD	Supplied profile	Discretization by Garand
MGG	Average grain diameter	TEM data
	Orientation probability	TEM data
	Orientation Wf_delta	Literature for <111> & <200>, otherwise adjusted
LER	RMS	LER data wo edge/edge correlation
	LCOR	Best-guess
BTV	RMS	DRM/AFM data + adjust.
	LCOR	Best-guess

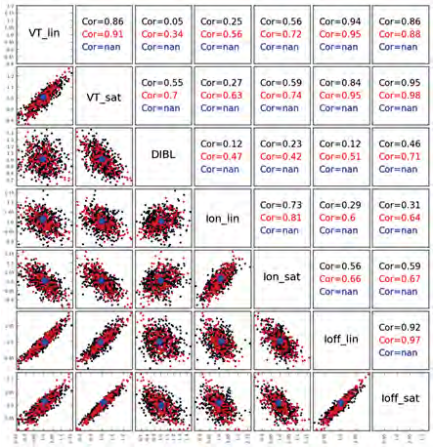


- Unknown parameters updated through iterative variability simulation (3-4)
- Enigma had to manage 2000 statistical simulations per iteration

Statistical Variability Analysis (nMOS)



- Simulation of nMOS Id(Vg) characteristics for 200 randomised devices



- Simulation/Hardware FOMs variations and correlations (normalized)

Sources contribution	σVT_{LIN}	σVT_{SAT}	$\sigma DIBL$	σION_{LIN}	σION_{SAT}
RDD	3	3	3	**1**	2
LER	4	4	3	4	4
MGG	**1**	**1**	2	3	**1**
BTV	2	2	**1**	2	3

SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

A.Juge & al. Statistical Variability analysis in 28nm FDSOI devices

Outline

Presentation

Introduction to project Way2GoFast

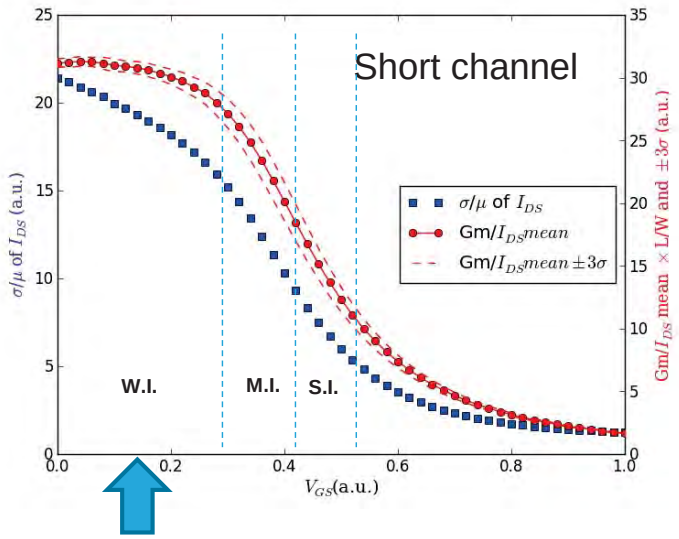
Statistical Variability analysis in 28nm FDSOI

Model for Circuit Design

How gm/I accuracy serves statistical model accuracy?
Leti UTSOI enhancements for gm/I

Summary

How Gm/Id model accuracy serves statistical modeling?



- Strong inversion

$$Ids \propto \beta \times (Vgs - Vth - Dibl \times Vds)^a$$

$$\left(\frac{\sigma_{Ids}}{Ids}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\boldsymbol{gm}}{\boldsymbol{Ids}}\right)^2 \times [\sigma_{Vth}^2 + Vds \times \sigma_{Dibl}^2]$$

- Gm/Id is the amplification factor by which variability in electrostatics induces bias-dependent variability of current
- Applies for whatever inversion regime
- Gm/Id accuracy helps variations modeling

- Weak inversion

$$Ids \propto \beta \times \exp\left(Vgs - Vth - Dibl \times Vds\right)/\left(n \times ut\right))$$

$$\left(\frac{\sigma_{Ids}}{Ids}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\boldsymbol{gm}}{\boldsymbol{Ids}}\right)^2 \times \left[\sigma_{Vth}^2 + Vds^2 \times \sigma_{Dibl}^2 + (Vgs - Vth)^2 \times \left(\frac{\sigma_n}{n}\right)^2\right]$$

[SISPAD 2016]

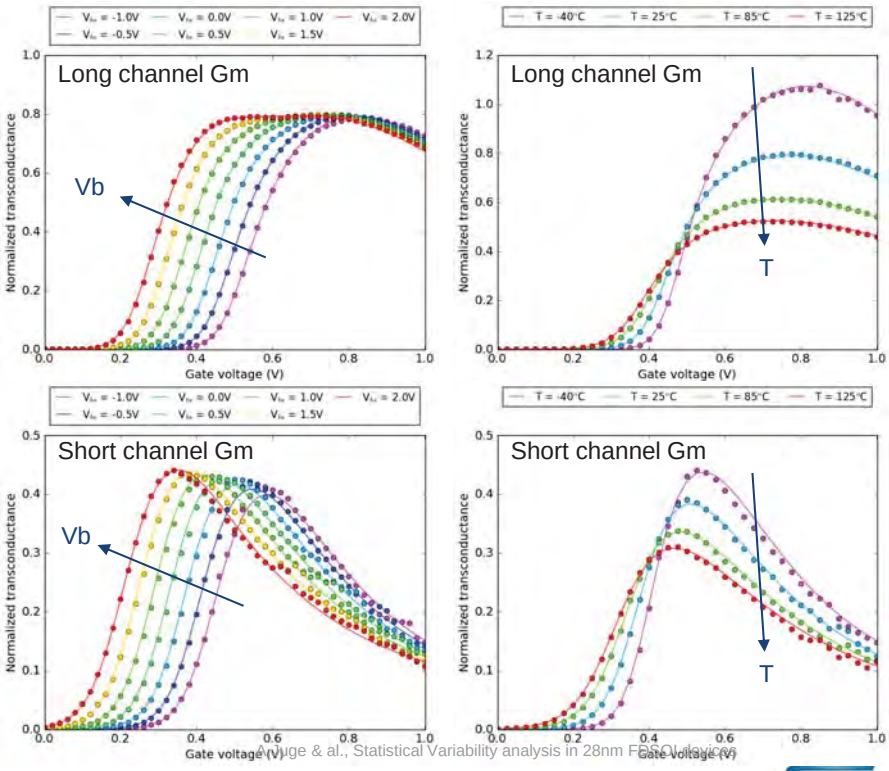
SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

A.Juge & al. Statistical Variability analysis in 28nm FDSOI devices

Leti UTSOI model enhancement for Gm/I

- Mobility and series resistance model improvements

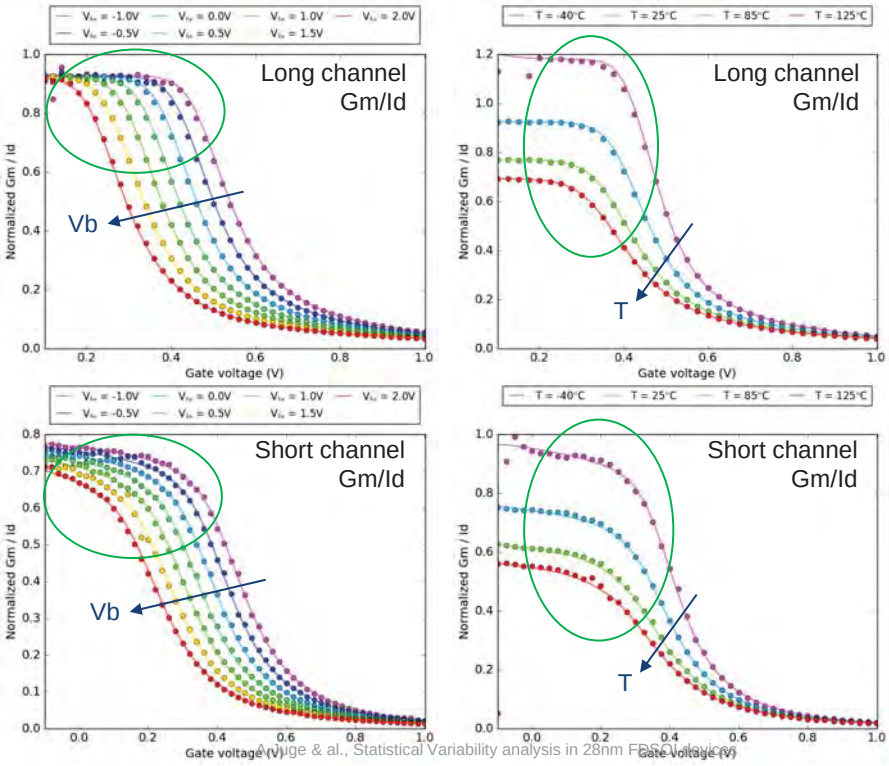
- Refined model for Coulomb scattering dependence with transverse field
- Refined model for series resistance dependence over back bias



Leti UTSOI model enhancement for Gm/I

- Improvement of accuracy in moderate inversion region

- Refined modeling of source/drain depletion as a function of longitudinal field



Summary

- Modelling for Low Power Analog-RF in 28nm FDSOI technology highlighted
  - Support of ECSEL JU Way2GoFast project
  - Cooperation between CEA Leti, Synopsys, and ST
- Physical/Electrical characterization methodologies suited for FDSOI devices
  - Some unknown parameters remain (Work-function values per grain orientation)
- Variability analysis with Garand
  - Provided well-calibrated TCAD deck, and set of physical/electrical variability data, Garand can predict the local variability, including key figure of merit sigmas and correlations
  - Tool chain capabilities were extended (MGG,..).
  - Enigma provides capability of reverse-engineering to provide physical inputs not available
  - Calibration methodology ensures consistent variability inputs for nMOS and pMOS devices
  - Comprehensive analysis of statistical variability observed in 28nm FDSOI device characteristics
  - Classification of local variability sources provides guidance for LP device optimization
- Leti-UTSOI model for Low Power Circuit Design
  - Accuracy in Gm/Id metric is valuable for Variability modeling
  - Leti-UTSOI qualified for Low Power Analog-RF circuit design using 28nm FDSOI technology

Acknowledgements

- ST: Y.Carminati, J.Franco, S.El Ghouli, G.Gouget, F.Monsieur, P.Normandon, K.Pradeep, D.Rideau, P.Scheer, A.Valery, M.Minondo, F.Arnaud, N.Planes
- CEA Leti: T.Poiroux, O.Rozeau, S.Martinie
- Synopsys: P.Asenov, C.Millar
- IMEP: G.Ghibaudo
- University of Glasgow: A.Asenov
- Fraunhofer Institute: J.Lorenz, E.Bär

life.augmented

Thank you for your attention !

Variability-aware Topography Simulation

Eberhard Baer
Fraunhofer IISB, 91058 Erlangen, Germany

ESSDERC/ESSCIRC Workshop
“Process Variations from Equipment Effects to Circuit and Design Impacts”
September 3, 2018, Dresden, Germany

Outline

- Introduction
  - Goals and strategy
  - Project context
- Software integration
- Simulation models
- Simulation examples
- Conclusions and outlook

Introduction – Goals and Strategy
Approach

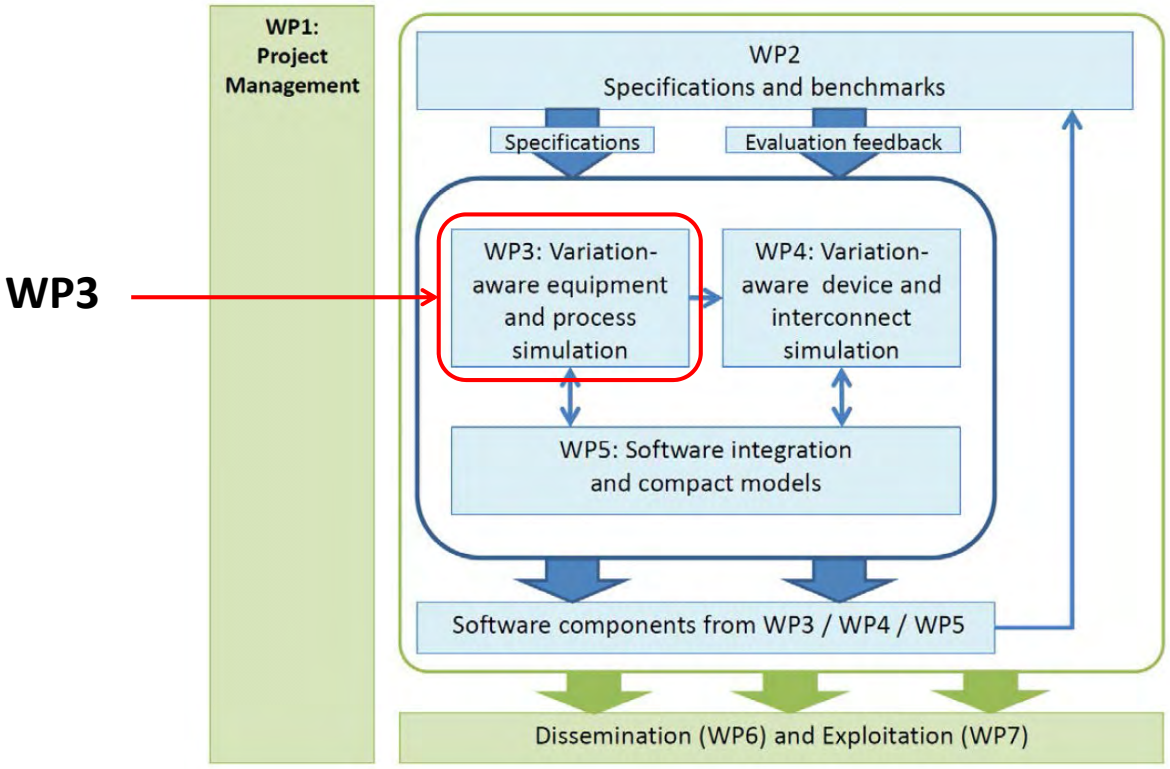
- For nanometer-scale devices, effects due to topography variations are important to consider, therefore the work on topography simulation within SUPERAID7 aims at:
  - Tight integration of the etching and deposition modules (DEP3D, ANETCH of Fraunhofer and ViennaTS of TU Wien) with background work on lithography simulation (using Dr.LiTHO of Fraunhofer) providing a unified frontend for topography simulation
  - Development of physical models for etching and deposition processes relevant for device and interconnect fabrication
  - Interfacing of feature-scale simulation with external equipment simulation modules
  - Integration of the topography modules with further process steps and device and interconnect simulation
  - Model calibration, verification, and benchmark support

Introduction – Goals and Strategy
State-of-the-art

- Individual modules for simulation of topography steps (lithography, etching, deposition) are available from academia and commercial vendors
  - The physical modeling level of the SUPERAID7 modules is comparable or ahead (the latter in particular for lithography simulation)
- The possibility to run the SUPERAID7 topography modules in an integrated environment and to provide the structures to device and interconnect simulation is – to our knowledge – beyond state-of-the-art

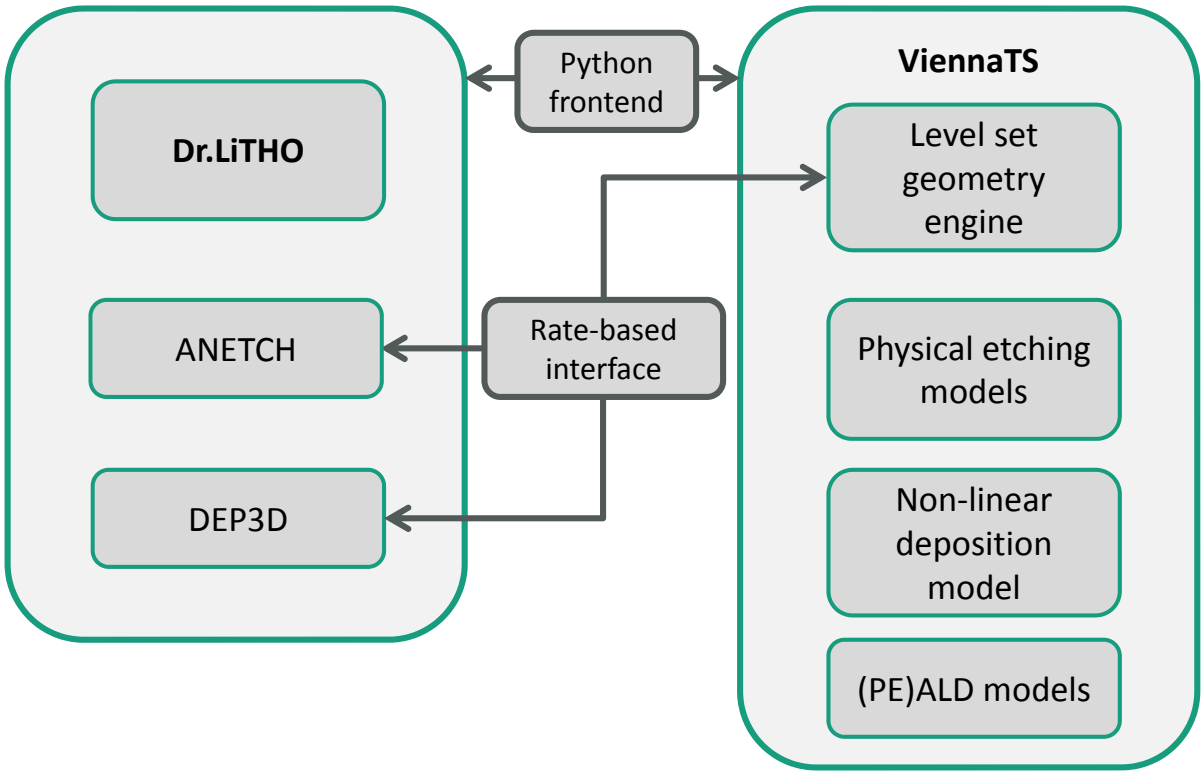
  This allows the end-user
  - to address advanced topography processes
  - to use the results in the context of various applications by running device and interconnect simulations

Introduction – Project Context



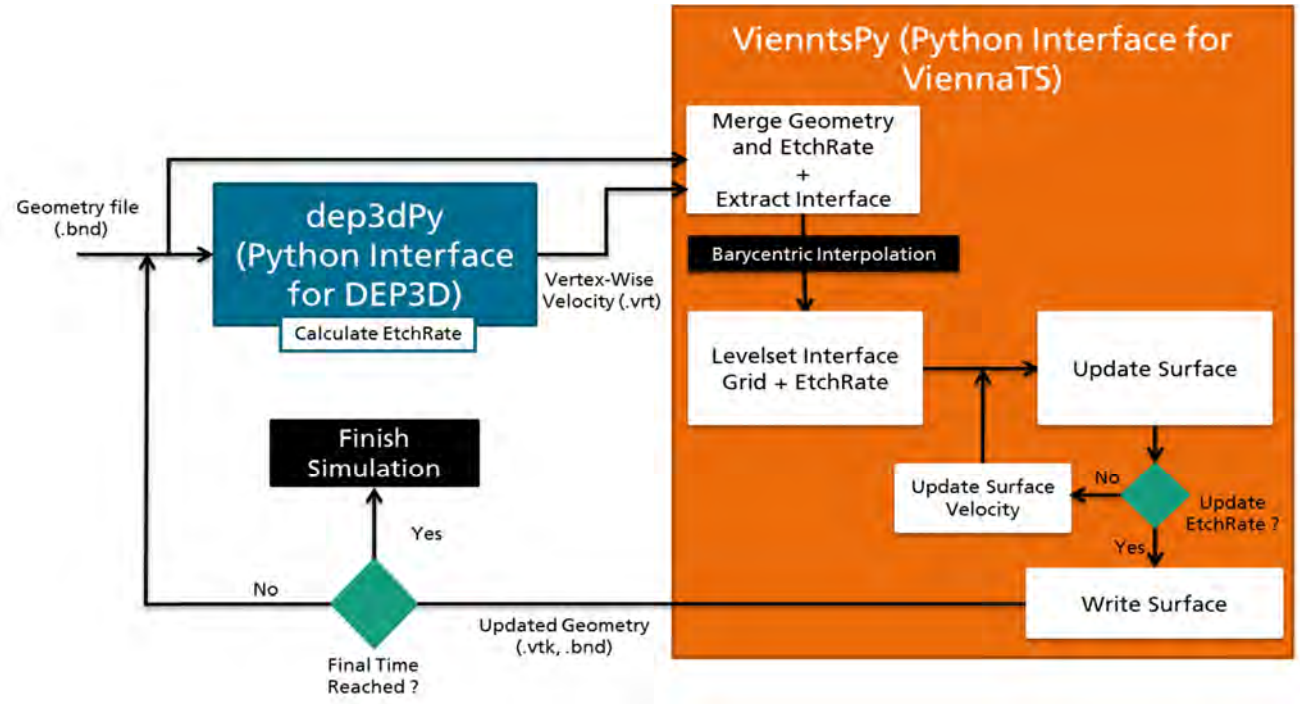
Software Integration

Topography Simulation Modules and their Interaction



Software Integration

Example: Integration of DEP3D from IISB with ViennaTS



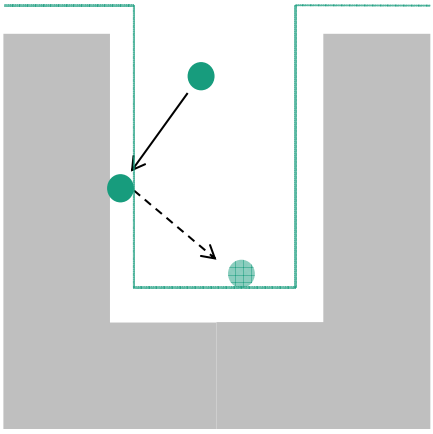
Simulation Models

Deposition and Etching Models

- Deposition models are available for
  - general non-linear multiple-species deposition, model is able to reproduce a plenum of processes driven by multiple species by adjusting a few parameters
  - sputter deposition, chemical vapor deposition (CVD), ionized metal plasma deposition, plasma-enhanced CVD, and superconformal deposition
  - transient simulation of atomic layer deposition (ALD) and plasma-enhanced ALD (PEALD)
- Etching models are available for etching of different materials
  - such as (poly)silicon, silicon oxide, TiN, HfO_2
  - with different chemistries, such as Cl_2, HBr, SF_6, CH_2F_2, C_xH_y, CF_x, BCl_3

Simulation Models
Example: Modeling of Non-conformal Oxide Deposition

- Reactive molecules arrive from the reactor and hit the structure surface. The following can happen:
  - Reaction → contribution to layer growth
    or
  - Re-emission → molecule can reach other positions
- Simulation approach:
  - Quasi steady-state with slowly varying local fluxes
  - Solving for local rates R_i, using surface discretization



$$\pi R_i - \sum_{i \neq j} T_{ij} R_j = \pi - \frac{1}{1 - s_c} \sum_{i \neq j} T_{ij} \quad i = 1 \ldots N$$

← System of N linear equations

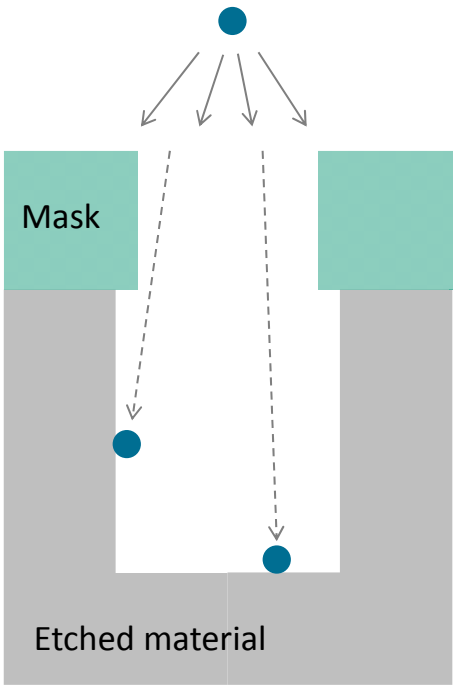
- Layer profile depends on reaction probability s_c and the geometry, e.g., the aspect ratio of a contact hole

Simulation Models
Example: Physical Etching Simulation

Simple model (view-angle dependent etching), can be applied, e.g., to sputter etching:

- Rate-determining species, e.g., ion, with given angular distribution and etching law $r(\theta_{loc})$
- Local rate $r(\boldsymbol{x})$ is determined by integrating the flux $\phi(\theta, \varphi)$, taking into account shadowing by the structure leading to a restriction of the solid angle to Ω_{free}:

$$r(\vec{x}) \sim \int_{\Omega_{free}} r(\theta_{loc})\, \phi(\theta, \varphi)\, d\Omega$$

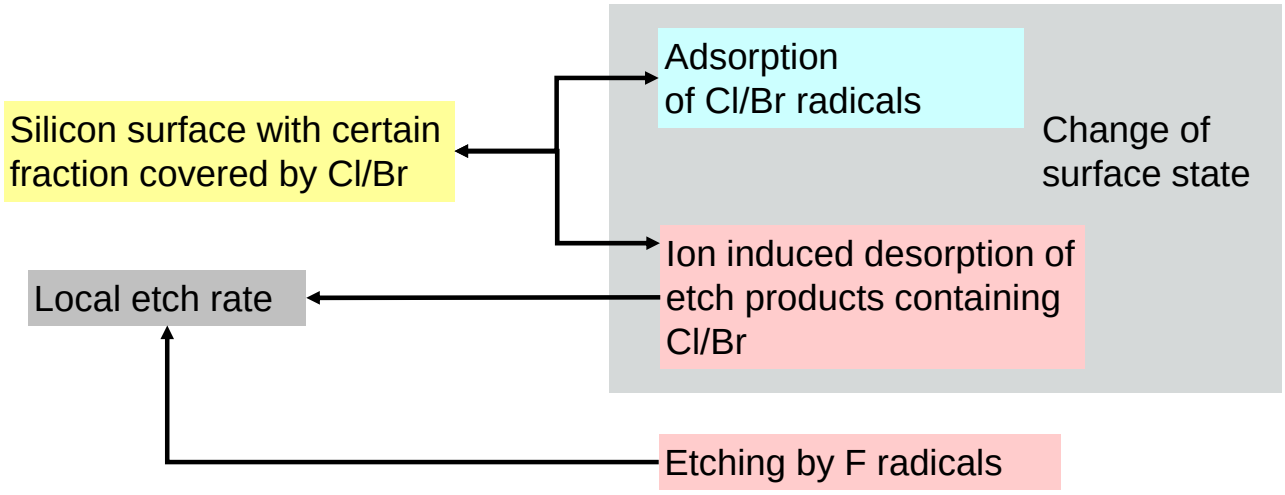


Complex etching models consider multiple species and laws for interaction with the structure, e.g., for reactive ion etching

Simulation Models

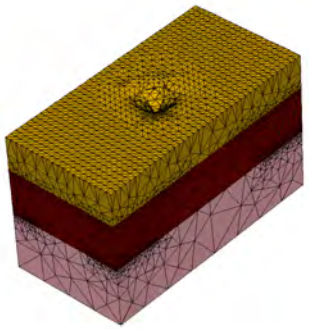
Example: Reactive Ion Etching of Silicon or Polysilicon

- Etching process in a plasma based on Cl_2, HBr, CF_4 chemistry

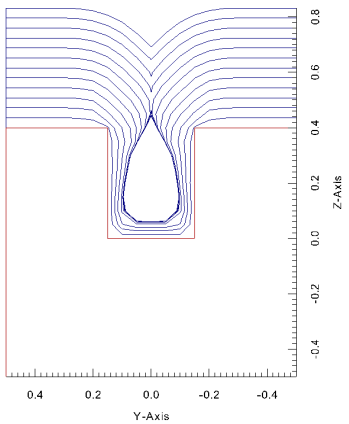


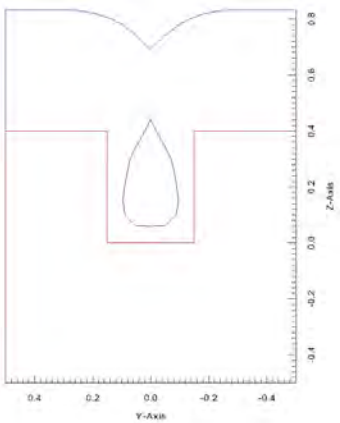
Simulation Examples

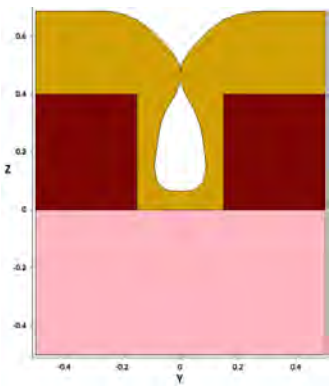
Low-temperature Oxide Deposition with Void Formation



- Simulation of low-temperature oxide (LTO) deposition with the LPCVD (low-pressure chemical vapor deposition) model of DEP3D using a sticking coefficient $s_c = 0.2$



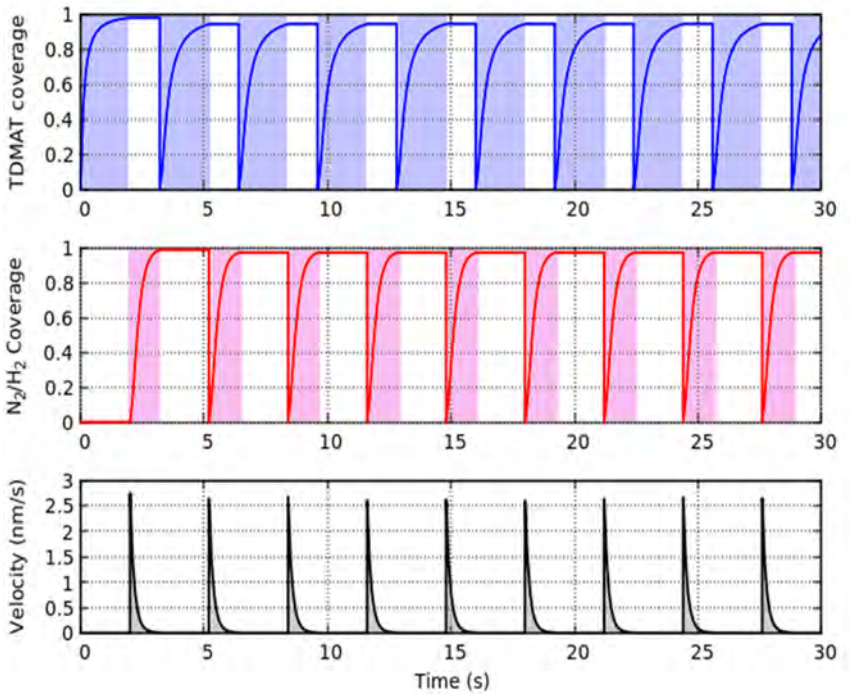




Simulation Examples

Plasma-enhanced Atomic Layer Deposition (PEALD)

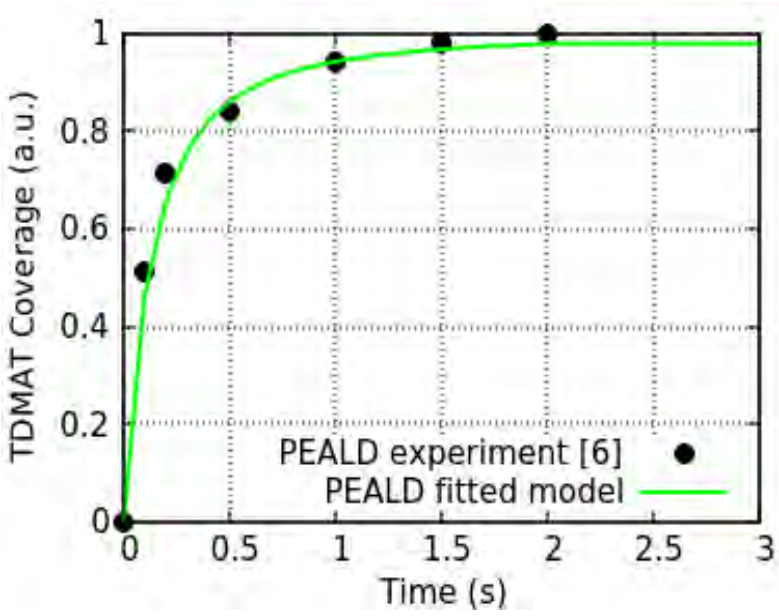
- TiN PEALD using TDMAT and N_2/H_2 plasma is modeled based on an adaptation of a model for conventional ALD
- The film growth (deposition of a single layer of TiN) takes place only during the H_2-N_2 plasma step



Simulation Examples

Plasma-enhanced Atomic Layer Deposition (PEALD)

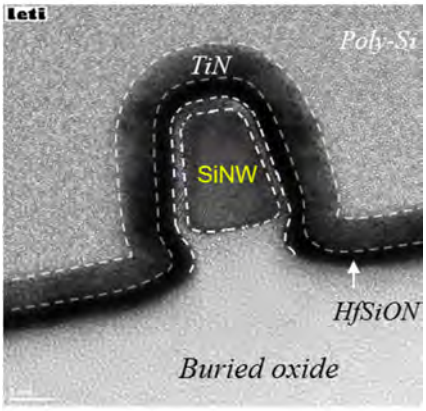
- We used the experimental data from literature to find the best fitting values for the model parameters
- Adjusting the fitting parameters results in a PEALD model, which fits well with the measurements

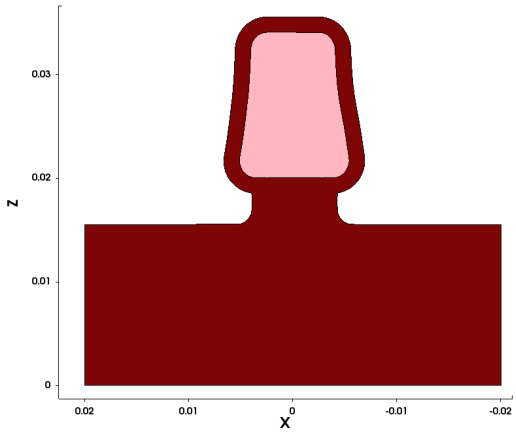


Simulation Examples

Simulation of Fin Etching

- Fin etching is carried out using a dry etching process with HBr, Cl_2, and oxygen chemistry
- Using the corresponding model in ANETCH, the profiles can be reproduced using typical values for the fluxes of ions and neutrals and model parameters from literature
- Extension of the model includes the link to equipment simulation for obtaining boundary conditions for fluxes of ions and neutrals

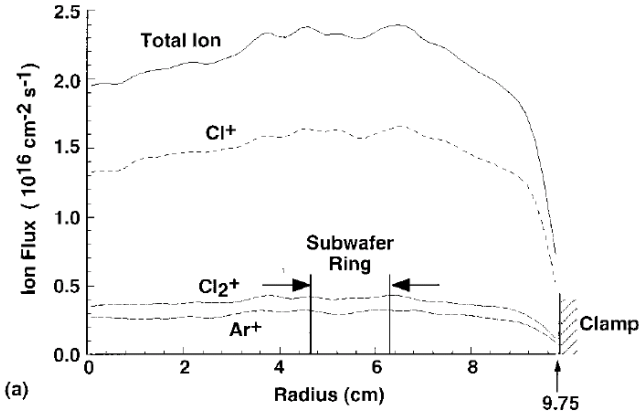


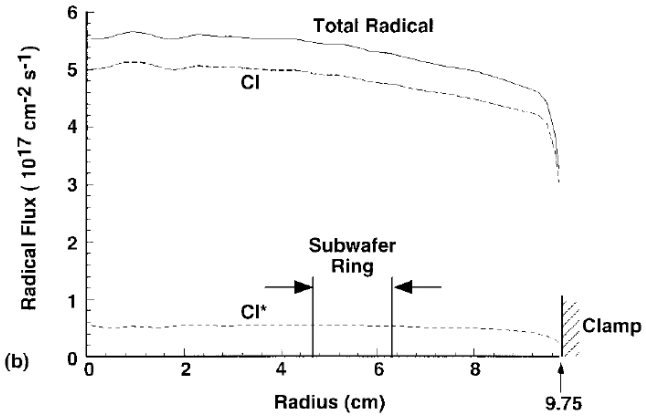


Simulation Examples

Simulation of Fin Etching with Coupling to Equipment Data (1)

Equipment simulation results (Hoekstra et al., 1997)





Ion flux

Neutral flux

Relative change (center / Radius = 4 cm / Radius = 8 cm)

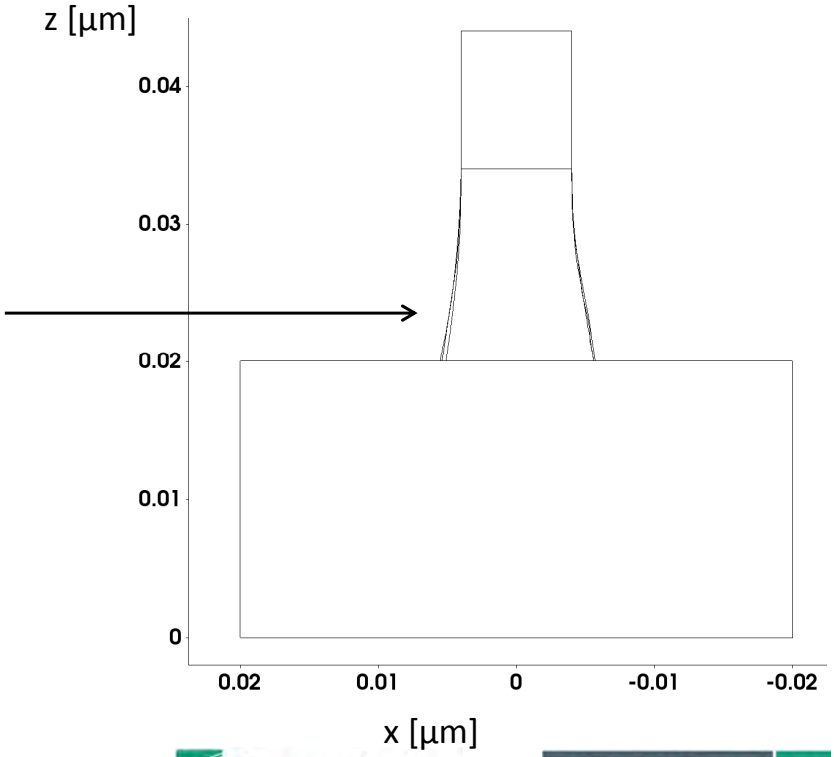
0 % / + 17 % / + 6 %

0 % / 0 % / - 11 %

Simulation Examples

Simulation of Fin Etching with Coupling to Equipment Data (2)

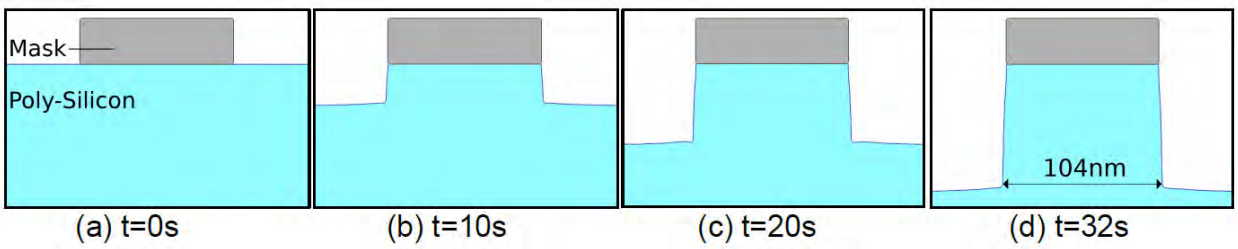
- Ratio of etch rates center / 4 cm / 8 cm: 52 / 55 / 50 (relative units)
- Due to overetching, the resulting fin profiles are only slightly modified



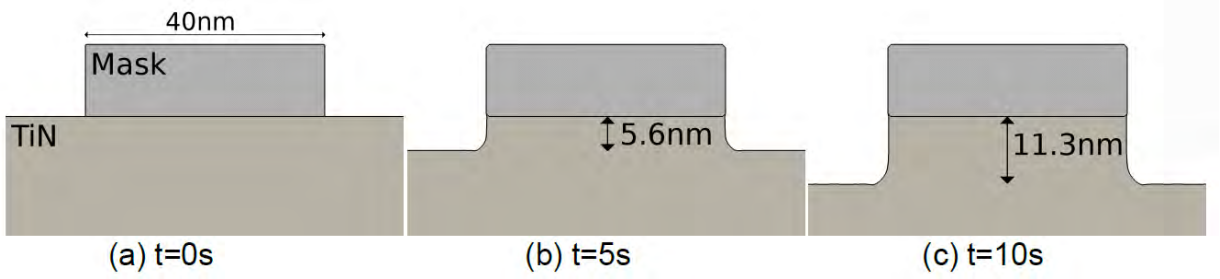
Simulation Examples

Simulation of Gate Stack Patterning (1)

- Sample simulation of poly-silicon etching in a SF_6/CH_2F_2 plasma with a bias power set to 75 W and a SF_6 to CH_2F_2 ratio of 0.45:

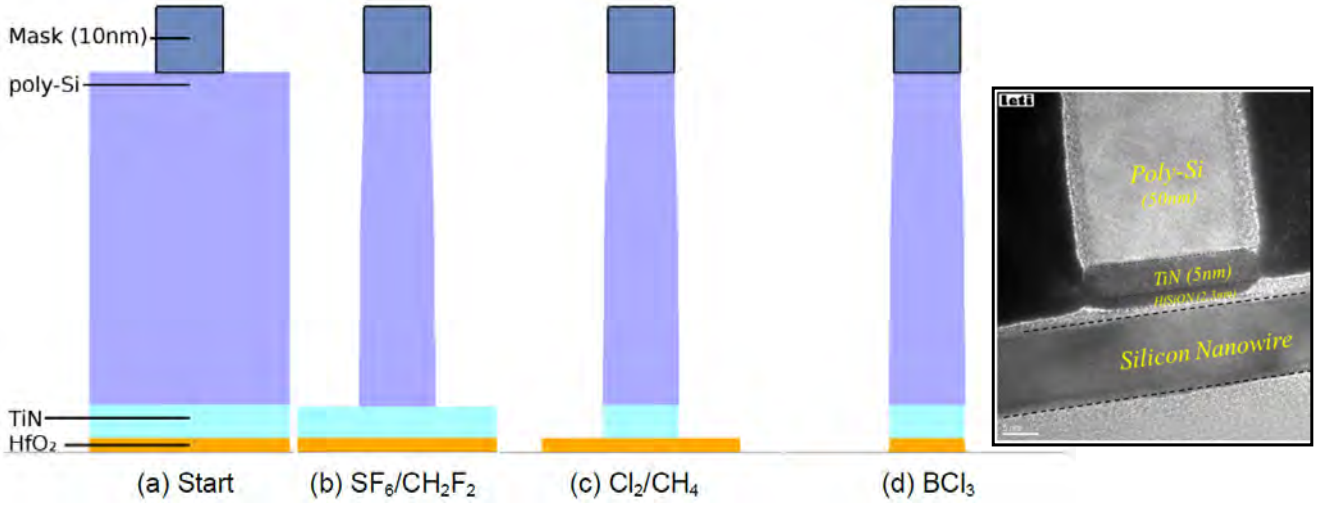


- Sample simulation of titanium nitride etching in a Cl_2/CH_4 plasma:



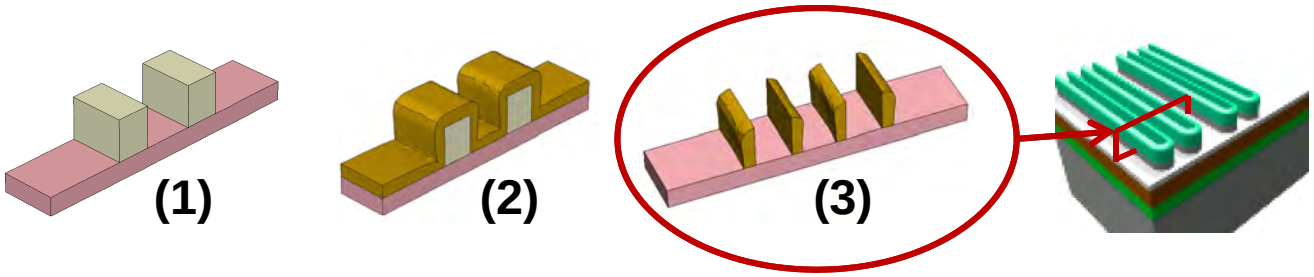
Simulation Examples
Simulation of Gate Stack Patterning (2)

- Result of the simulation sequence used to etch through the gate stack of HfO_2 (1.9 nm), TiN (5 nm), and poly-Si (50 nm) with a 10 nm mask:



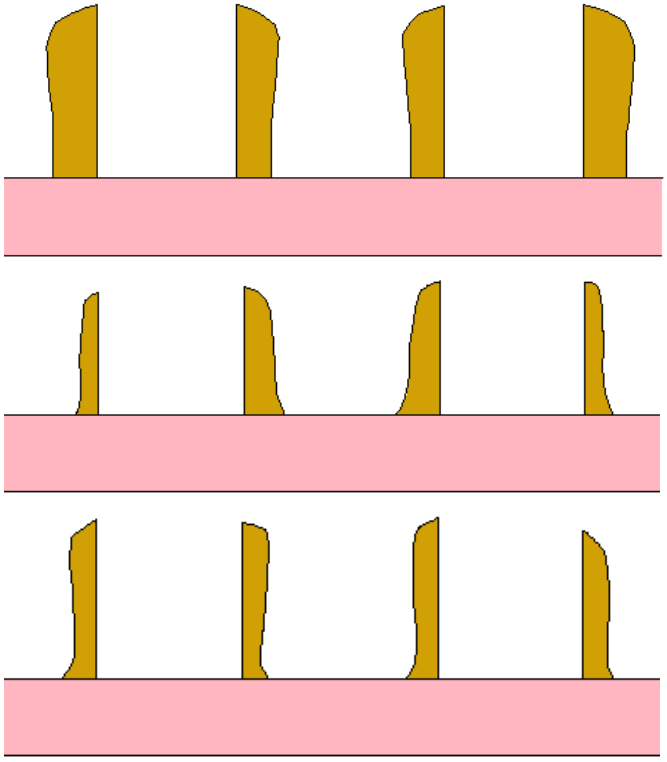
Simulation Examples
Self-aligned Double Patterning (1)

- Carbon lines are created using CD values from a lithography model (1)
- CVD oxide is deposited (2)
- and etched back to form the spacers after carbon line removal (3)



Simulation Examples

Self-aligned Double Patterning (2)



- Non-conformal deposition followed by perfectly anisotropic etching
- Conformal deposition followed by chemical dry etching
- Non-conformal deposition followed by chemical dry etching

Conclusions and Outlook

- The topography modules allow the integrated simulation of lithography, etching, and deposition
  - The software provides integration routines for the Fraunhofer and TU Wien tools, based on a Python frontend and a rate-based interface between ANETCH, DEP3D and the ViennaTS level set module
  - The integration is extended by a Geometry Engine Python Package which provides additional functions
- The data exchange with electrical simulation of devices and interconnects is possible via file exchange
- The modules provide a large variety of physical models and capabilities for structure emulation
  - They have been applied to the SUPERAID7 benchmarks cases
  - This will be extended, particularly including equipment simulation, and using further experimental data, e.g., from the Industrial and Scientific Advisory Board

Physical models for nanowire device simulation

Dr. Vihar Georgiev, University of Glasgow, Glasgow, UK

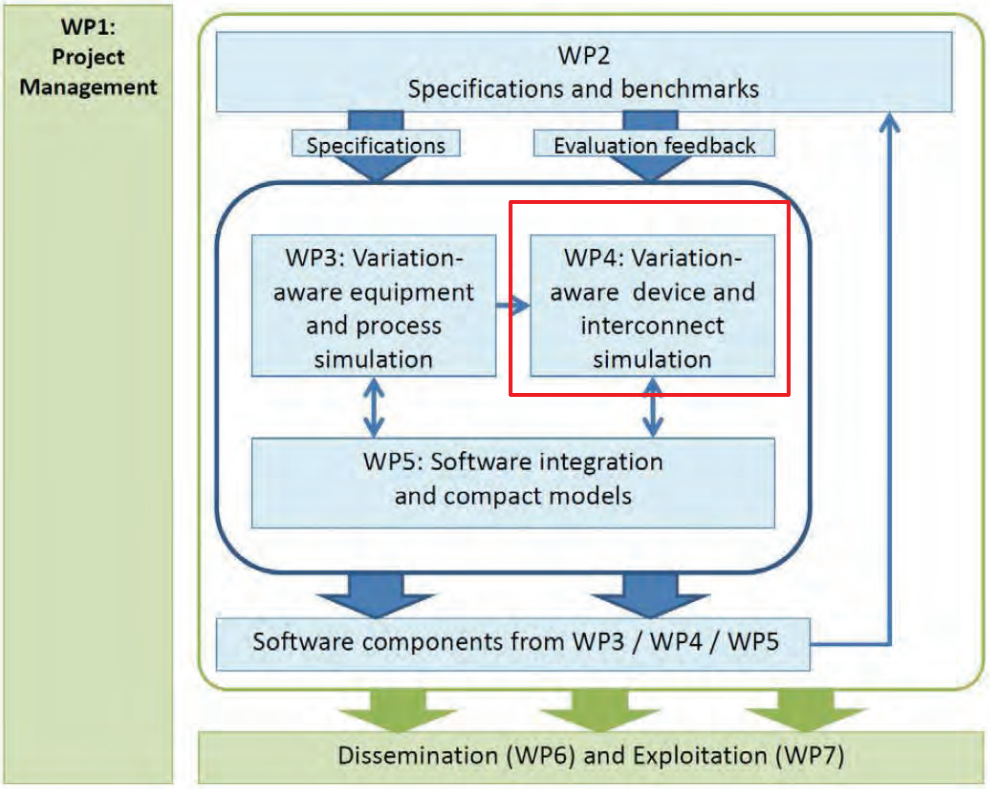
ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

Outline

- Introduction
  - Project flow and link between the Work Packages
- Physical models and methods
  - Drift Diffusion Method (DD)
  - Kubo-Greenwood
  - Non-Equilibrium Green’s Function (NEGF)
  - Wigner Monte Carlo
- Conclusions and outlook

Introduction - Project Context

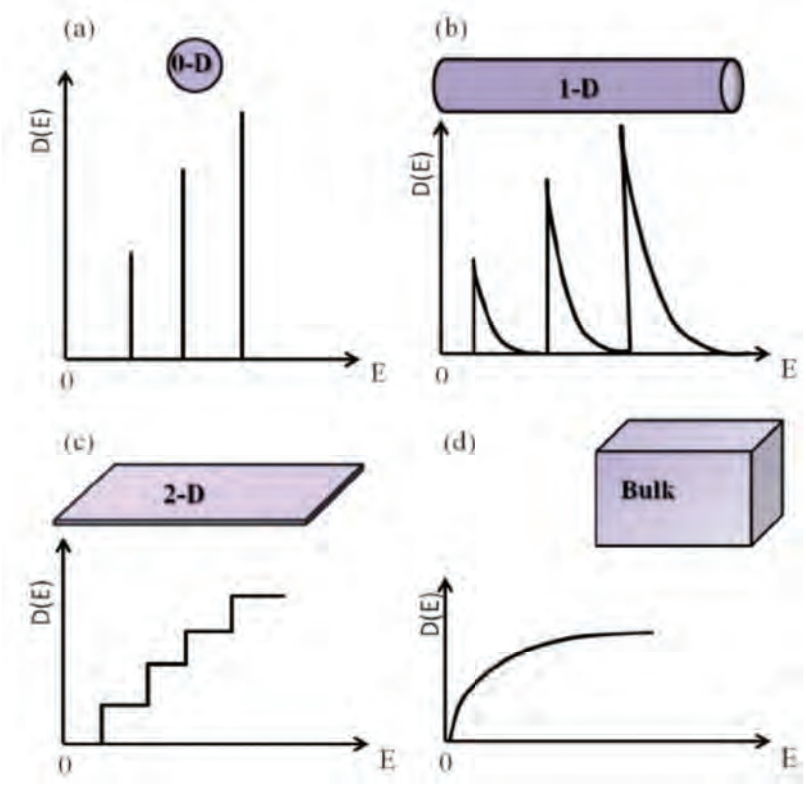


Introduction - Goals and Strategy of WP4

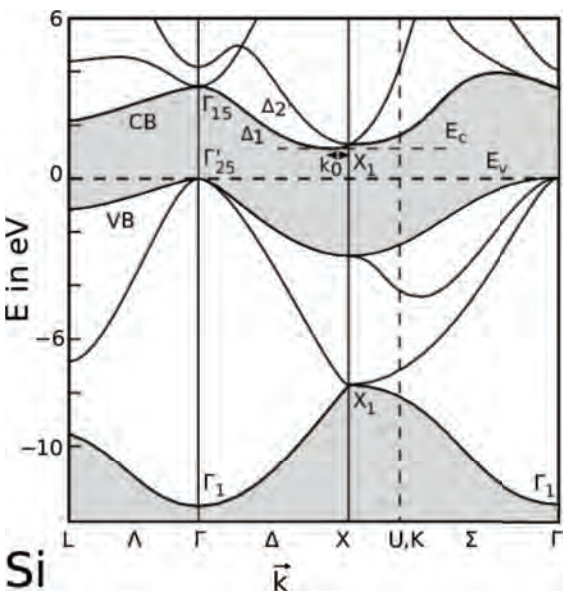
- The objective of this work package is to **enable device and advanced interconnect simulation tools** to deal with **realistic geometries including variability and process-induced variation**.

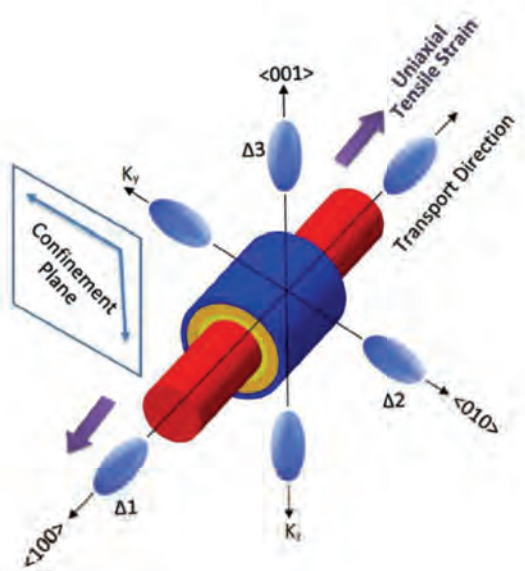
- **To develop and to implement refined physical models** which are needed for the **simulation of advanced More Moore devices like FinFETS and Nanowire Transistors**, especially when effects of ***confinement, quantum behaviour and charge granularity*** come into play. Interconnect models will be developed, which properly account for grain boundary and surface roughness effects on electron transport.

Introduction - Basic Physics



Introduction - Basic Physics



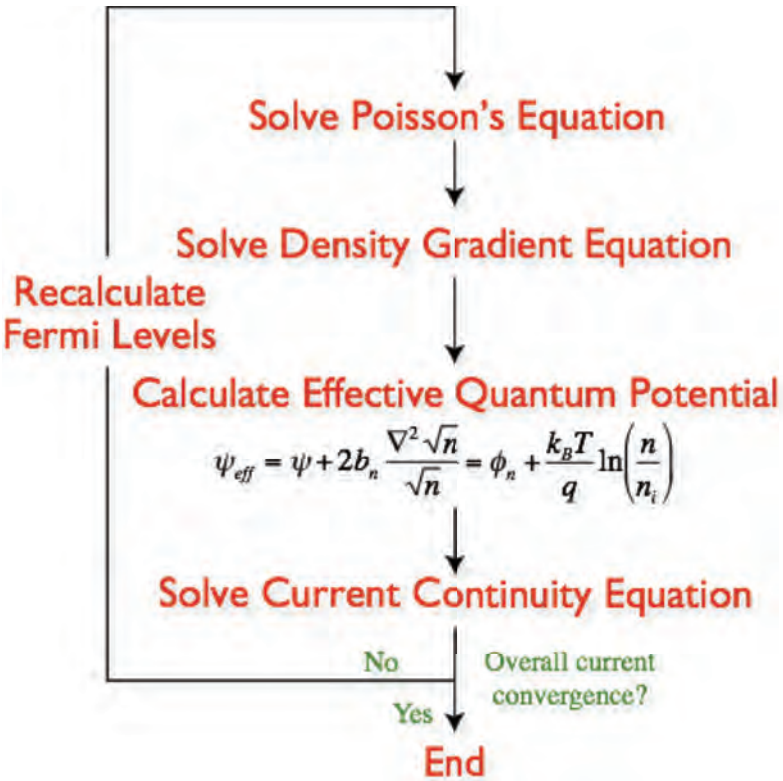


Conduction band consists of six energy ellipsoids (Δ) along the confinement plane and uniaxial tinsel strain.

Outline

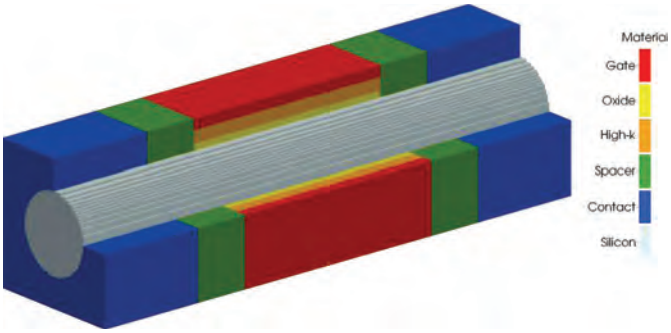
- Introduction
  - Project flow and link between the Work Packages
- Physical models and methods
  - **Drift Diffusion Method (DD)**
  - Kubo-Greenwood
  - Non-Equilibrium Green's Function (NEGF)
  - Wigner Monte Carlo
- Conclusions and outlook

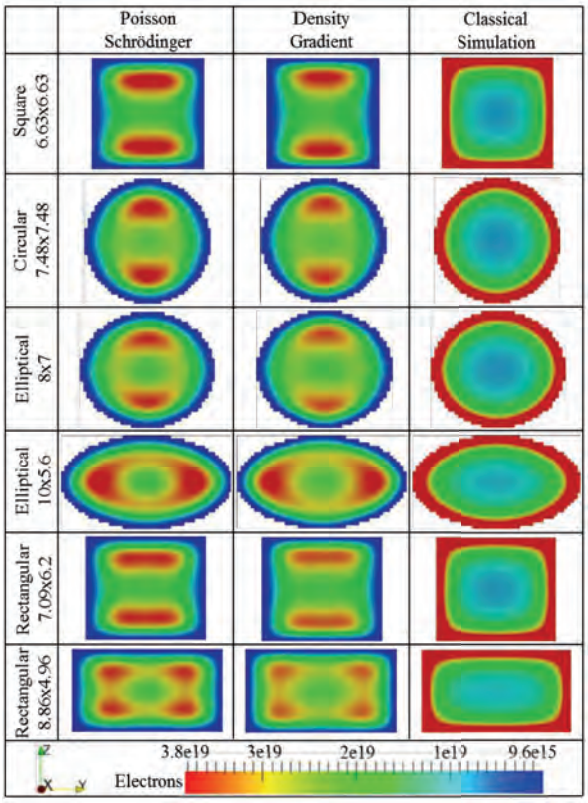
Physical Model - Drift Diffusion



Physical Model - Drift Diffusion

Parameters	Value
Gate length (nm)	18
Spacer thickness (nm)	5.0
S/D peak doping (cm^{-3})	2×10^{20}
Channel doping (cm^{-3})	10^{14}
Substrate orientation	(001)
Nanowire orientation	<110>, <100>
T_{oxide} (nm)	0.8

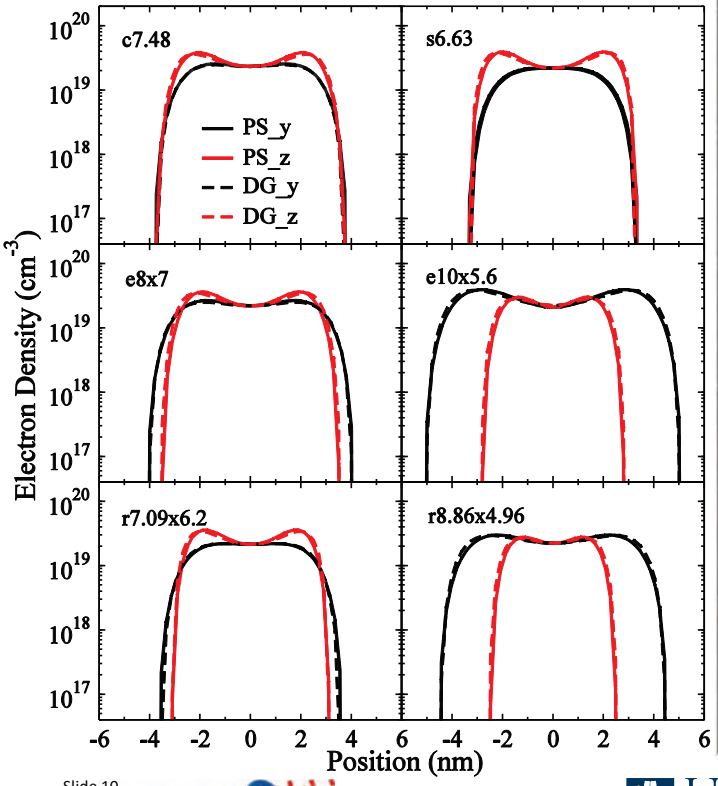


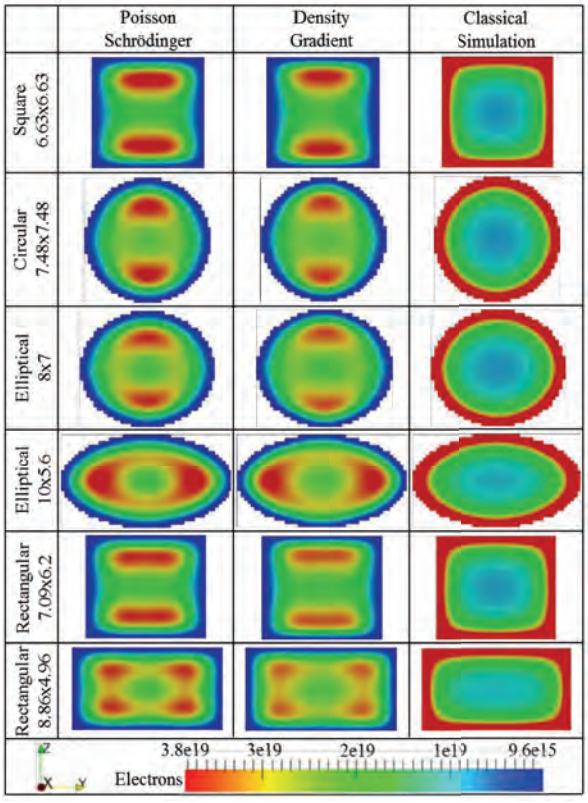


University of Glasgow

SUPERAID 7

Physical Model - Drift Diffusion





University of Glasgow

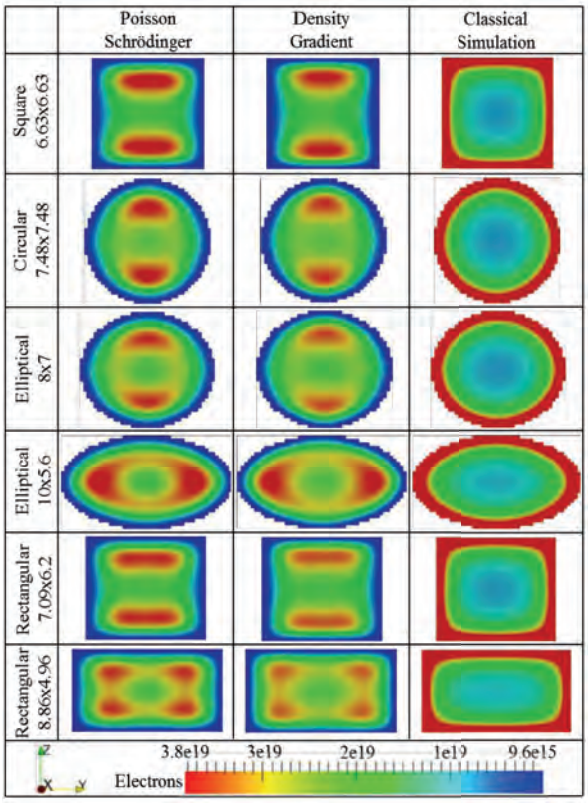
SUPERAID 7

Physical Model - Drift Diffusion

Device	Q_M (10^6/cm)	C_G (10^{-12}F/cm)	Q_M/C_G (10^{18}/F)
s6.63x6.63	7.208	5.915	1.219
c7.48x7.48	7.670	5.922	1.295
e8x7	8.229	6.171	1.334
e10x5.6	9.638	7.081	1.361
r7.09x6.2	7.971	6.130	1.300
r8.86x4.96	9.104	6.746	1.350
e5.6x10	6.771	6.312	1.073

The change in **shape** can have > 20% impact on performance

The change in **orientation** can have > 30% impact on performance

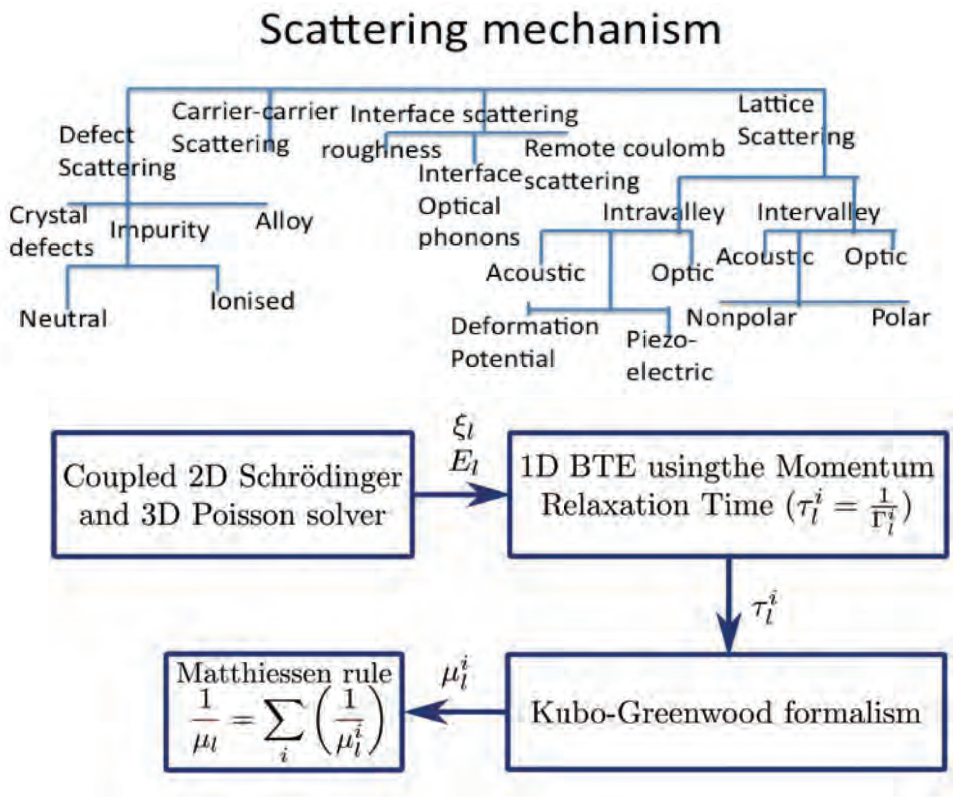


Outline

- Introduction
  - Project flow and link between the Work Packages
- Physical models and methods
  - Drift Diffusion Method (DD)
  - **Kubo-Greenwood**
  - Non-Equilibrium Green's Function (NEGF)
  - Wigner Monte Carlo
- Conclusions and outlook

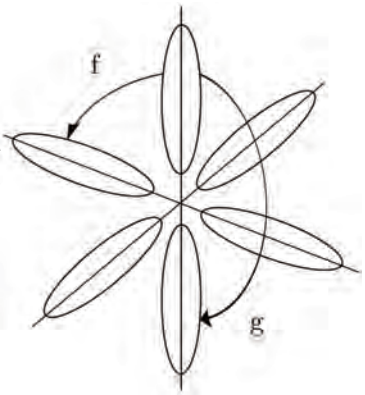
SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

Physical Model - Kubo-Greenwood

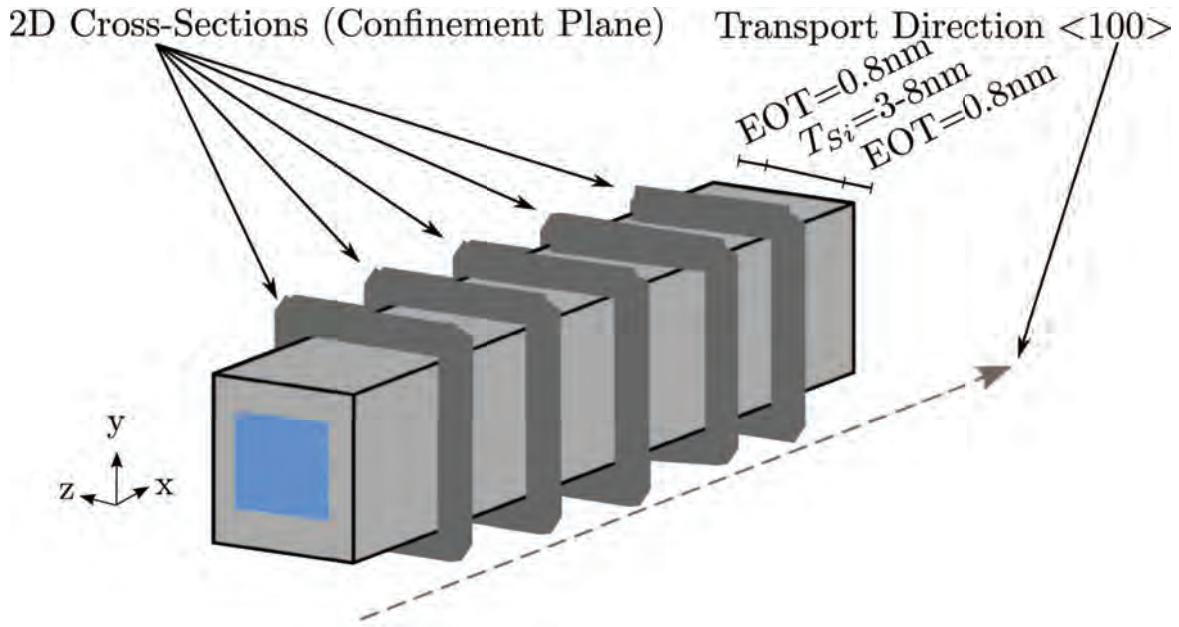


Physical Model - Kubo-Greenwood

- **Acoustic Phonon Scattering Mechanism**
  - Elastic and intra-valley transitions are only allowed
- **Optical Phonon Scattering Mechanism**
  - Inelastic mechanisms
  - The two different transitions among the six equivalent X minima of Si must be considered: g-type (intra-valley) and f-type (inter-valley) processes
- **Ionized Impurity Scattering Mechanism**
  - Elastic and intra-valley transitions are only allowed
  - Fixed uniform ionized impurity concentration: $n_0 = [10^{17} - 10^{19}]$ cm^{-3}



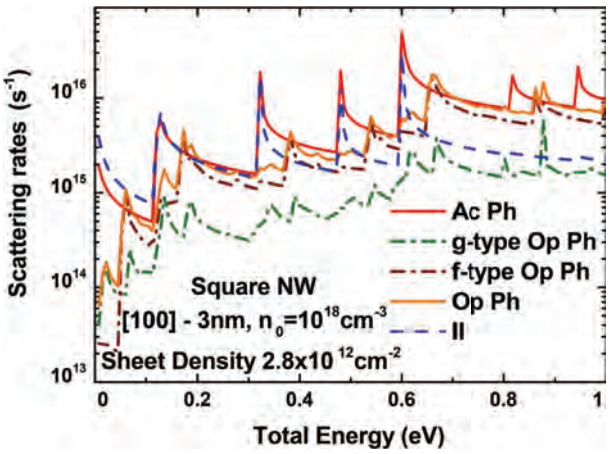
Physical Model - Kubo-Greenwood



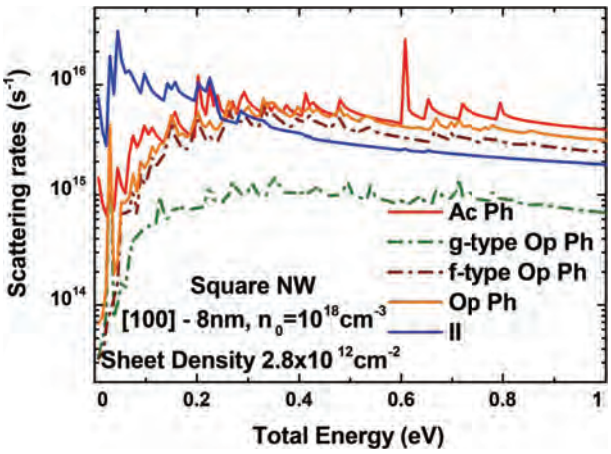
Silicon gate-all-around (GAA) nanowire transistor (NWT) in [100] orientation. Thickness (T) and width (W) range from T=W=3nm to T=W=8nm for square and circular cross-sectional shapes including 20 sub-bands.

Physical Model - Kubo-Greenwood

3 nm cross-section



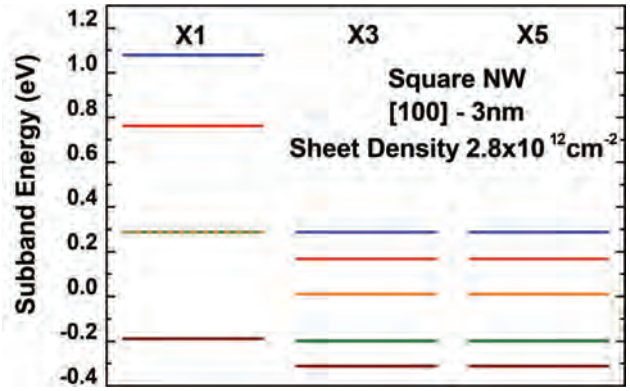
8 nm cross-section



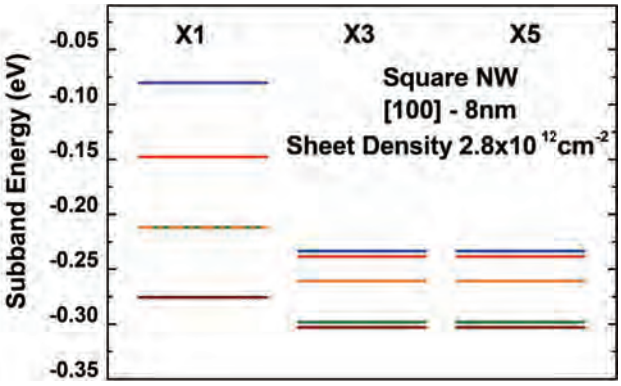
- The multisub-band effects in the scattering rates are generally more pronounced for smaller W.

Physical Model - Kubo-Greenwood

3 nm cross-section



8 nm cross-section



- The multisub-band effects in the scattering rates are generally more pronounced for smaller W.
- Higher energy difference between sub-bands minimizes the electron transitions.

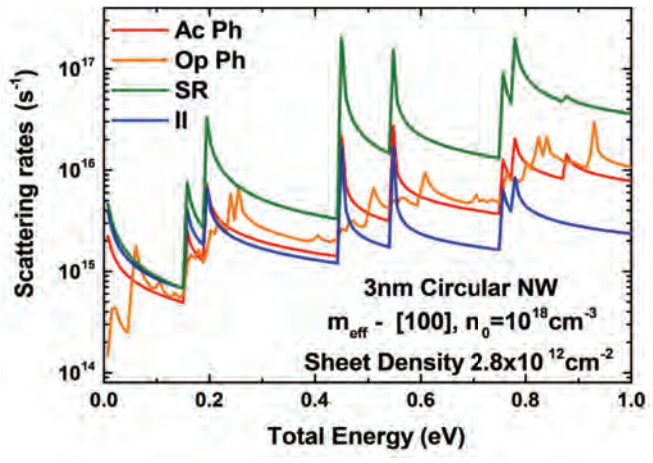
Physical Model - Kubo-Greenwood

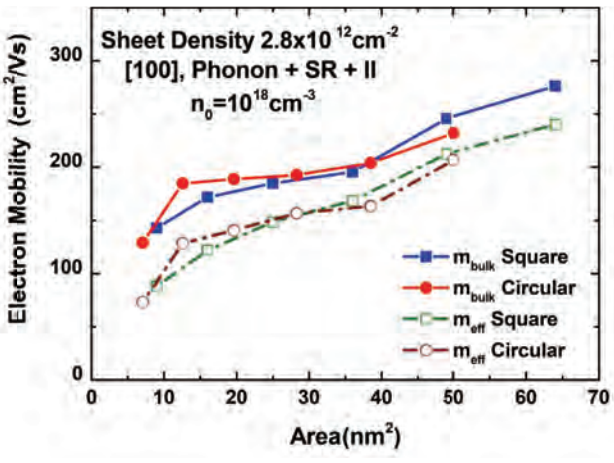
Scattering mechanisms:

- Elastic intra-valley acoustic phonon
- g- and f-type optical phonon
- Ionized impurity
- *Surface Roughness*

Si Nanowire transistors [100]:

- Effective mass calculation for each device
- Different width/height: 3nm – 8nm
- Different shape: square and circular

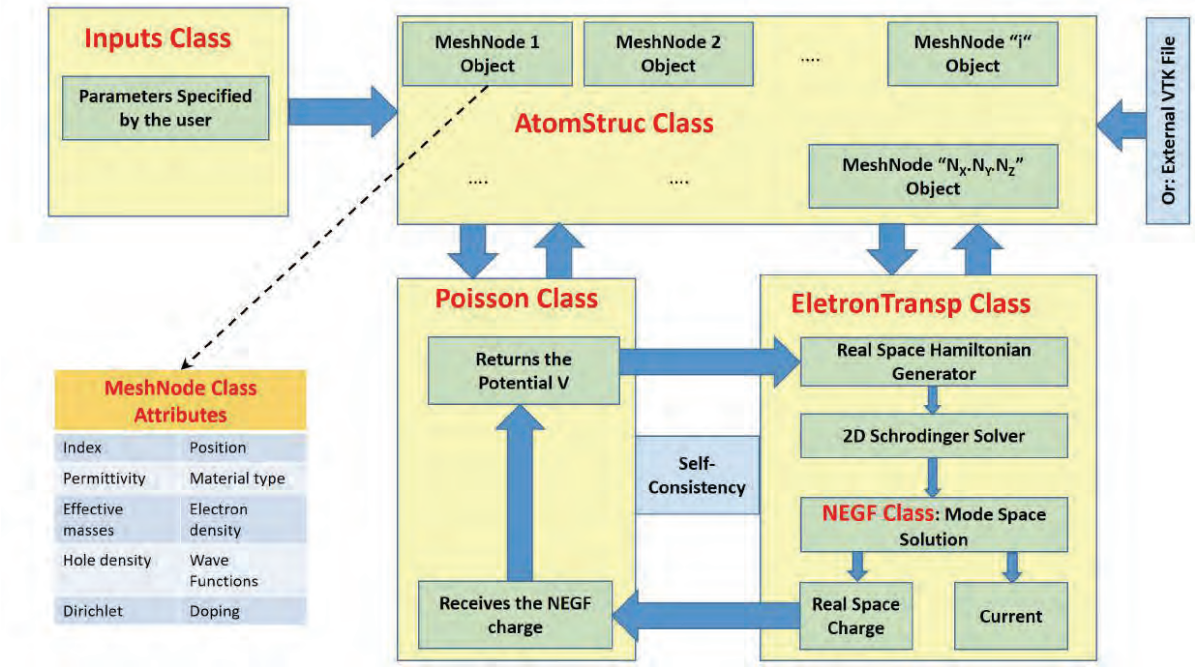




Outline

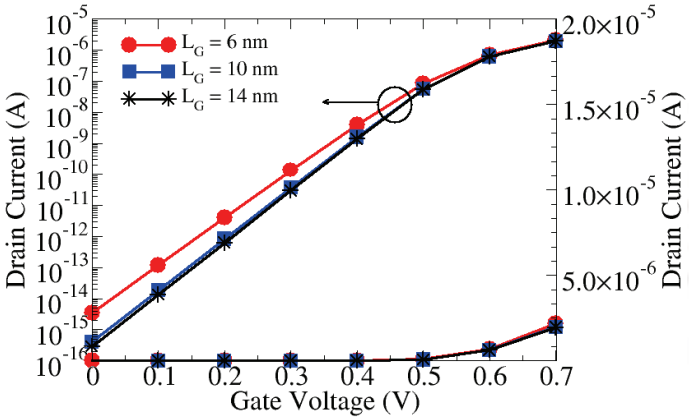
- Introduction
  - Project flow and link between the Work Packages
- Physical models and methods
  - Drift Diffusion Method (DD)
  - Physical Model - Kubo-Greenwood
  - **Non-Equilibrium Green's Function (NEGF)**
  - Wigner Monte Carlo
- Conclusions and outlook

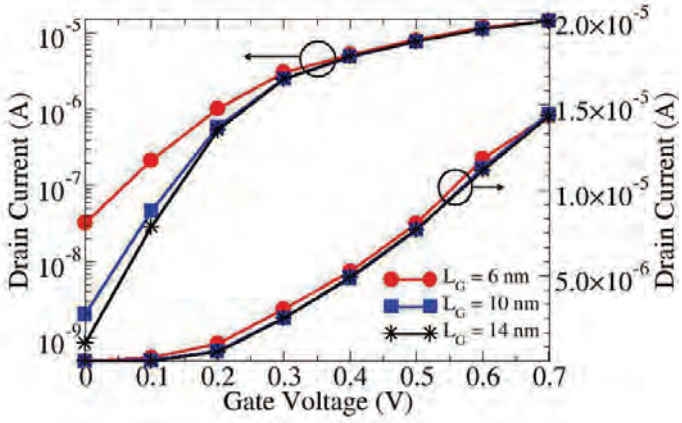
Physical Model - NEGF



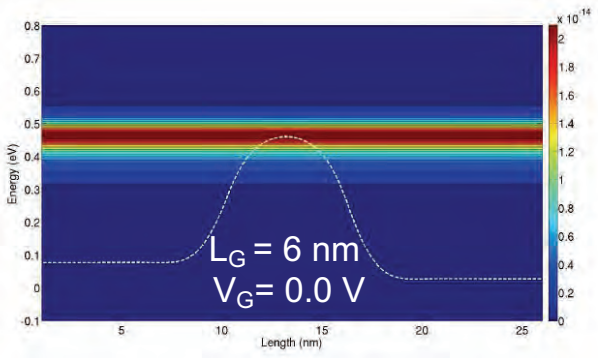
- Nano-Electronic Simulation Software (NESS) - University of Glasgow Device Simulator

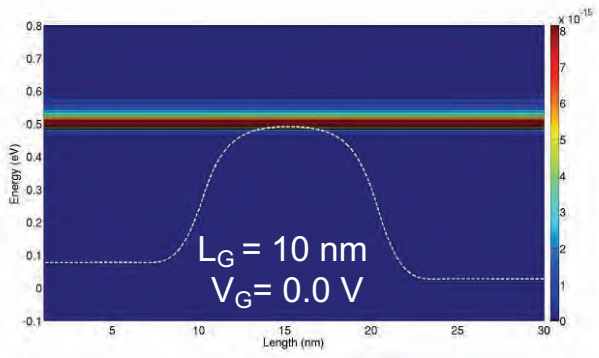
Physical Model - NEGF

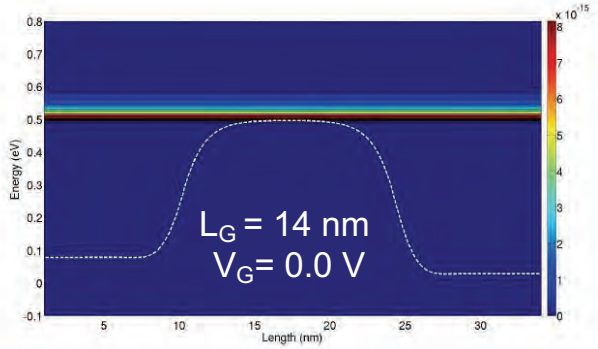




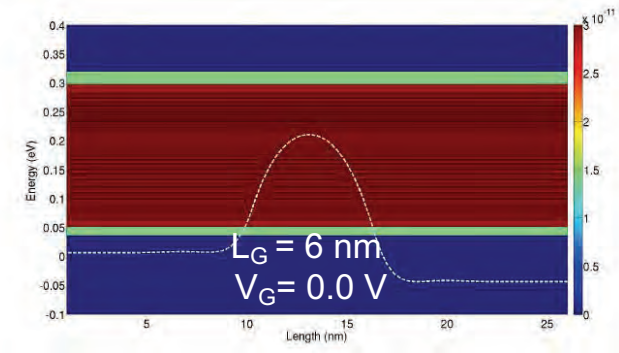
Physical Model - NEGF

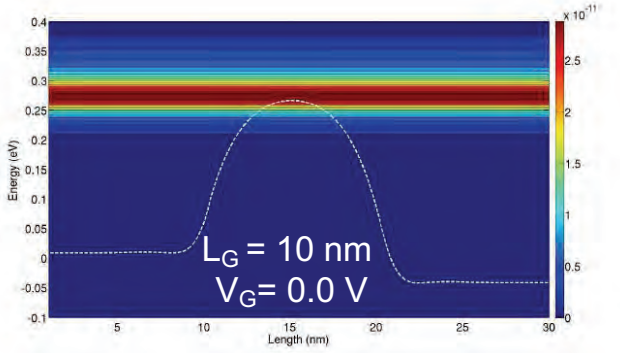


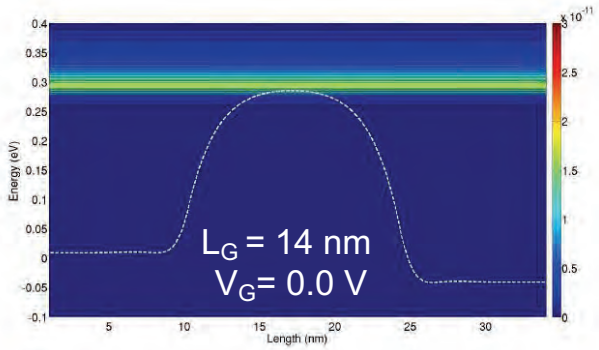




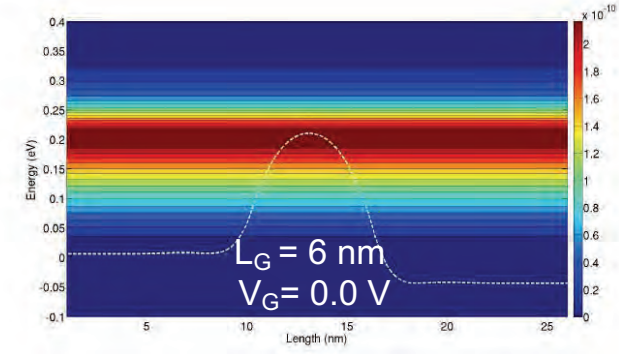
Physical Model - NEGF

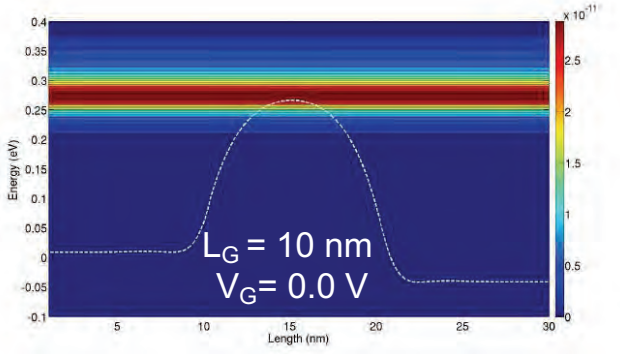


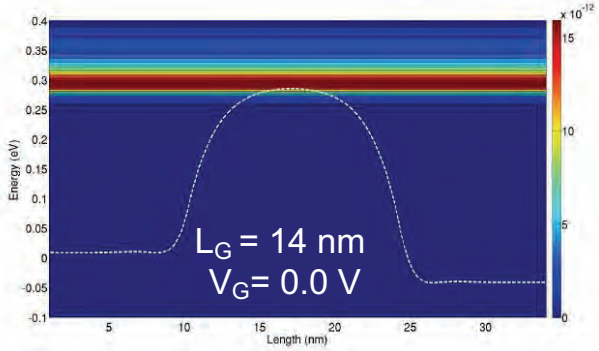


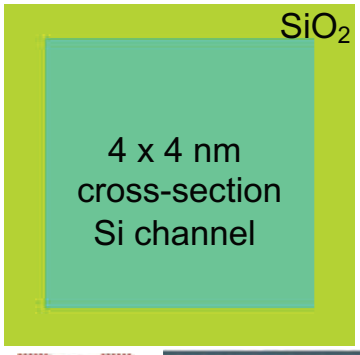


Physical Model - NEGF

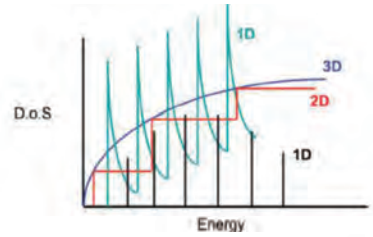


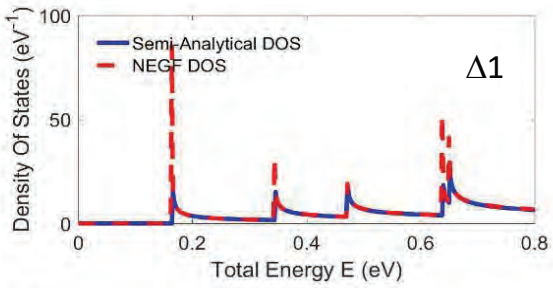


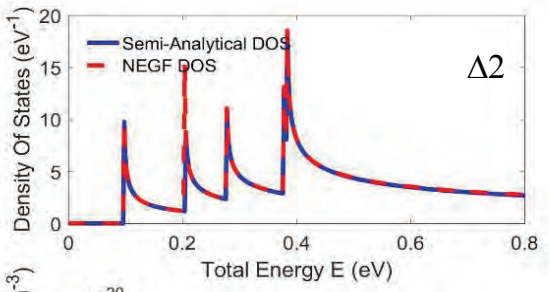


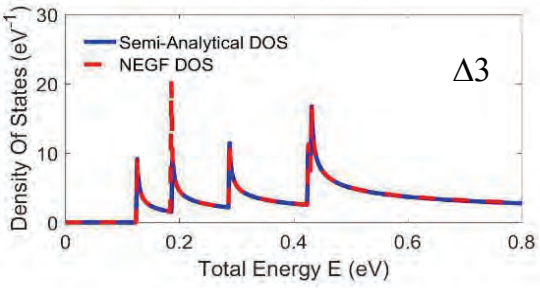


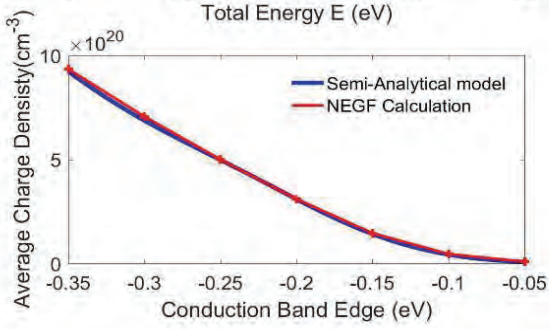
Physical Model - NEGF





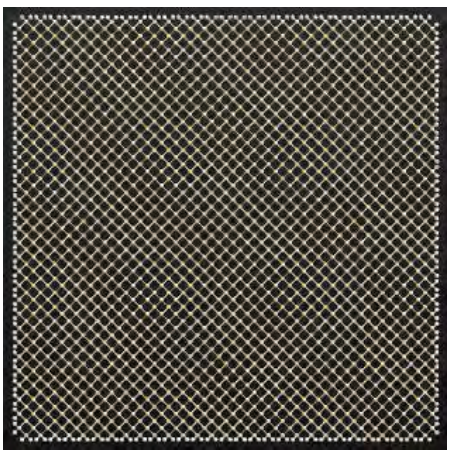






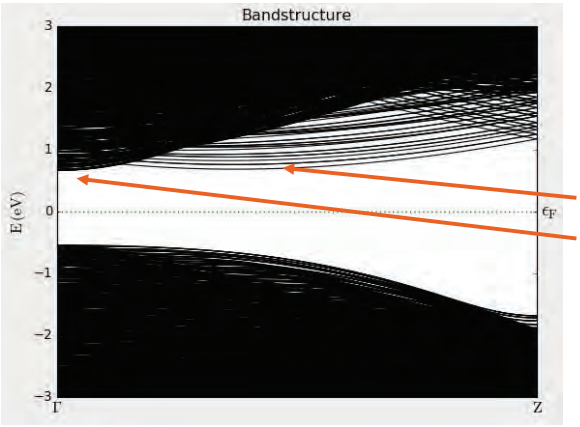
Physical Model - Band Structure

8nm Square Si NW



Simulation Method
- ***sp3d5s* tight binding*** with a Boykin parameter set
- No geometric optimization
- [100] transport direction

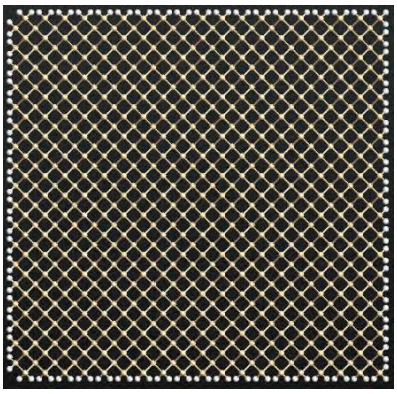
From reference [PRB 69 115201 (2004)]
- Effective mass of bulk Si: 0.891, 0.201 m_e (longitudinal, transverse)
- Bandgap: 1.131 eV



Effective mass (parabolic fit)
m_l: 0.900 m_e
m_t: 0.215 m_e

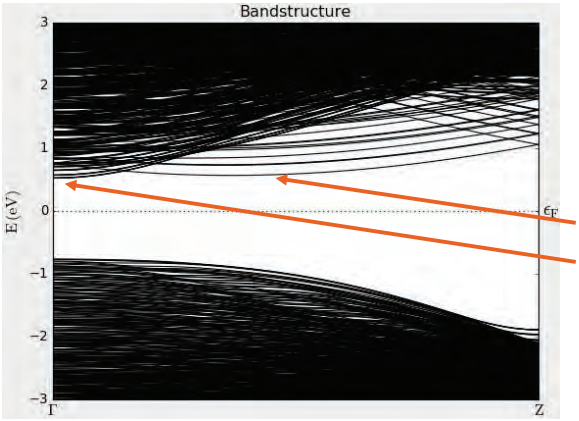
Physical Model - Band Structure

5nm Square Si NW



Simulation Method
- ***sp3d5s* tight binding*** with a Boykin parameter set
- No geometric optimization
- [100] transport direction

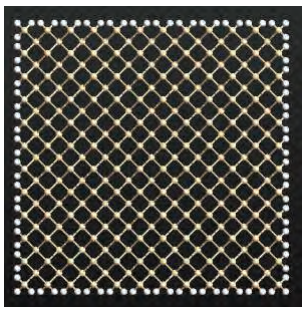
From reference [PRB 69 115201 (2004)]
- Effective mass of bulk Si: 0.891, 0.201 m_e (longitudinal, transverse)
- Bandgap: 1.131 eV



Effective mass (parabolic fit)
m_l: 0.917 m_e
m_t: 0.231 m_e

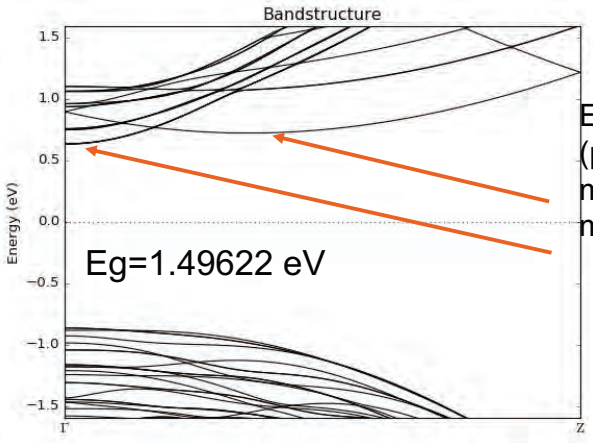
Physical Model - Band Structure

3nm Square Si NW



Simulation Method
- ***sp3d5s* tight binding*** with a Boykin parameter set
- No geometric optimization
- [100] transport direction

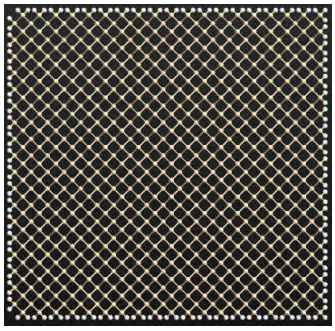
From reference [PRB 69 115201 (2004)]
- Effective mass of bulk Si: 0.891, 0.201 m_e (longitudinal, transverse)
- Bandgap: 1.131 eV

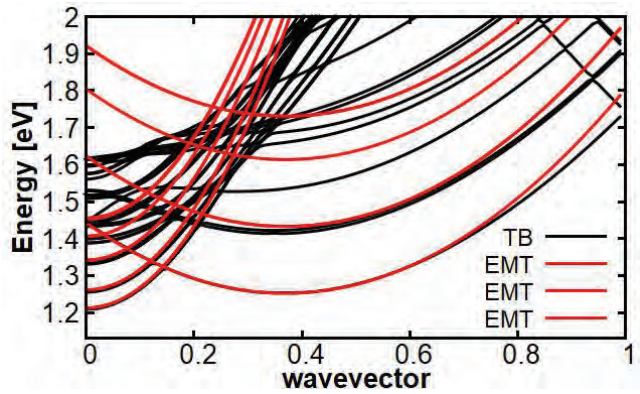


Effective mass (parabolic fit)
m_l: 0.951 m_e
m_t: 0.268 m_e

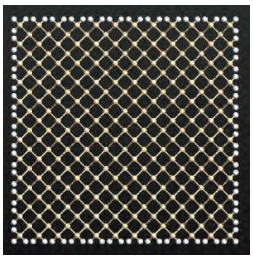
Physical Model - Band Structure

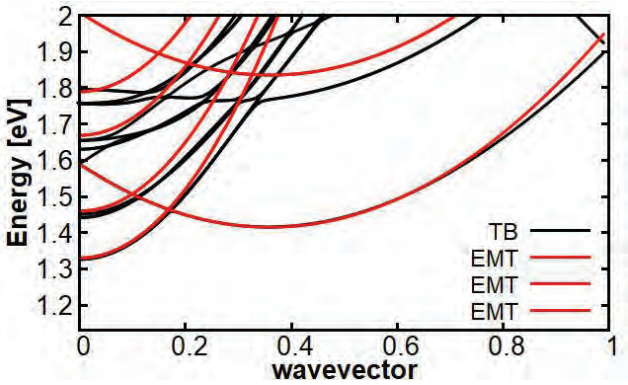
5nm Square Si NW



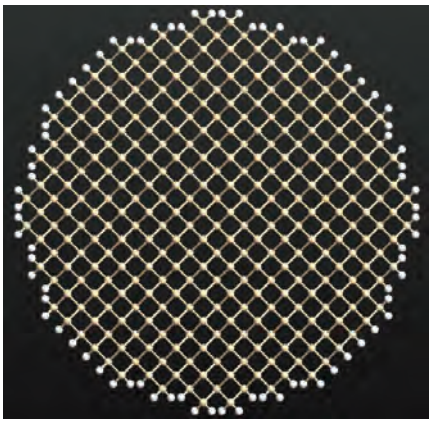


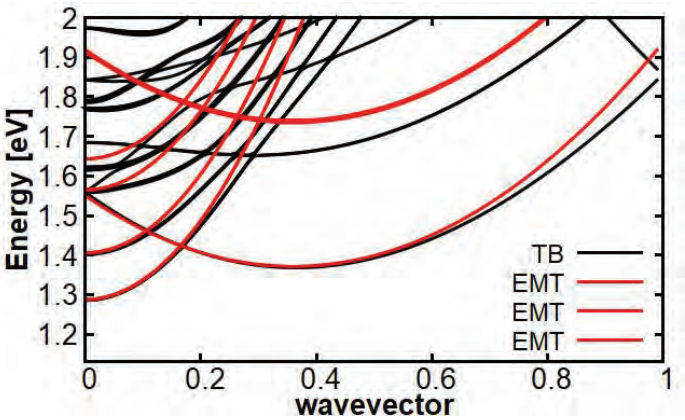
3nm Square Si NW





Physical Model - Band Structure (Task 4.1.4)



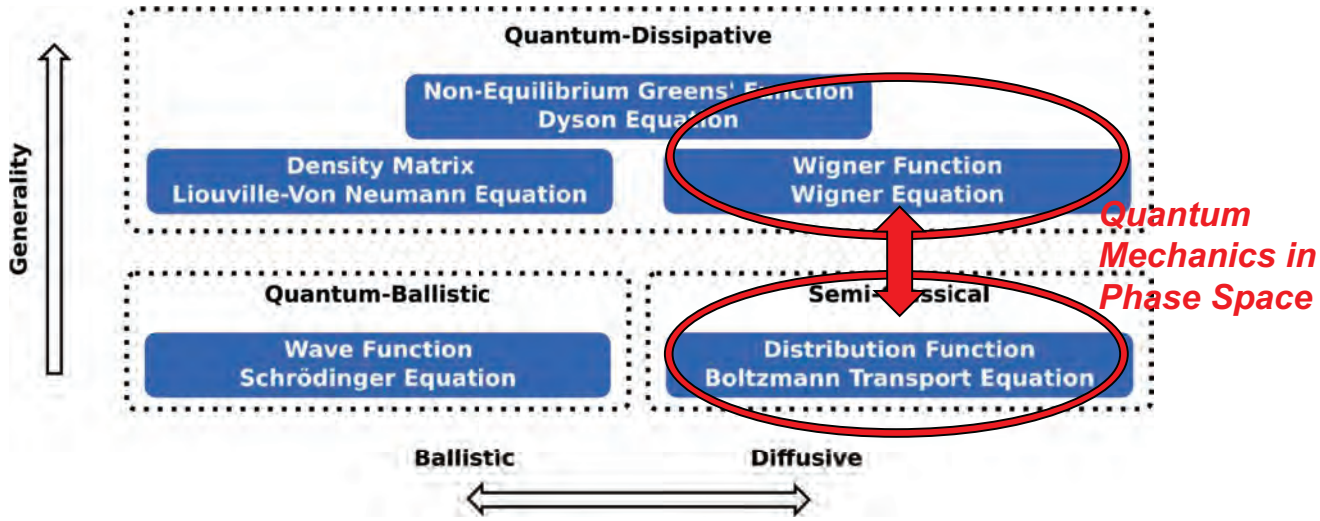


Atomic structure of Si NW (3.82 nm)

Outline

- Introduction
  - Project flow and link between the Work Packages
- Physical models and methods
  - Drift Diffusion Method (DD)
  - Kibo-Greenwood
  - Non-Equilibrium Green's Function (NEGF)
  - **Wigner Monte Carlo**
- Conclusions and outlook

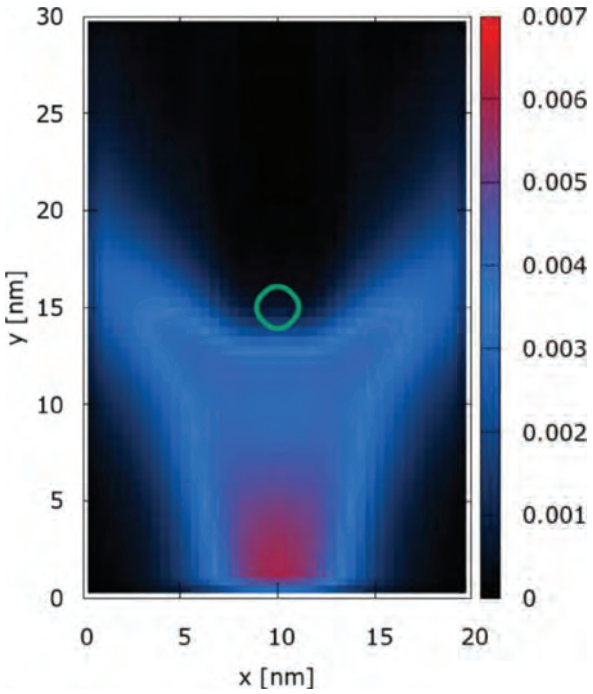
Physical Model - Wigner MC



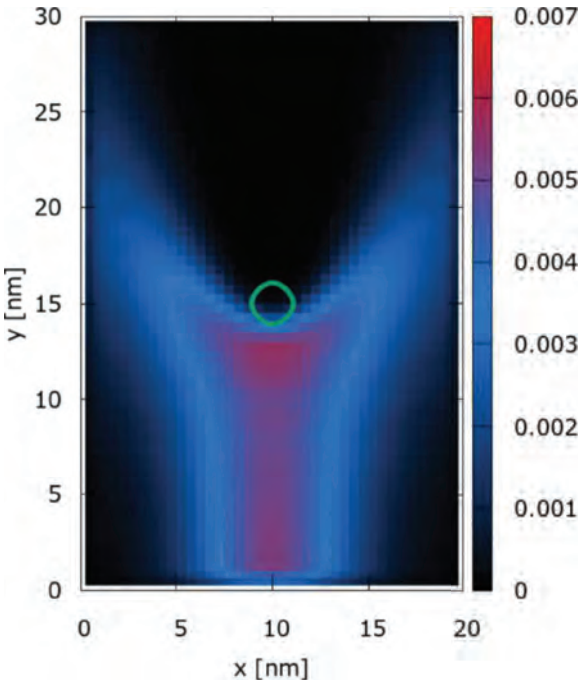
Signed particle **approach supports switching between**

- **Quantum particle evolution: Wigner transport**
- **Classical particle evolution: Boltzmann transport**

Physical Model - Wigner MC

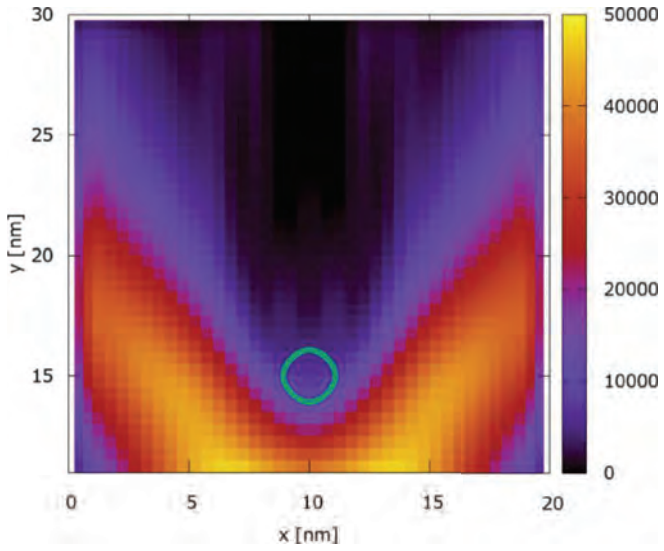


Quantum electron density [a.u.]

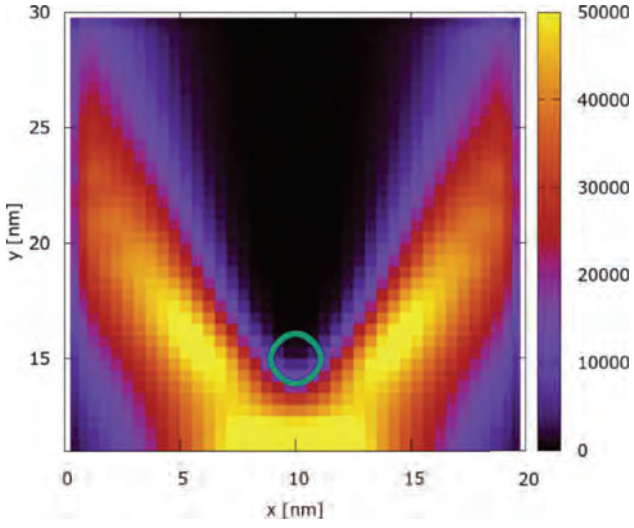


Classical electron density [a.u.]

Physical Model - Wigner MC

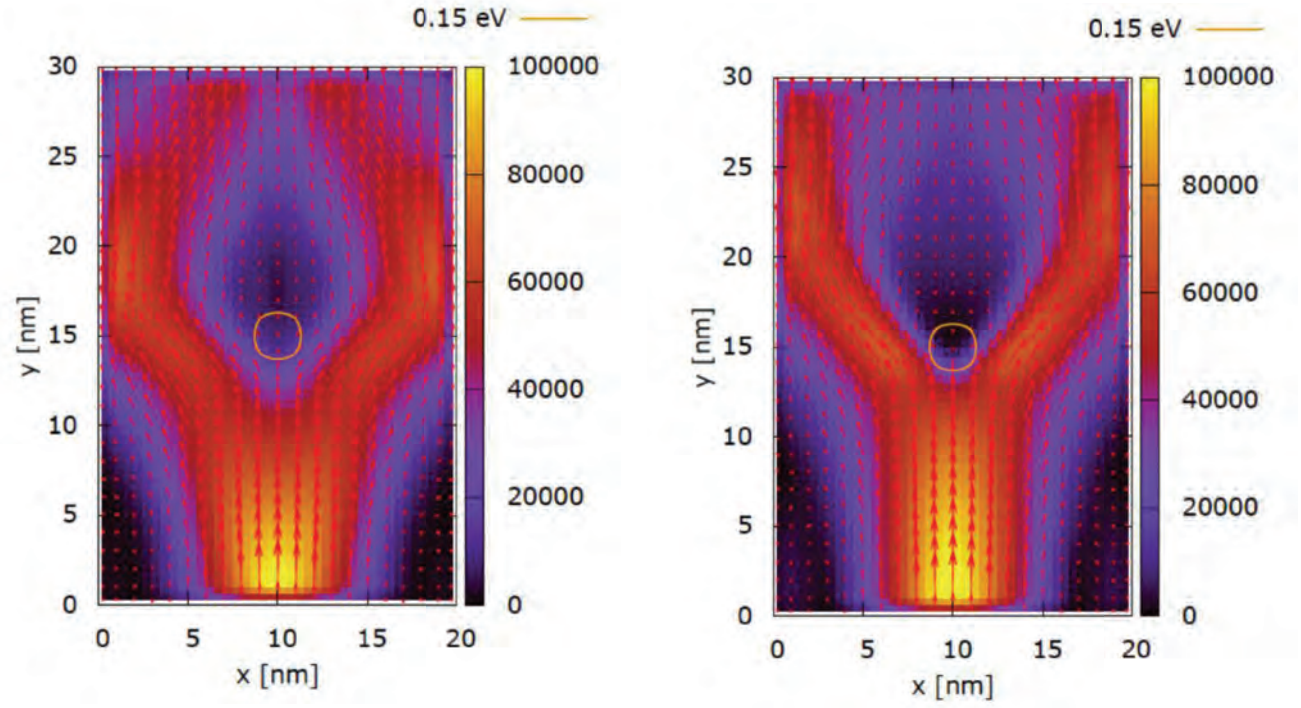


Quantum current density [a.u.]



Classical current density [a.u.]

Physical Model - Wigner MC



With lateral reflecting boundaries

Quantum current density [a.u.]

Classical current density [a.u.]

Conclusions and Outlook

- Physical models and methods
  - Drift Diffusion Method (DD)
    - Fast and well established method but needs quantum corrections
  - Kubo-Greenwood
    - Particle statistical method, needs the appropriate scattering models, good for evaluating mobility in the devices
  - Non-Equilibrium Green's Function (NEGF)
    - Wave representations of the carriers, able to capture quantum mechanical tunneling
  - Wigner Monte Carlo
    - Particle statistical method, quantum mechanics in phase space

Simulation of Nanoscale Interconnects

Lado Filipovic, Institute for Microelectronics, TU Wien

Vienna, Austria

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

Outline

- Introduction
- Copper Conductivity
  - Electron Scattering Mechanisms
    - Electron-Electron
    - Surface Roughness
    - Grain Boundary
- Electromigration Reliability
- Conclusions and Outlook

Outline

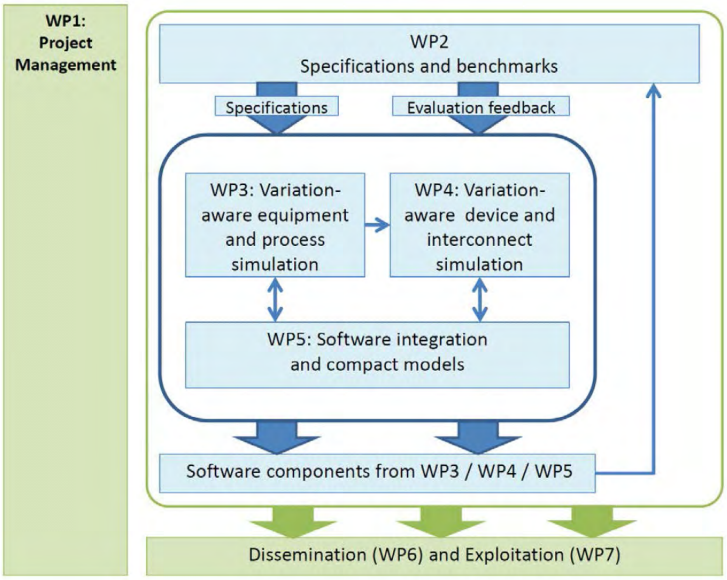
- **Introduction**
- Copper Conductivity
  - Electron Scattering Mechanisms
    - Electron-Electron
    - Surface Roughness
    - Grain Boundary
- Electromigration Reliability
- Conclusions and Outlook

Introduction – Goals and Strategy

- Copper-based metallization in use at least down to 7nm node
  - Nanoscale Cu behavior is influenced by grain size and surface roughness
- Simulations of nano-interconnects lack a connection between modeling the individual interfaces and the continuum simulation of the entire interconnect
  - True for both conductivity and electromigration reliability
- Our goal is to provide simulations to
  - Better understand electron and atom movement inside nanoscale Cu
    - Using Monte Carlo simulations
  - Provide simplified simulation options, while avoiding complex meshes
    - Using spatial parameters in FEM framework

Introduction – Project Context

- This work fits into WP4, dealing with variation-aware interconnect simulations
- The goal is to provide a link between grain boundary/ surface roughness and continuum simulations
- Primarily concentrating on copper conductivity and electromigration reliability

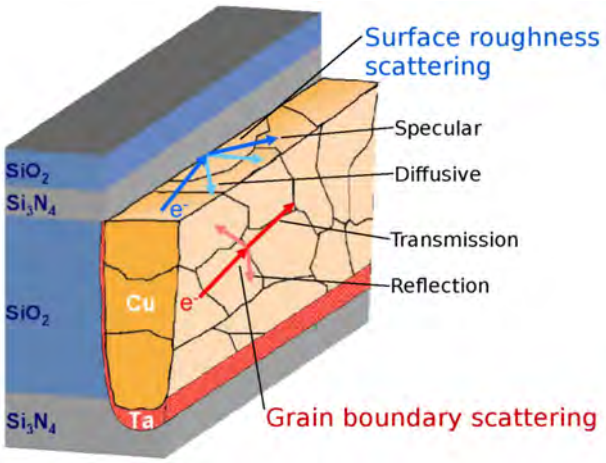


Outline

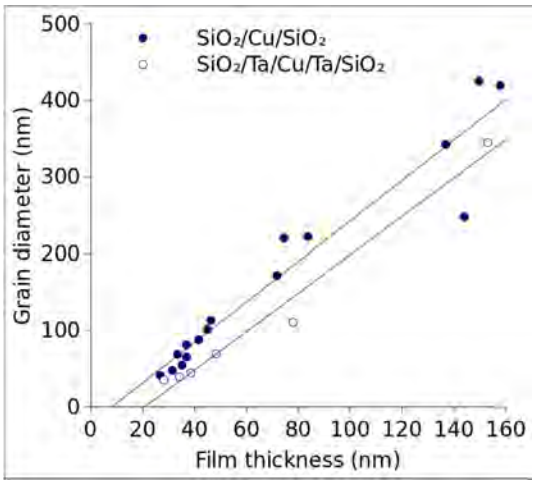
- Introduction
- **Copper Conductivity**
  - Electron Scattering Mechanisms
    - Electron-Electron
    - Surface Roughness
    - Grain Boundary
- Electromigration Reliability
- Conclusions and Outlook

Copper Conductivity

- Cu interconnect scaling results in reduced dimensions
  - Surface roughness and grain boundary play an increasing role



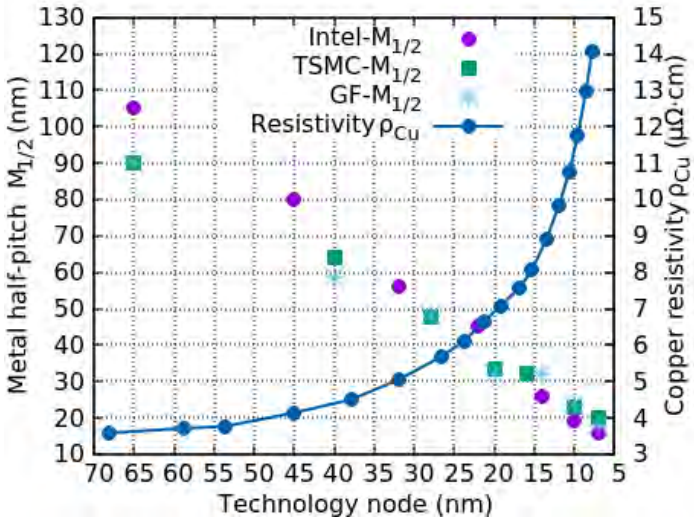
G. Schindler, Sematech workshop on Cu resistivity (2005)



T. Sun, PhD Dissertation, U of Central Florida (2009)

Electron Scattering in Metals

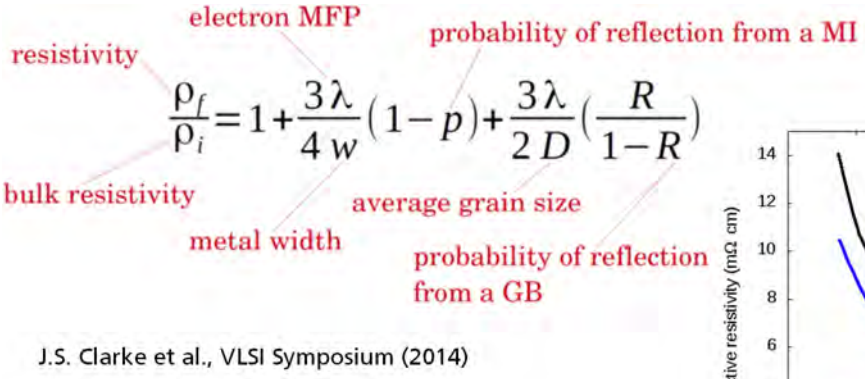
- Cu interconnect scaling results in reduced dimensions
  - Surface roughness and grain boundary play an increasing role



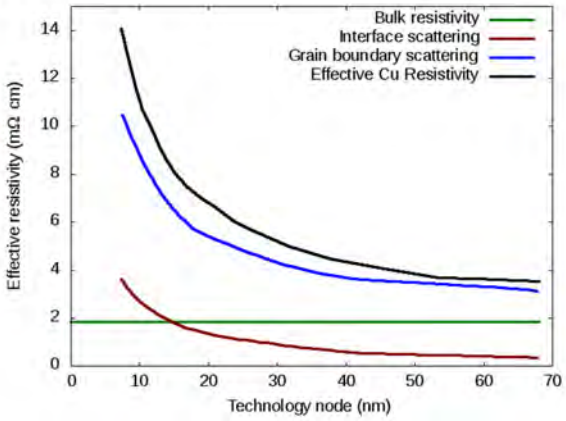
L. Filipovic et al., SISPAD (2017)

Electron Scattering in Metals

- The effects of the granular microstructure on resistivity is modeled by



J.S. Clarke et al., VLSI Symposium (2014)



Electron Scattering in Metals

- Classical macroscopic model for electron transport
  - Scattering events are independent of each other
  - Calculate each event separately, then sum to give total probability
- Microscopic models for electron transport
  - Physical semiconductor models have matured over many decades
  - Modern physical models of transport in metals is far from mature
- Use lessons learned from semiconductor transport (heavily doped)
  - Semiconductor: Moving electrons occupy states above conduction band
  - Metals: Moving electrons in a half-occupied band near the Fermi energy

Equilibrium Electron Statistics I

- Quantum state of an electron is characterized by the quantum number k and energy $\epsilon(k)$
- Equilibrium electron statistics center around the Fermi-Dirac distribution:

$$f(k) = f(\epsilon(k)) = \frac{1}{e^{\frac{\epsilon(k)-\zeta}{k_B T}} + 1}$$

- ζ is the chemical potential, which is a large positive quantity for a many-particle system

Equilibrium Electron Statistics II

- Given the Pauli exclusion principle, the average number of electrons N can be determined as a sum of probabilities of given states to be occupied

$$N = 2\sum_k f(\epsilon(k)) = \frac{2V}{(2\pi)^3}\int d^3k f(\epsilon(k)) = \int_0^\infty d\epsilon 2g(\epsilon)f(\epsilon)$$

where k- states are discrete and 2 accounts for the Pauli exclusion principle

- A single state per volume of Fermi sphere $\frac{V}{(2\pi)^3}$
- Given 3D parabolic energy dispersion, the density of states is

$$g(\epsilon) = V\frac{\sqrt{2}m^{3/2}}{\pi^2\hbar^3}\sqrt{\epsilon}$$

Equilibrium Electron Statistics III

- Normalizing with $\xi = \zeta/k_BT$ and $x = \epsilon/k_BT$ we obtain the ½ Fermi integral

$$n = \frac{\sqrt{2}(mk_BT)^{3/2}}{\pi^2\hbar^3}\int_0^\infty dx\frac{\sqrt{x}}{e^{x-\xi}+1}$$

- And the Fermi energy is obtained

$$e_F = \frac{\hbar^2}{2m^*}(k_F)^2$$

Equilibrium Electron Statistics IV

- Relevant copper properties for electron statistics:

Parameter	Symbol	Value
Density	ρ	8.960 g/cm^3
Atomic mass	m_a	63.546 kg/mole
Permittivity	ε	8.85419 x 10^{-12} F/m
Effective mass	m^*	1.0 m_e = 911 x 10^{-31} kg

- Total electron density and the Fermi energy are then solved to give

$$n_e = \frac{N_A \times \rho}{m_a} = 8.49 \times 10^{28}\mathrm{m}^{-3} \qquad e_F = \frac{\hbar^2 k_F^2}{2m^*} = 7.0\mathrm{eV}$$

Equilibrium Electron Statistics V

- In semiconductors the bottom of the conduction band is above the chemical potential and serves as the origin of the energy
- In metals the number of *free* electrons taking part in conduction are those within a thin energy band around the Fermi energy

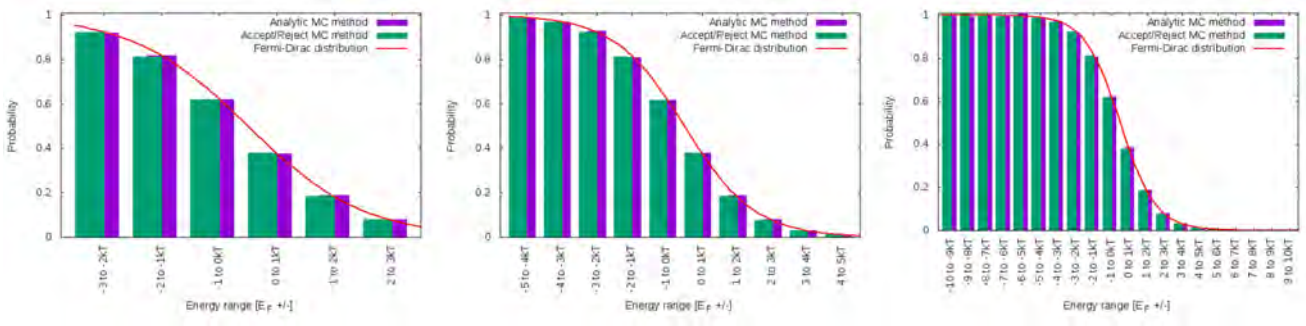
$$n_C = \int_{e_F - e_n}^{e_F + e_n} \frac{(2m^* e)^{1/2}}{8\hbar^3 \pi^2} \times \frac{de}{\exp\left(\frac{e - e_F}{k_B T}\right) + 1}$$

- Generated electron energies are assigned within the range $[e_F - e_n : e_F + e_n]$ according to the FD distribution

Equilibrium Electron Statistics VI

- We used two MC techniques to solve the previous equation and generate the conducting electrons and their energies.

$\epsilon_n = 3k_BT$ $\epsilon_n = 5k_BT$ $\epsilon_n = 10k_BT$



Improved simulation accuracy
Increased simulation time and effort

Scattering Mechanisms: Electron-Electron

- Electron-electron scattering depends on the electron density, applied field, energy, etc.
- It does not significantly increase at reduced dimensions
- In our simulator EE scattering is applied using a scattering time τ_{ee}, calculated using the classical definition of the conductivity baseline:

$$\sigma = \frac{q^2 n_e \tau_{ee}}{m^*} \quad or \quad \rho = \frac{m^*}{q^2 n_e \tau_{ee}}$$

- With a bulk resistivity of 1.7 x 10^{-8} Ωm the scattering time is τ_{ee} = 2.64 x 10^{-14} s

Scattering Mechanisms: Surface Roughness I

- Heuristic models associate to specular scattering, where the incident and reflected angels are equal
- Roughness results in randomization of the reflected angle of the scattered electron
- We set a parameter γ which determines the ratio between the specular and random scattering events

$0 \leq \gamma(r_\Phi) \leq 1$, where $\Phi(r_\Phi) = 0$ defines the surface of the boundary

Scattering Mechanisms: Surface Roughness II

- Comprehensive models account for stochastic properties of the roughness, based on the Fermi Golden Rule
- Probability *S* is given for a transition *per unit time* from an initial state $|k\rangle$ defined by quantum numbers k and energy E_k, to a state k' under the action of a perturbing Hamiltonian H':

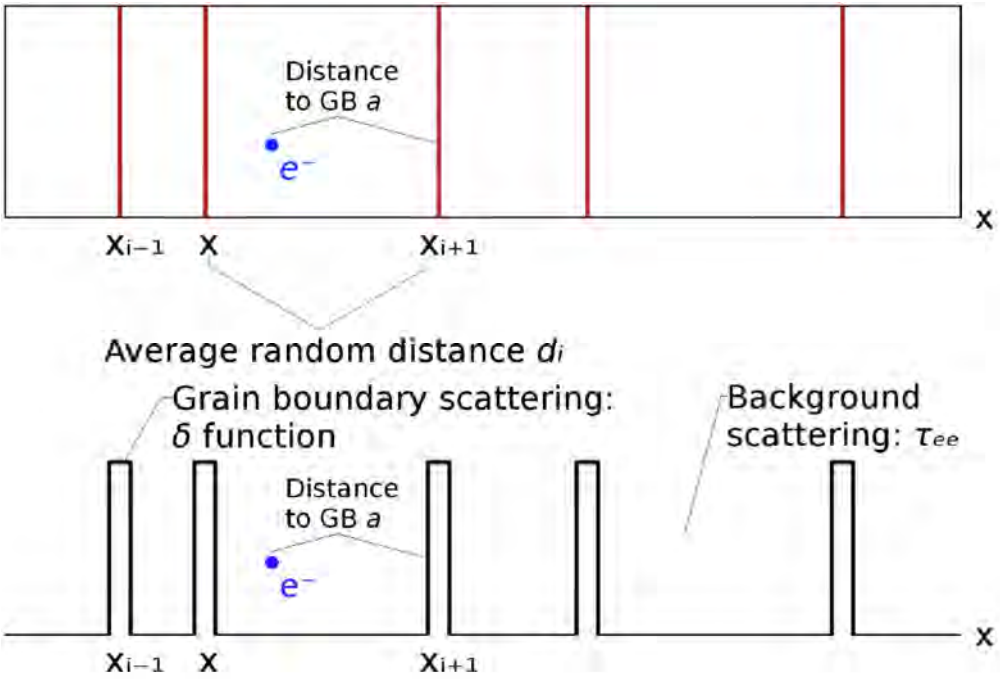
$$S(\mathbf{k}, \mathbf{k}') = \frac{2\pi}{\hbar} \left| \langle \mathbf{k}' | H' | \mathbf{k} \rangle \right|^2 \delta(E_{\mathbf{k}'} - E_{\mathbf{k}})$$

- Here the δ function accounts for the energy conservation of the interaction with the surface roughness potential H'

Scattering Mechanisms: Grain Boundaries

- An electron, interacting with a grain boundary has a probability of reflection *R* or transmission *(1 - R)*
- A combination of specular and diffusive reflection represents the physical reflection from a grain boundary
- Electron energy loss during reflection or transmission should also be included

Scattering Mechanisms: Grain Boundaries

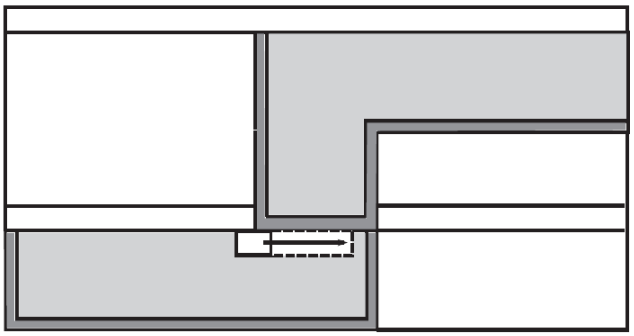


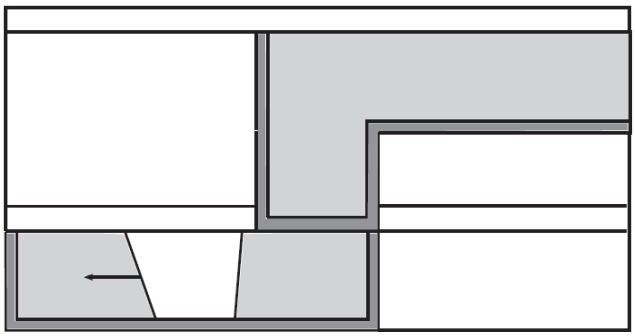
Outline

- Introduction
- Copper Conductivity
  - Electron Scattering Mechanisms
    - Electron-Electron
    - Surface Roughness
    - Grain Boundary
- **Electromigration Reliability**
- Conclusions and Outlook

Electromigration in Copper: Failure Modes

- Time to failure due to electromigration is a combination of two failure modes:





Early failure mode:

- E-field causes movement of ions
- Ion transport forms vacancy/hillock
- Vacancy and hillock induce stress
- Critical stress causes crack/failure

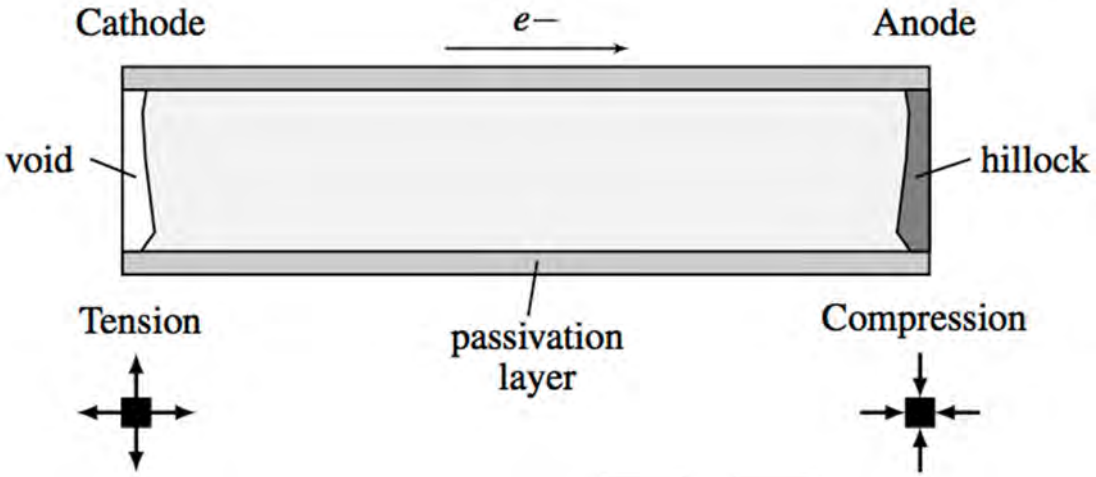
Late failure mode:

- Critical stress causes void nucleation
- Nucleated void grows to relieve stress
- Void growth increases line resistance
- Fails at critical resistance/open circuit

R.L. de Orio et al., Microelectron. Rel. (2011)

Electromigration in Copper: Early Failure Mode

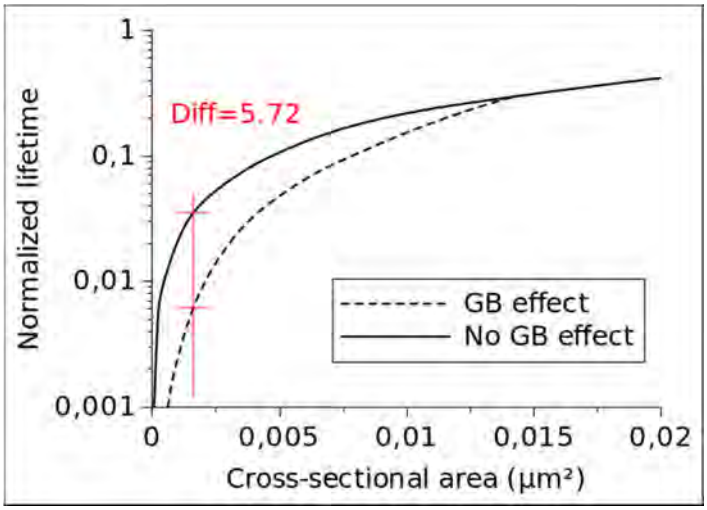
- Early failure mode is a combination of
  - Vacancy transport (anode to cathode) forming voids/hillocks
  - Resulting tensile (cathode) and compressive (anode) stress



Electromigration in Copper: Scaling

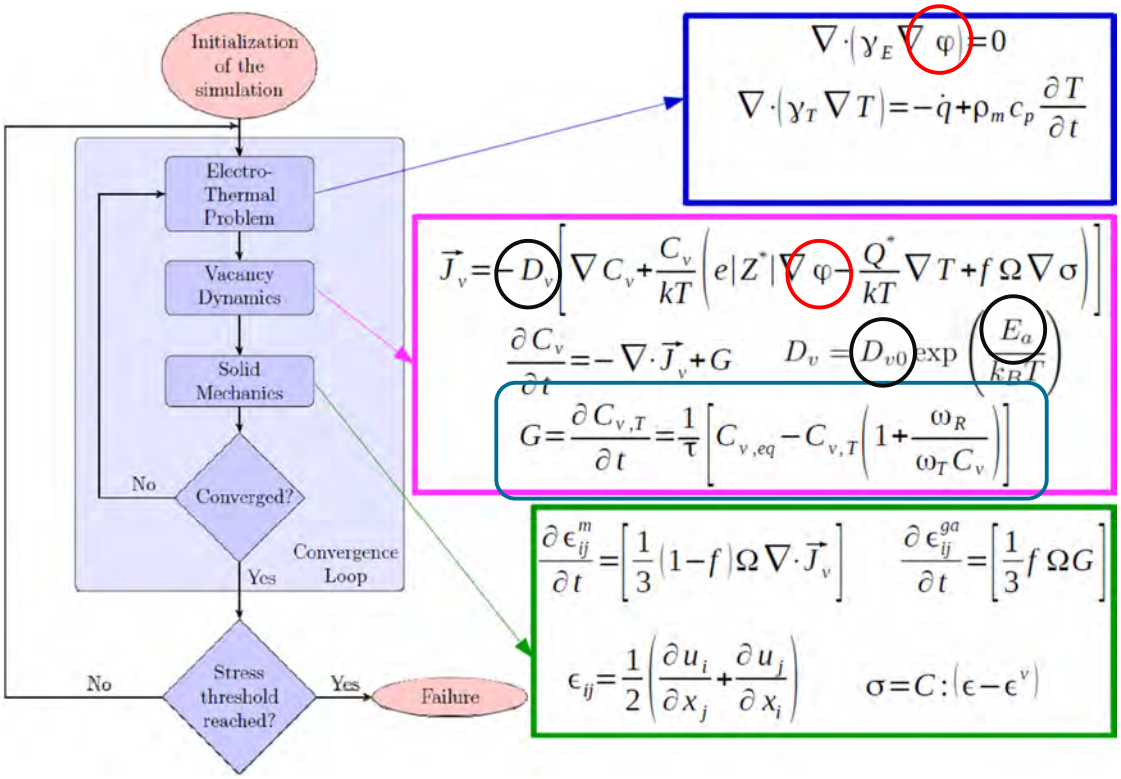
- Shrinking dimensions result in increased current densities
- Experiments show increased grain boundaries reduce expected lifetimes

An electromigration model must include the effects of material interfaces and grain boundaries

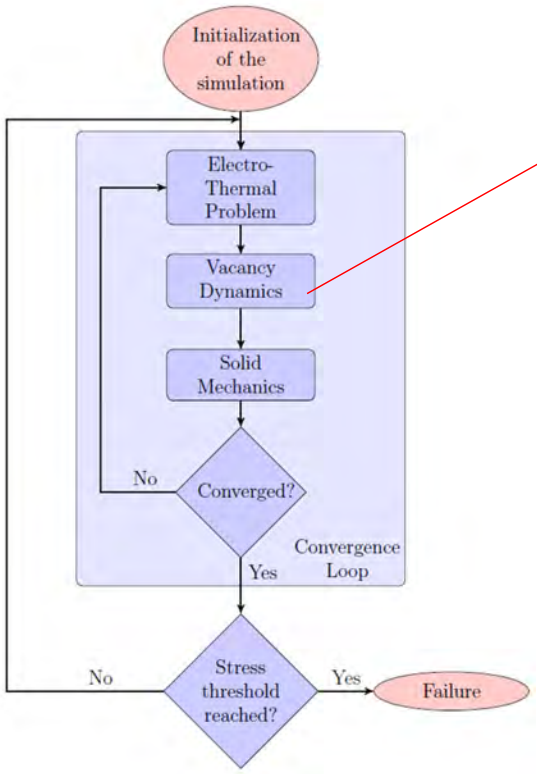


L. Filipovic et al., SISPAD (2017)

Electromigration in Copper: Model I



Electromigration in Copper: Model II



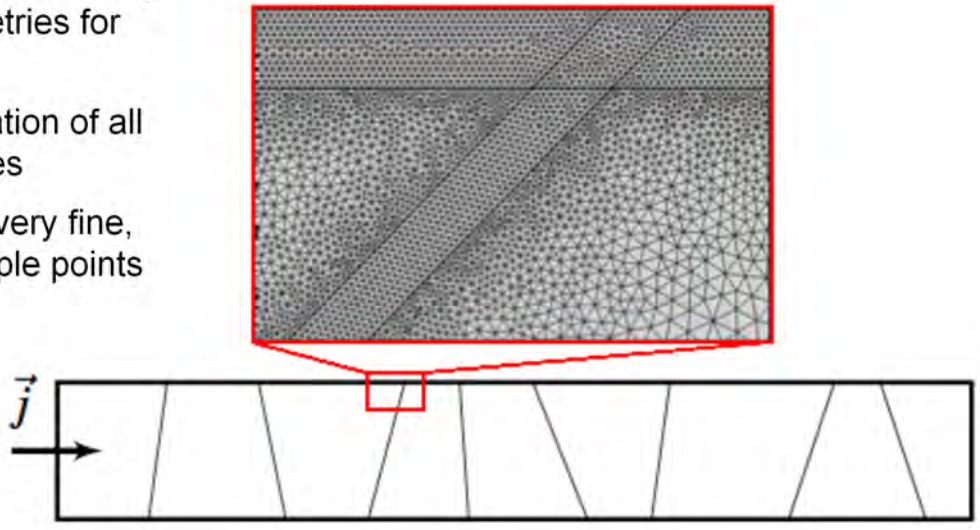
$$D_v = D_{v0}\exp\left(\frac{E_a}{k_B T}\right)$$

Parameter	E_a (eV)	D_{v0} (cm²/s)
Grain	0.89	0.52
GB	0.7	52
MI	0.5	520

R.L. de Orio et al., Microelectron. Rel. (2011)

Electromigration in Copper: SOA

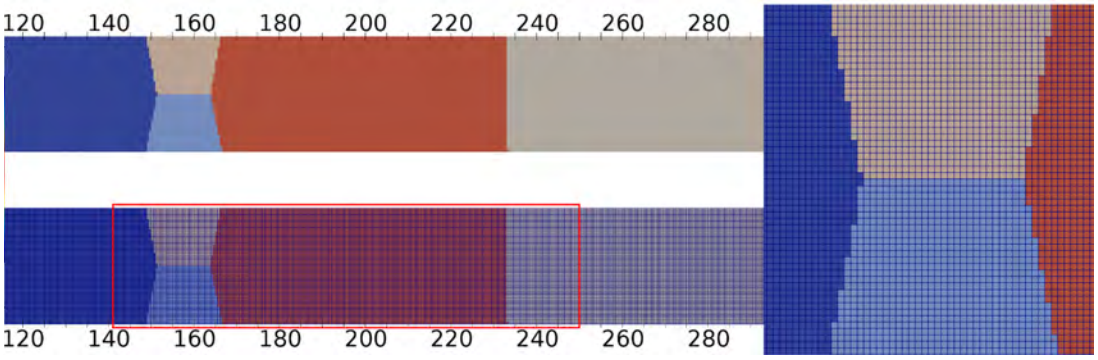
- Microstructure treated using predefined geometries for GB and MI
  - Must know location of all grain boundaries
  - Mesh must be very fine, especially at triple points



M. Rovitto, *PhD Dissertation* TU Wien (2016)

Electromigration in Copper: Modeling Approach I

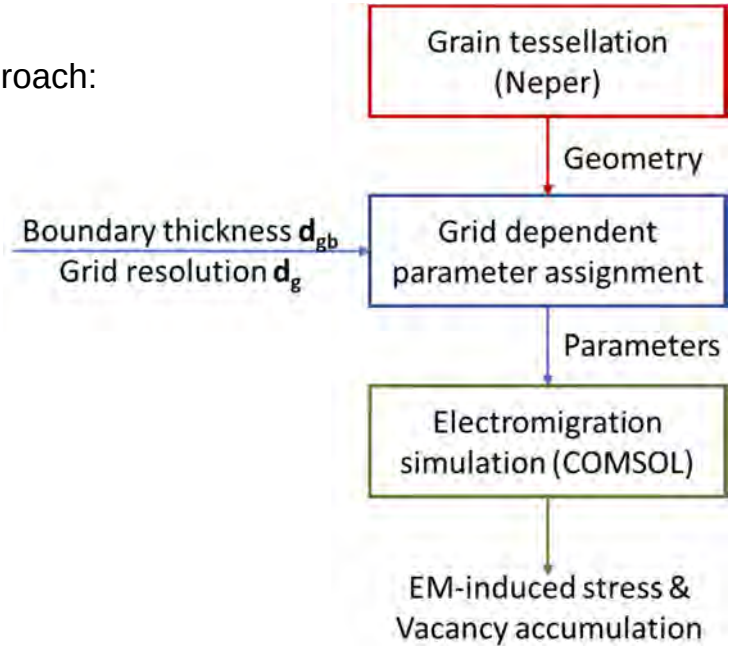
- Developed approach:
  - Treat microstructure using a spatial material parameter to define GBs, MIs, and Cu grains, applied to:
    - Conductivity, Vacancy diffusivity, Effective valence Z*
    - Apply the vacancy generation/annihilation term at GB/MIs



L. Filipovic et al., SISPAD (2018)

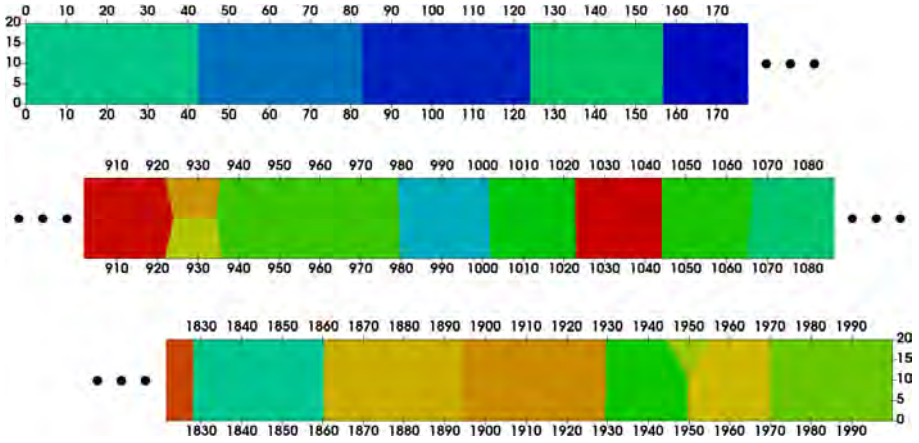
Electromigration in Copper: Modeling Approach II

- Developed approach:



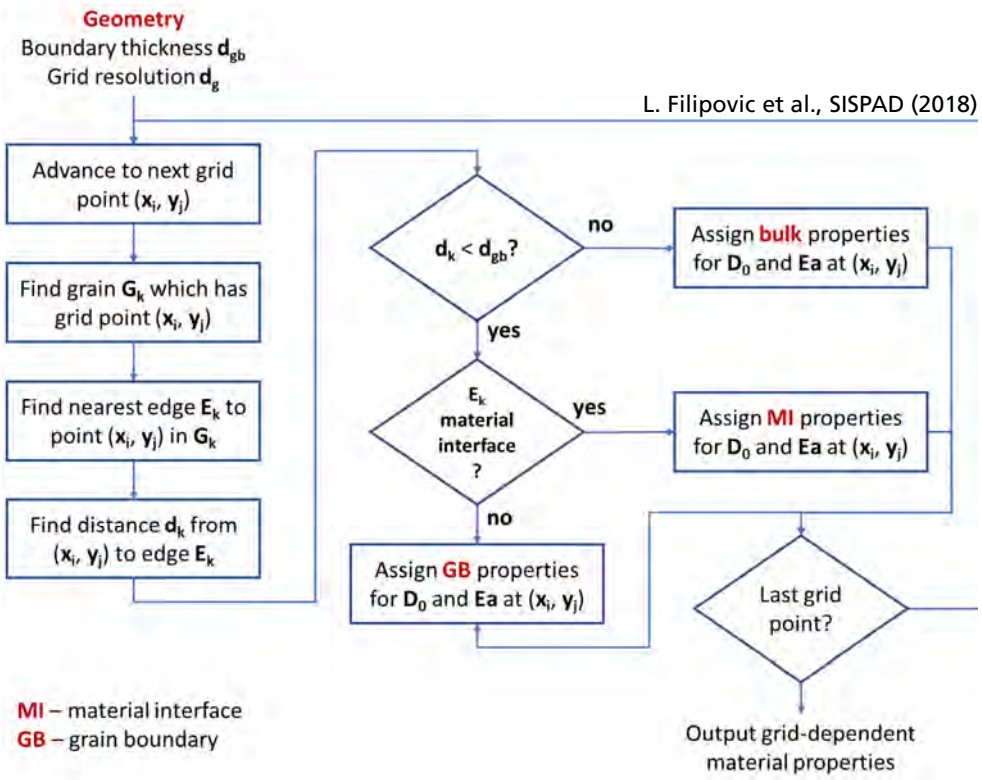
Electromigration in Copper: Grain Tessellation

- Grain tessellation
  - Using an average grain size, set total number of grains (seeds)
  - Randomly place seeds in the copper line and grow until filled



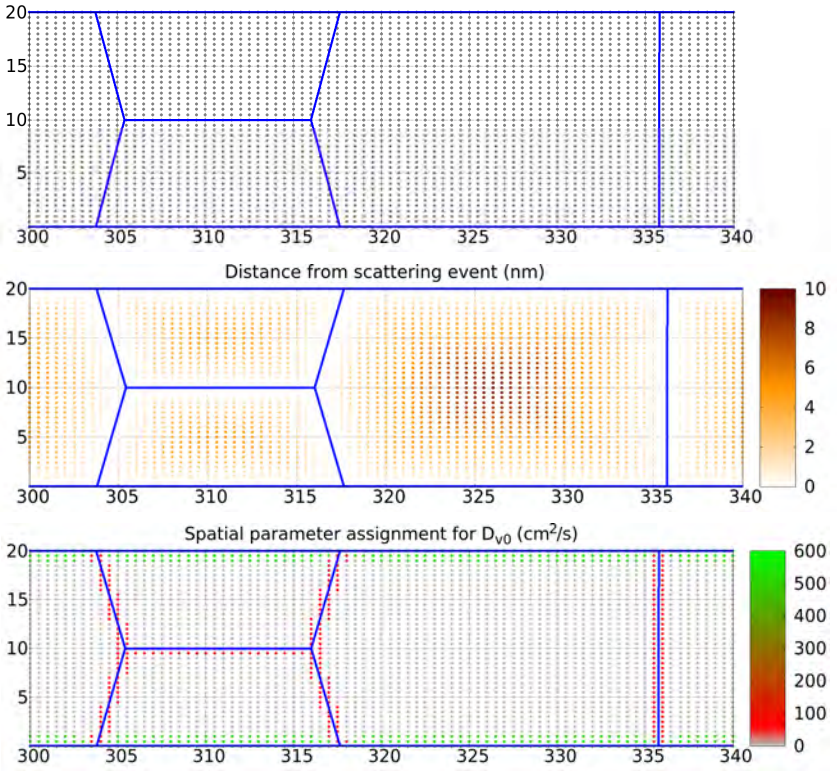
L. Filipovic et al., SISPAD (2018)

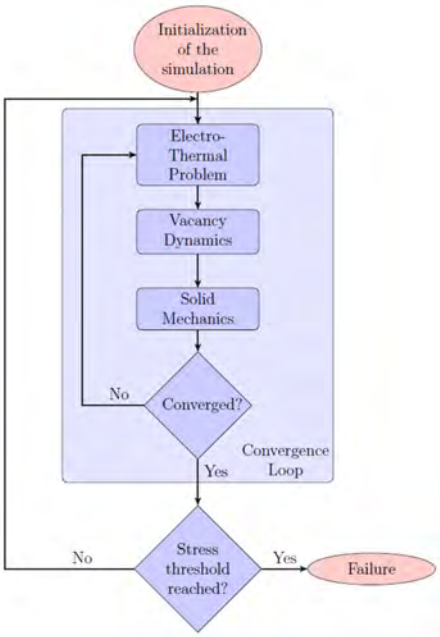
Electromigration in Copper: Parameter Assignment I



L. Filipovic et al., SISPAD (2018)

Electromigration in Copper: Parameter Assignment II

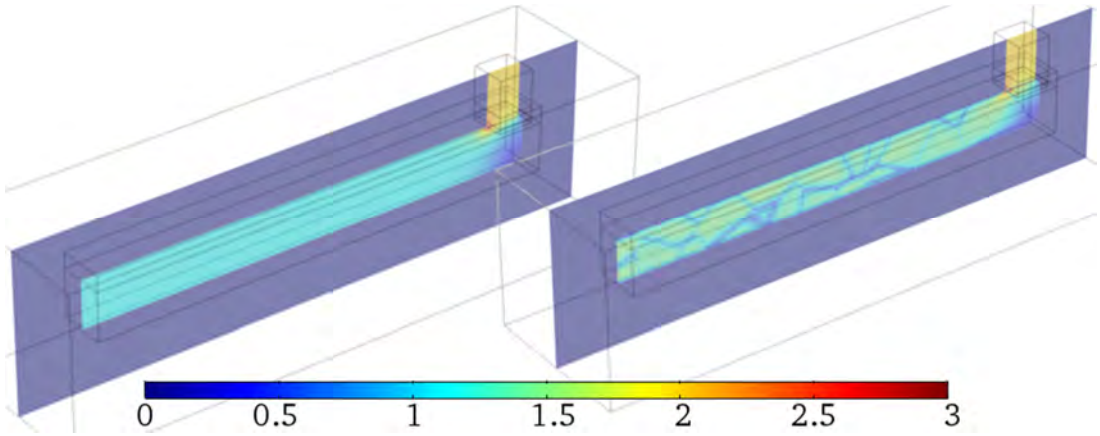




L. Filipovic et al., SISPAD (2018)

Electromigration in Copper: Simulation Results I

- Current density variation when 1MA/cm² is applied (bulk vs microstructure):

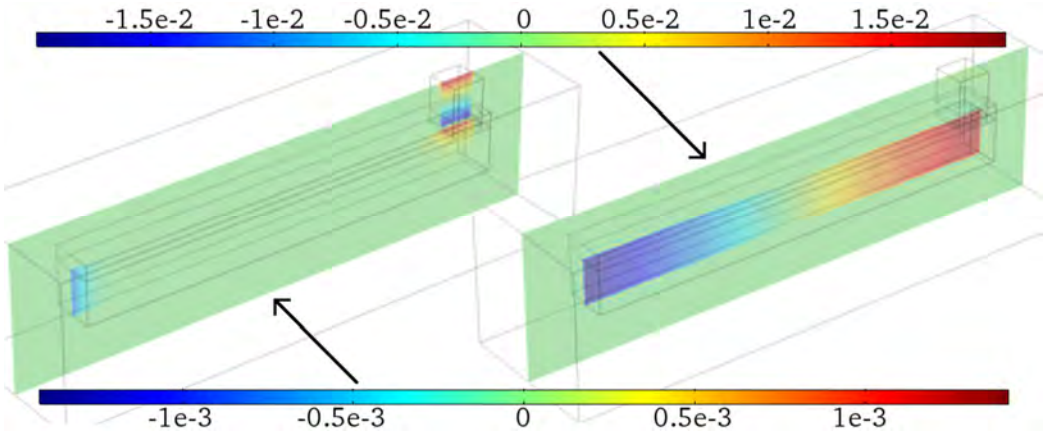


The effects of microstructure are immediately evident!

L. Filipovic et al., SISPAD (2017)

Electromigration in Copper: Simulation Results I

- Vacancy concentration at 0.1ms when 1MA/cm^2 at 300°C is applied (bulk vs microstructure):



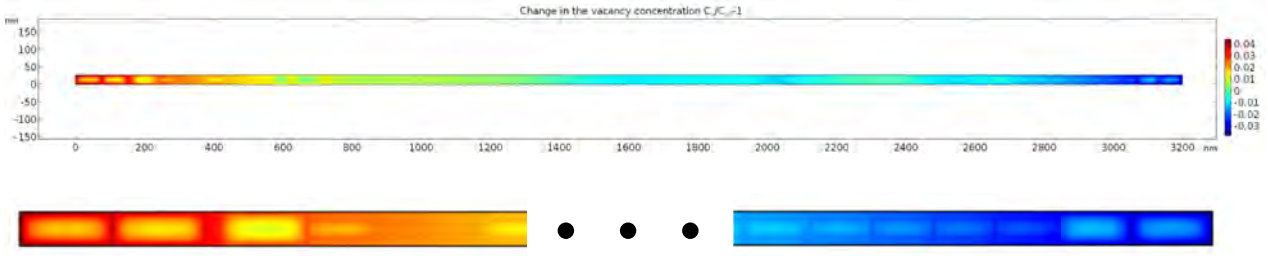
Normalized vacancy concentration (C_v/C_{v0} - 1)

Vacancies accumulate much faster due to the GBs and MIs

L. Filipovic et al., SISPAD (2017)

Electromigration in Copper: Simulation Results I

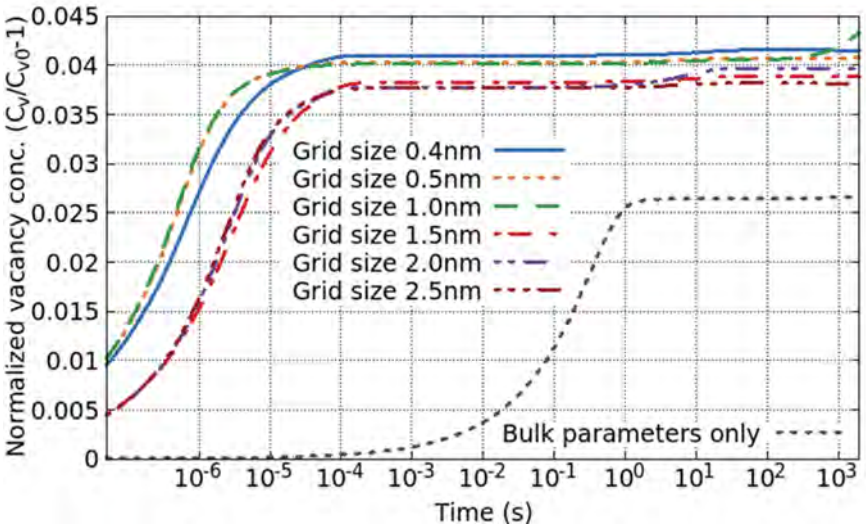
- Electromigration simulations using different mesh resolutions were performed
  - Geometry: 2000 x 20nm, grain size 25nm
  - Electromigration setup: 1MA/cm^2 current density applied at 300°C
  - Vacancy concentration at onset of electromigration:



L. Filipovic et al., SISPAD (2018)

Electromigration in Copper: Simulation Results II

- Electromigration simulations using different mesh resolutions were performed

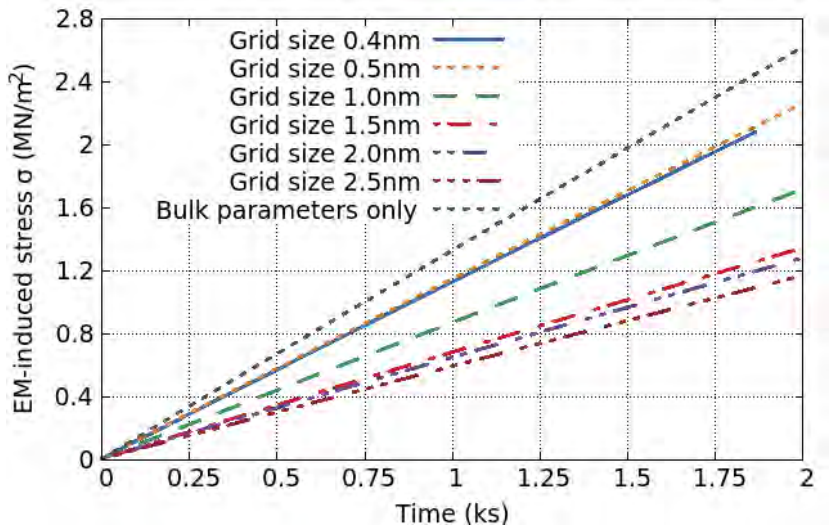


- Even coarse grids show reasonable results for the vacancy concentration
- Bulk parameters underestimate the time at which EM effects initiate

L. Filipovic et al., SISPAD (2018)

Electromigration in Copper: Simulation Results III

- Electromigration simulations using different mesh resolutions were performed



- Underestimated stress values with increasing grid size

L. Filipovic et al., SISPAD (2018)

Outline

- Introduction
- Copper Conductivity
  - Electron Scattering Mechanisms
    - Electron-Electron
    - Surface Roughness
    - Grain Boundary
- Electromigration Reliability
- **Conclusions and Outlook**

Conclusions and Outlook

- As interconnects shrink grain boundaries and material interfaces play increasing roles in copper conductivities and reliability
- A Monte Carlo model was developed to include electron scattering mechanisms in metal lines
  - Model is based on semiconductor knowledge developed over decades
  - Will be implemented and released in an open simulator from TU Wien
- The effect of microstructure on interconnect lifetime is examined
  - Treat grain boundaries and material interfaces as parameters
  - Introduced spatial parameters within a finite element framework
    - Conductivity, atom diffusivity, activation energy …
  - Model will enable variation to be introduced to complex EM simulations

Variability aware simulations of nano-scale devices

Dr. Vihar Georgiev, University of Glasgow, Glasgow, UK

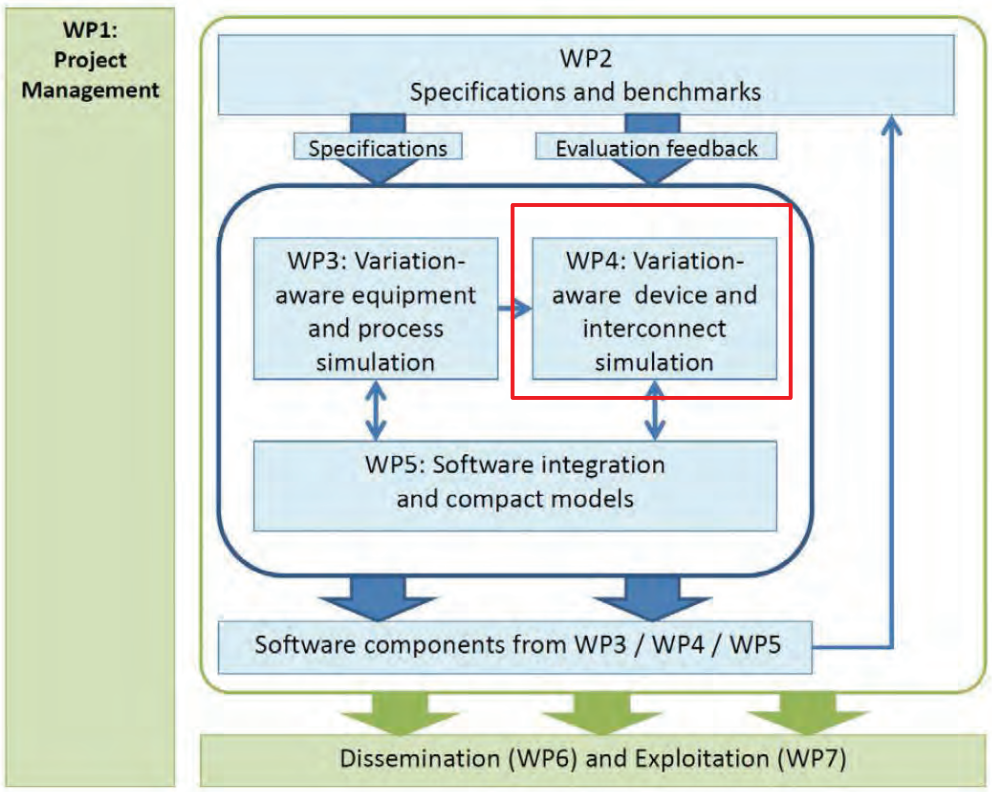
ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

Outline

- Introduction
  - Project flow and link between the Work Packages
- Long range, short range and statistical variability
- Time-dependent variability
- Statistical variability example
- Conclusions and outlook

Introduction – project context

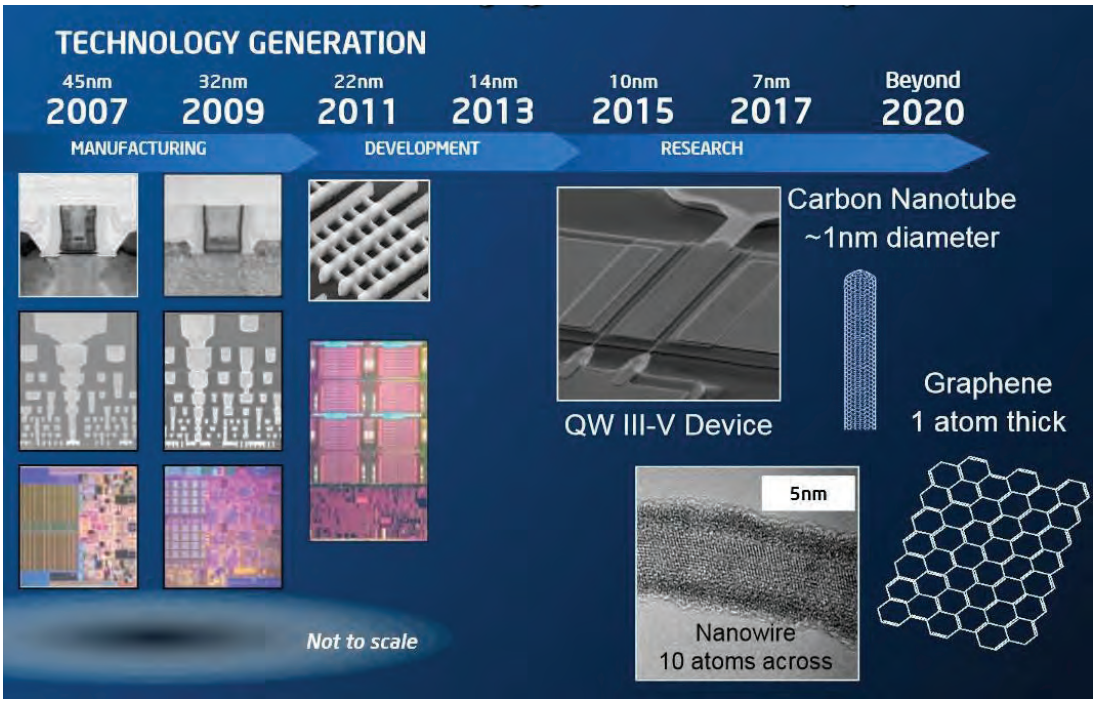


Outline

- Introduction
  - Project flow and link between the Work Packages
- **Long range, short range and statistical variability**
- Time-dependent variability
- Statistical variability example
- Conclusions and outlook

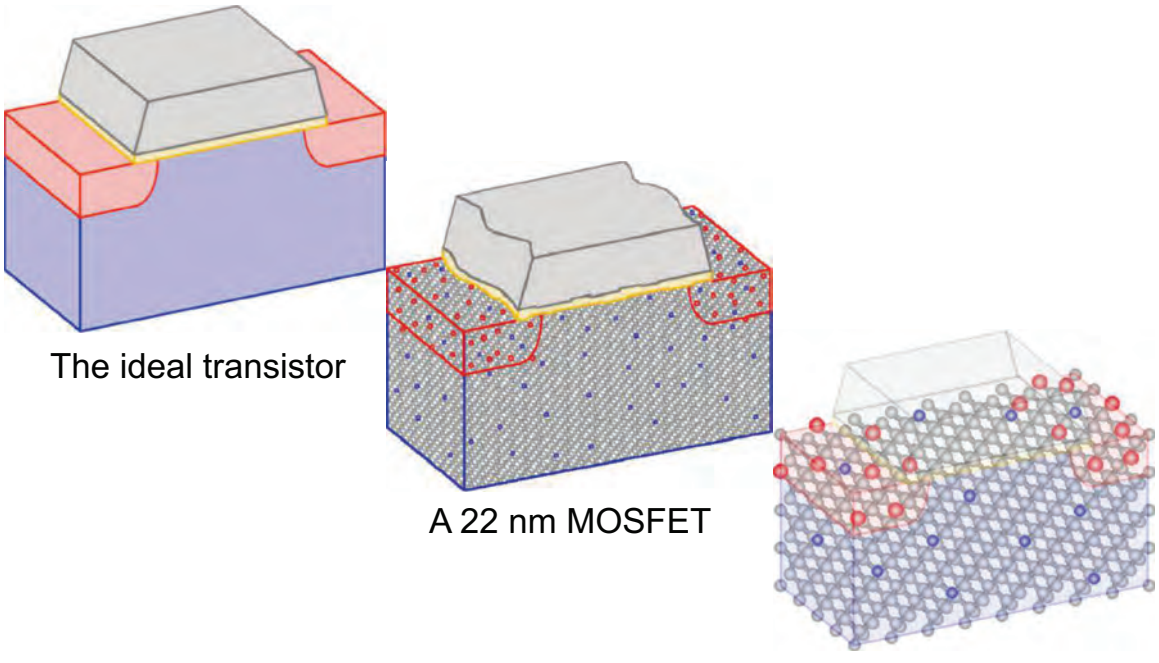
SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

Saturation in performance and increasing variability drives the CMOS innovations



Intel, ISSCC

Statistical variability



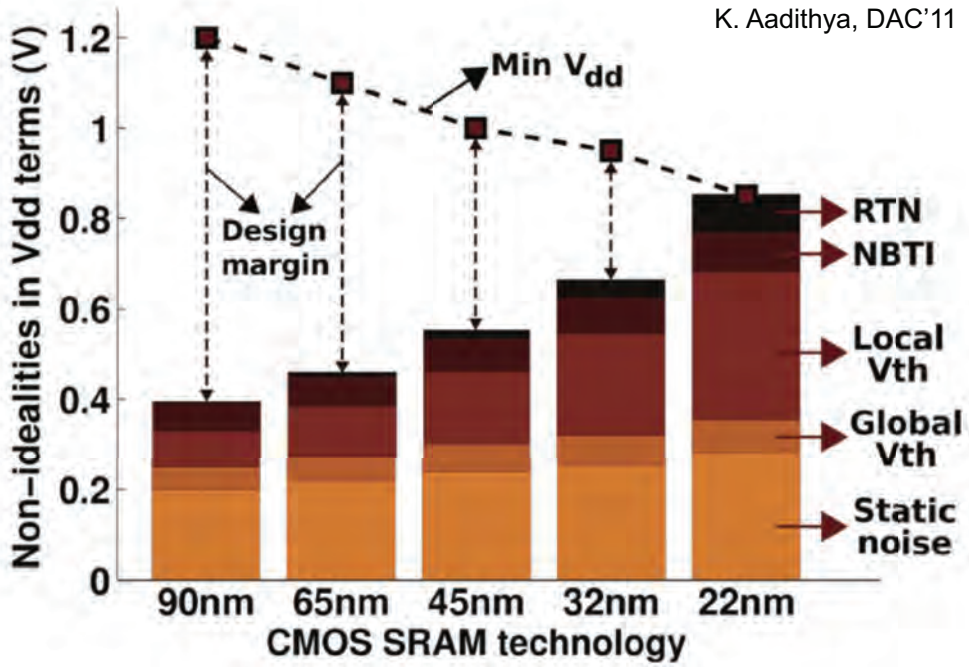
The ideal transistor

A 22 nm MOSFET

A 4.2 nm MOSFET

Variability is one of the major challenges associated with scaling

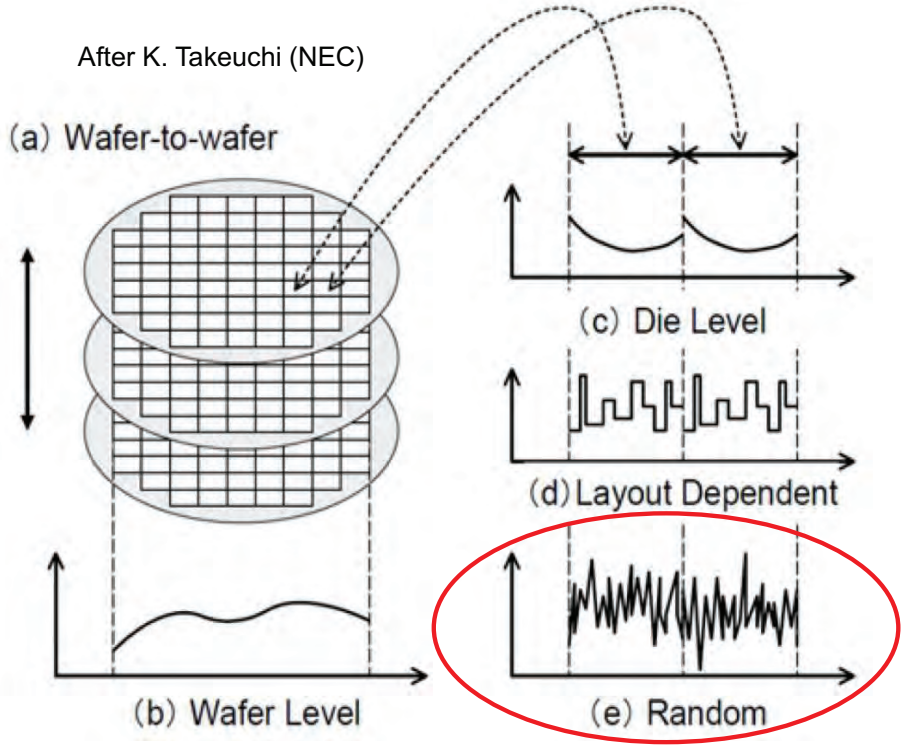
K. Aadithya, DAC'11



Variability results in higher parametric yield losses

Variability classification

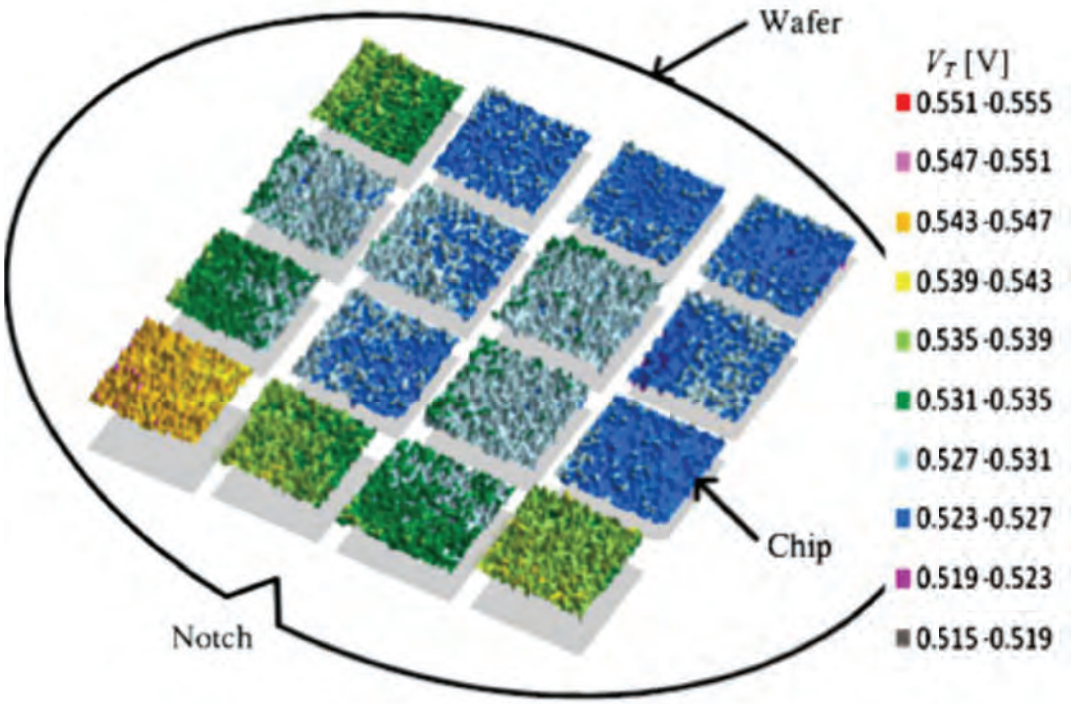
After K. Takeuchi (NEC)



Global – Local
Systematic – Statistical

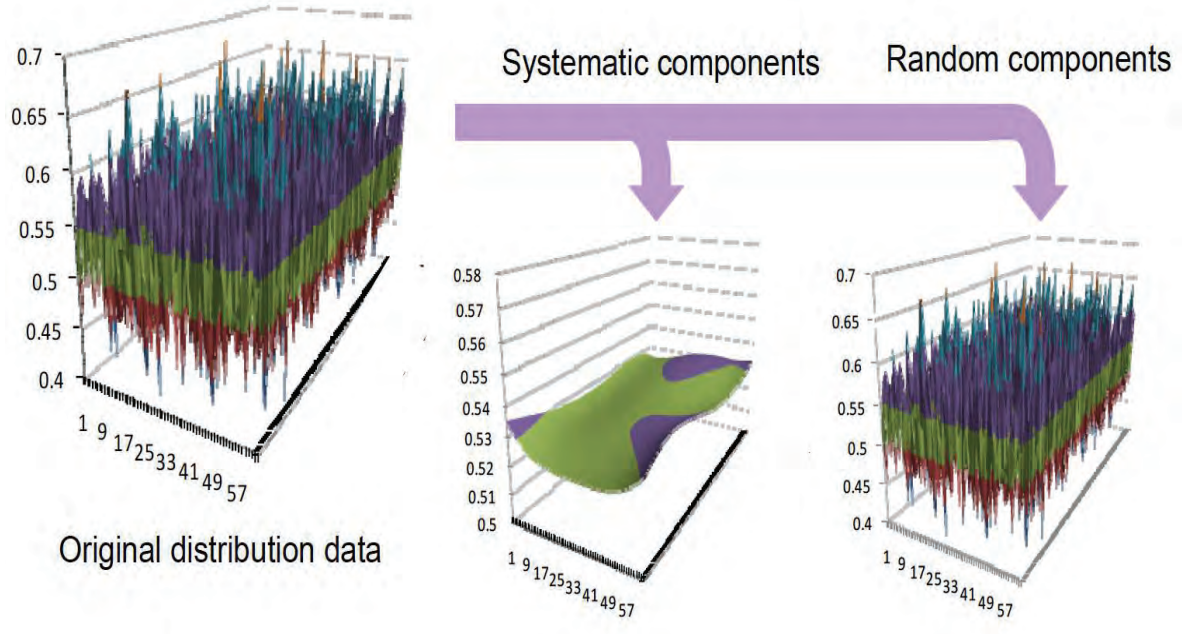
Wafer to wafer
Across the wafer
Across the chip

Variability in 65 nm (L=60 nm, W=140 nm)



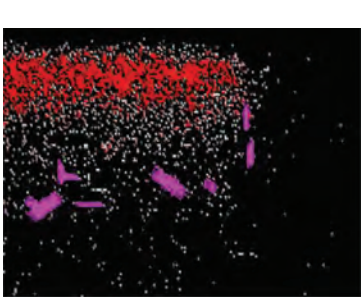
T. Hiramoto (Tokyo Univ)

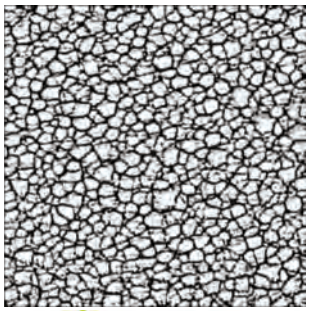
Variability in 65 nm (L=60 nm, W=140 nm)

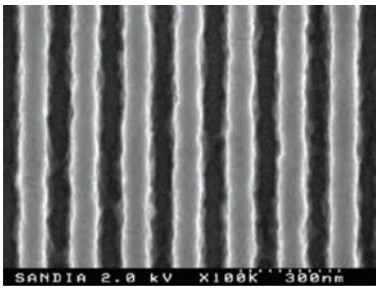


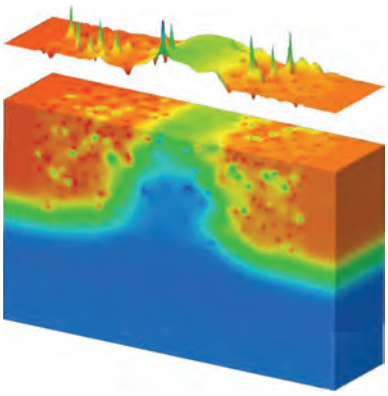
T. Hiramoto (Tokyo Univ)

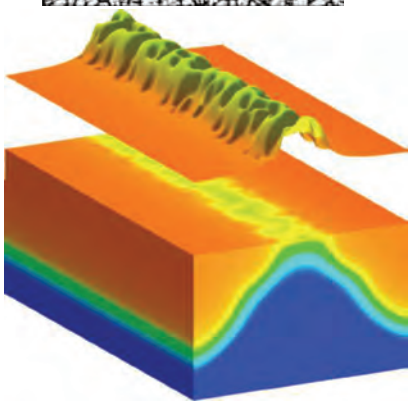
Sources of statistical variability

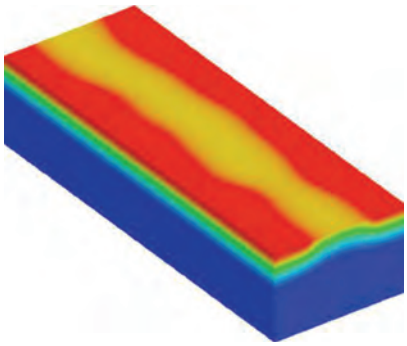










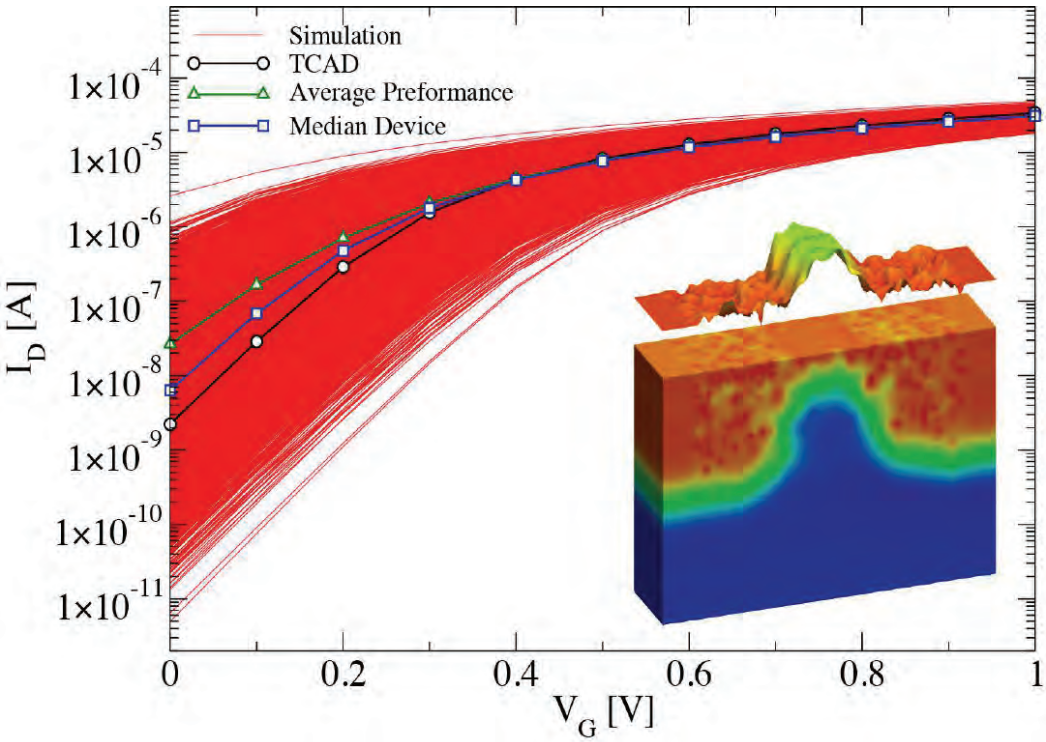


Random dopants

Metal gate or Polysilicon Granularity

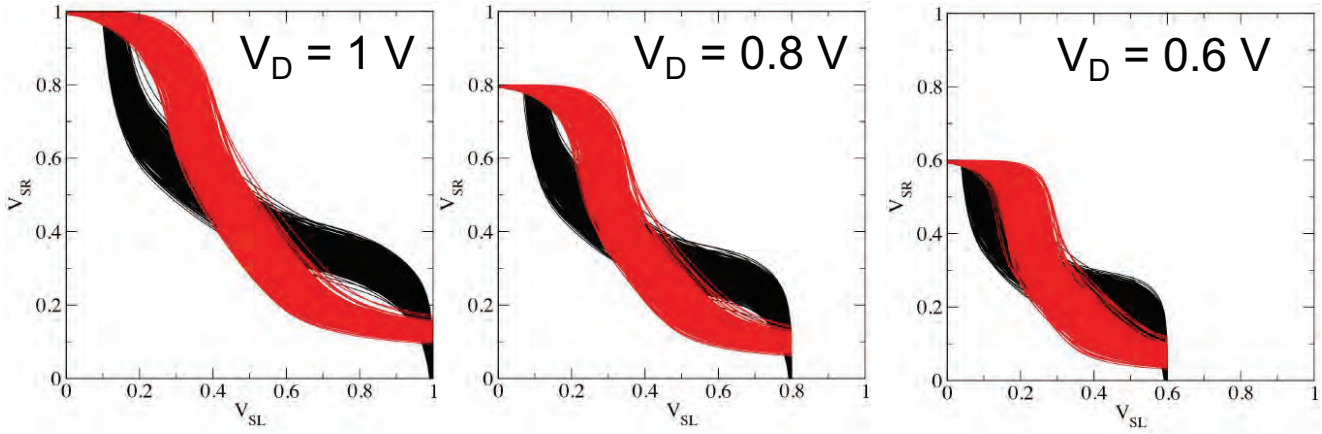
Line edge roughness

Variability in 20 nm CMOS



Statistical variability fuels the power crisis

The SRAM yield depends critically on supply voltage

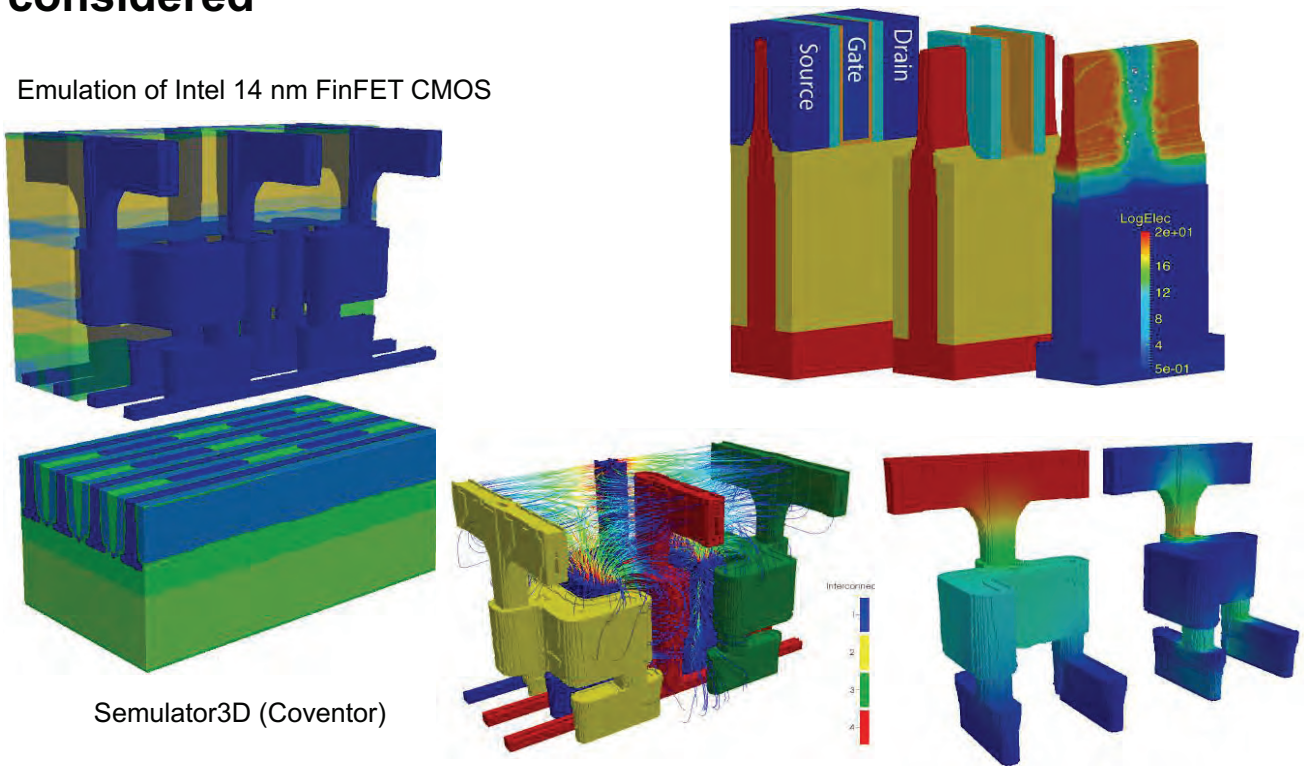


20nm SRAM butterfly curves as a function of V_{DD}

The butterfly eye is closing rapidly with the reduction of the supply voltage. This keeps the system on chip (SoC) supply voltage high increasing the dynamic power.

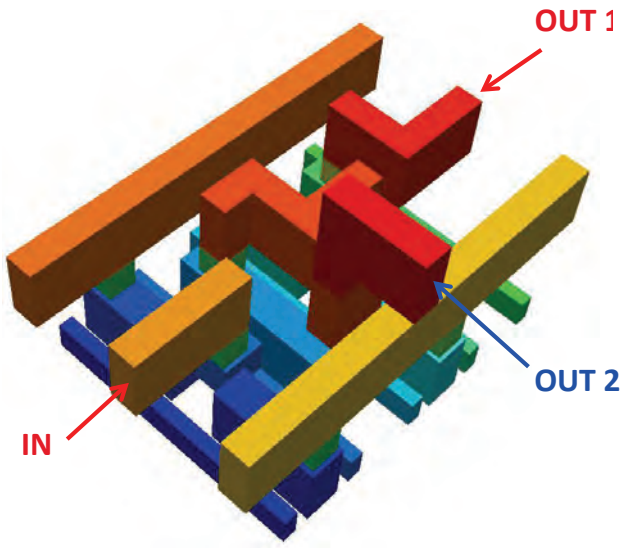
Both transistor and interconnect variability need to be considered

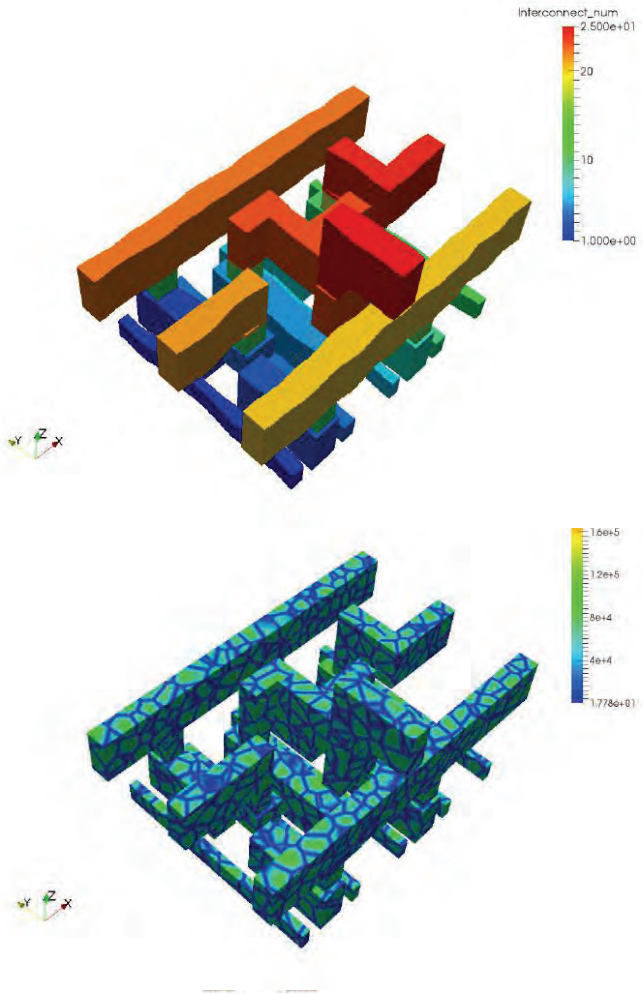
Emulation of Intel 14 nm FinFET CMOS



Semulator3D (Coventor)

Interconnect variability





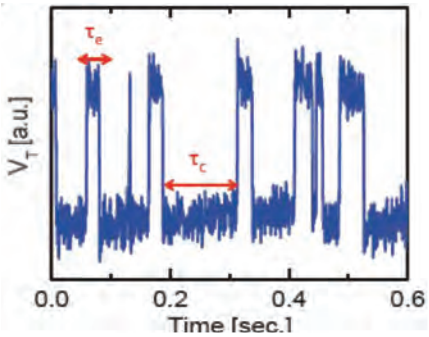
Outline

- Introduction
  - Project flow and link between the Work Packages
- Long range, short range and statistical variability
- **Time-dependent variability**
- Statistical variability example
- Conclusions and outlook

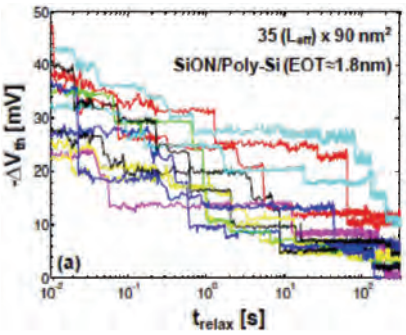
Time-dependent variability

- Random Telegraph Noise (**RTN**)
- Bias Temperature Instability (**BTI**)
- Trap Assisted Tunneling (**TAT**)
- Hot carrier injection (**HCI**)

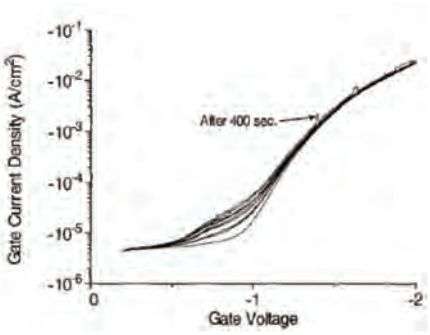
RTN



BTI relaxation

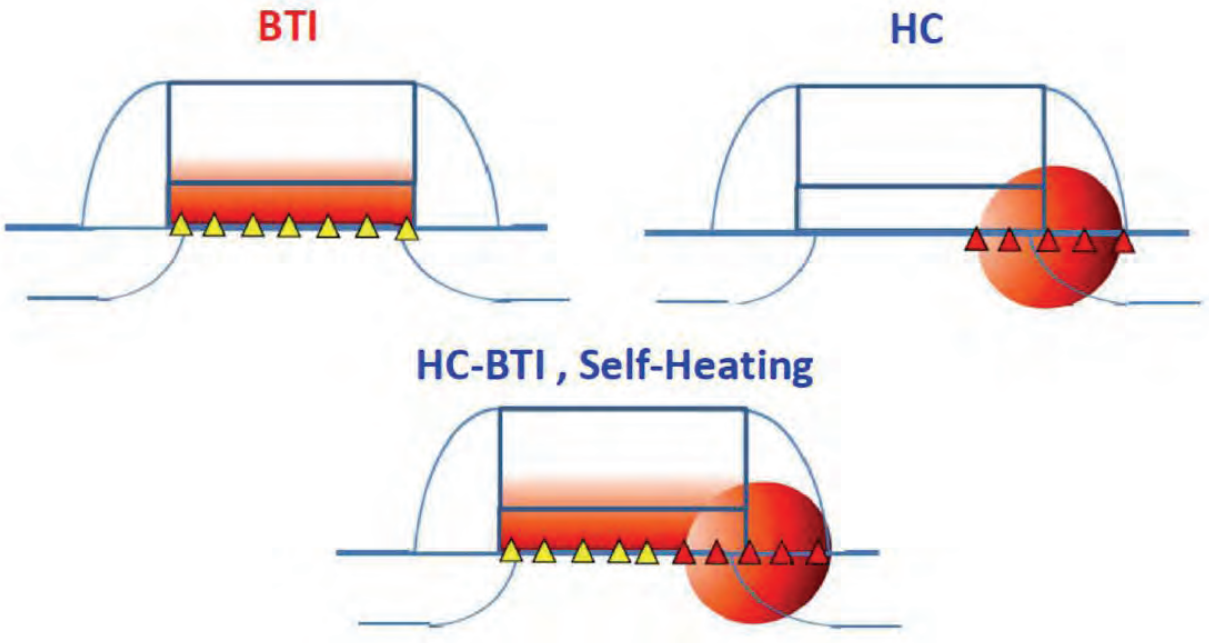


TAT



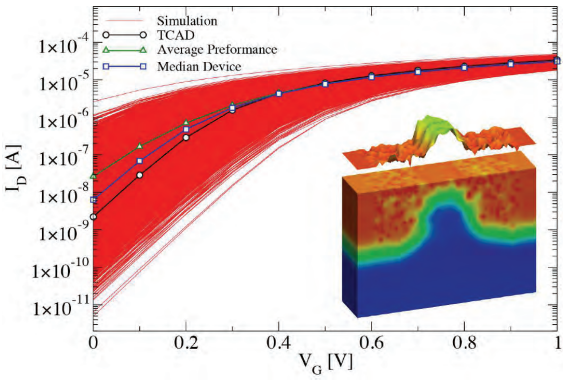
BTI vs HCI

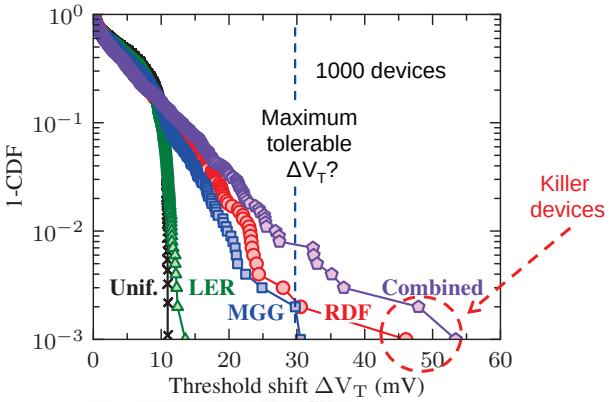
BTI – uniform trap distribution and charge trapping
HCI – non-uniform trap distribution and charge trapping



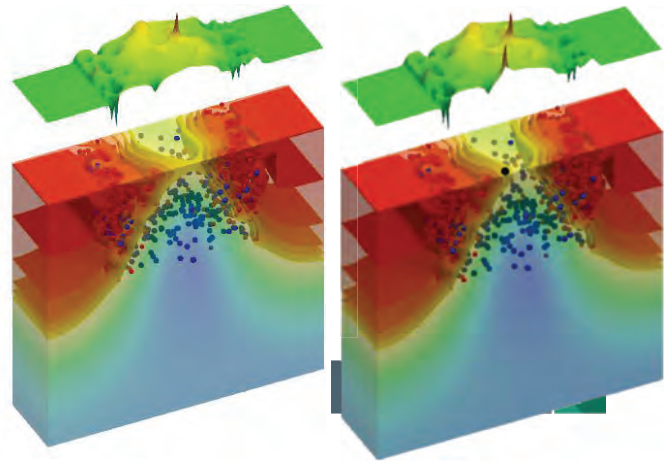
A. Bravaix

Strong interplay between statistical variability and statistical reliability





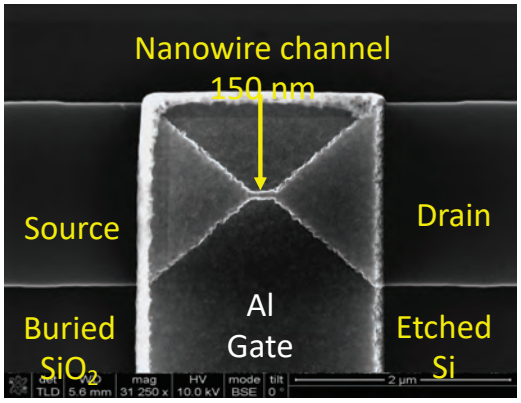
Parameter		n-MOS
L_g	[nm]	25
EOT	[nm]	0.85
X_j	[nm]	15
N_A	[E18/cm^3]	4.5
V_{dd}	[V]	1
I_{off}	[nA]	100
I_{on}	[µA]	1351
Spacer	[nm]	24

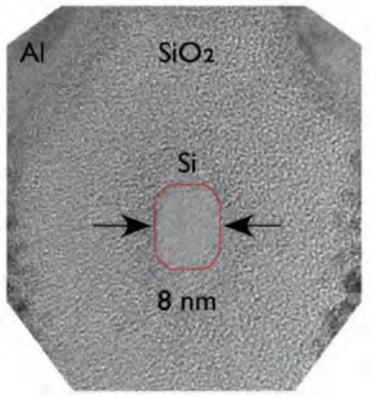


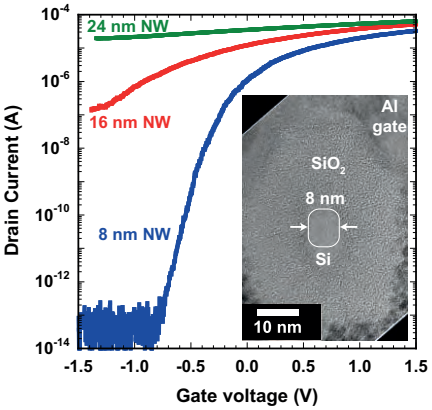
Outline

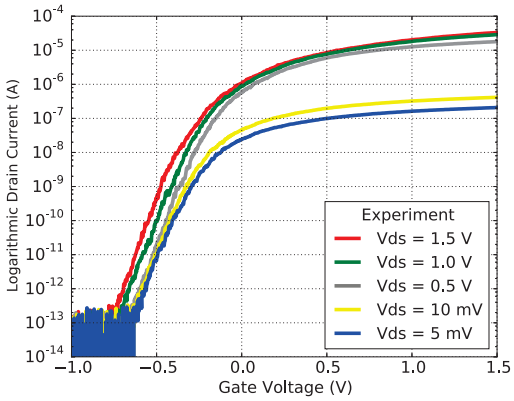
- Introduction
  - Project flow and link between the Work Packages
- Long range, short range and statistical variability
- Time-dependent variability
- **Statistical variability examples**
- Conclusions and outlook

Simulations of junctionless nanowires





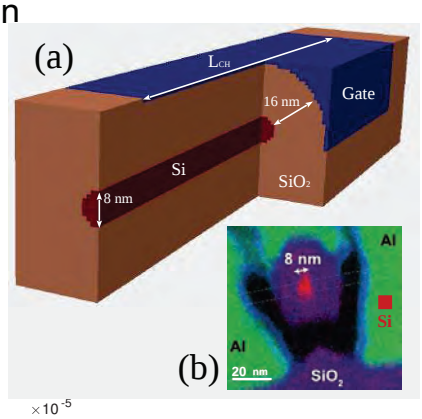


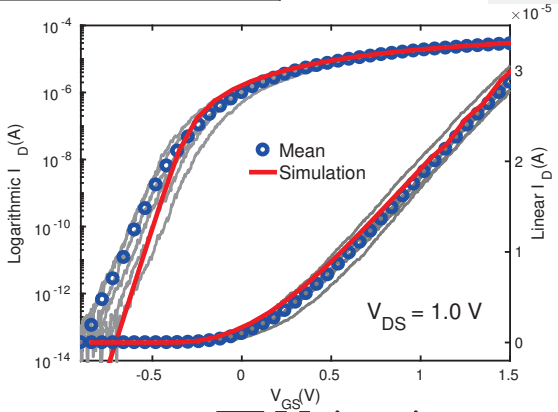


Simulations of junctionless nanowires

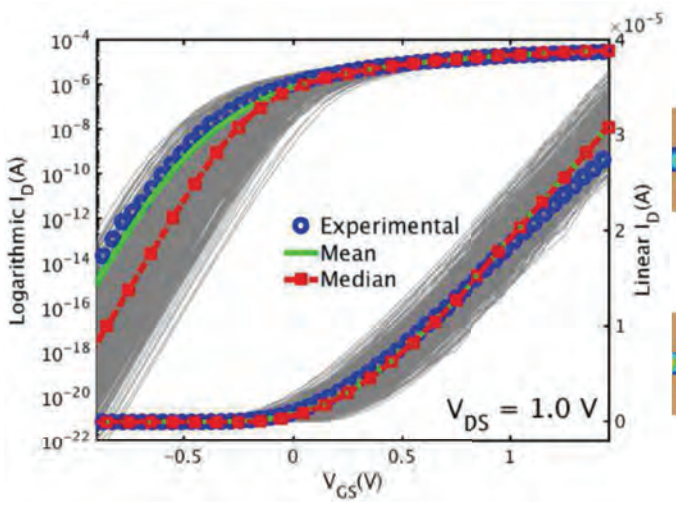
TCAD implementation

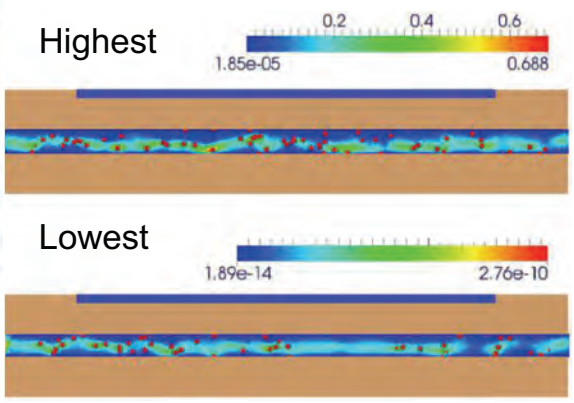
Si Nanowire	Parameters
Channel Diameter	8 nm
Channel Doping	1e19, 4e19,8e19 (donors)
Oxide thickness	16 nm
Gate Length	10, 25, 50, 100, 150 nm
V_D	5 mV and 1 V
Channel Length	150 nm





Simulations of junctionless nanowires

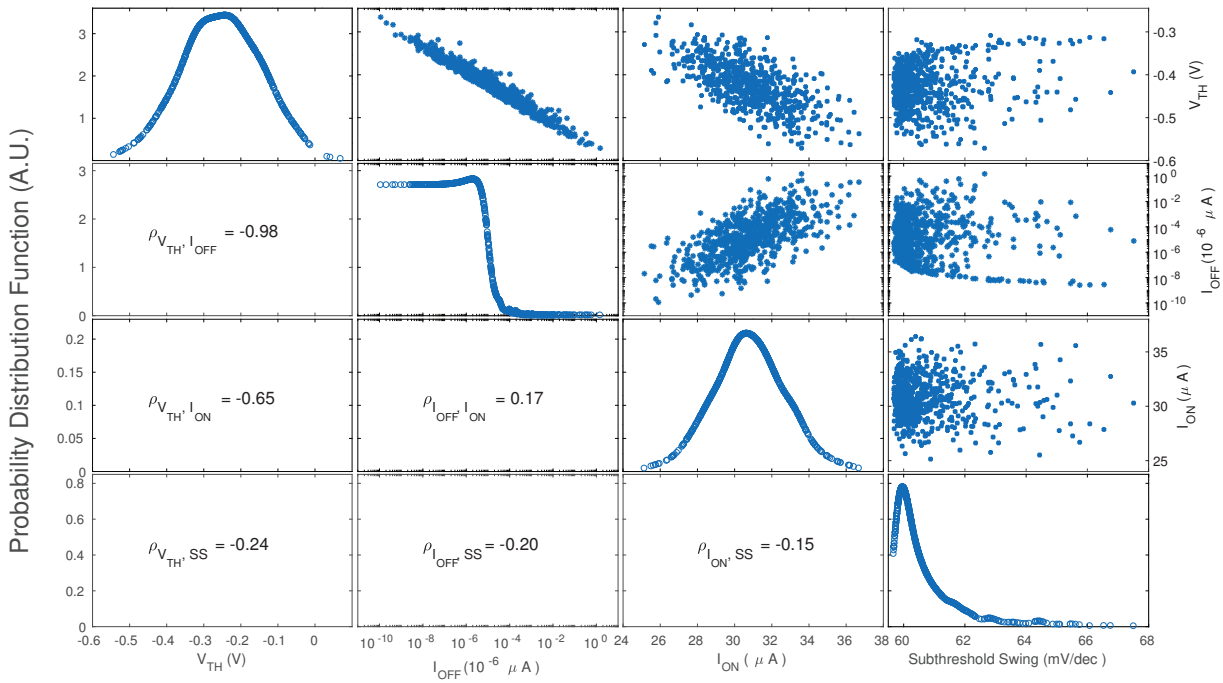




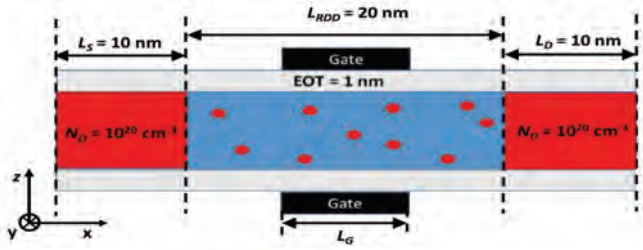
I_D–V_G characteristics of over 500 JL transistors with random distributed dopants. The last two are identical in the high gate bias region, e.g., V_G > 0 V, and in agreement with the experimental data.

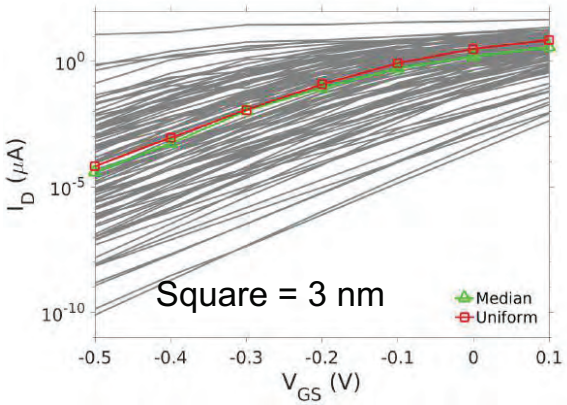
Simulated 3-D dopant position and current density contours corresponding to JL transistors with (a) the highest and (b) the low OFF-currents. Current density units are A/μ m^2.

Simulations of junctionless nanowires

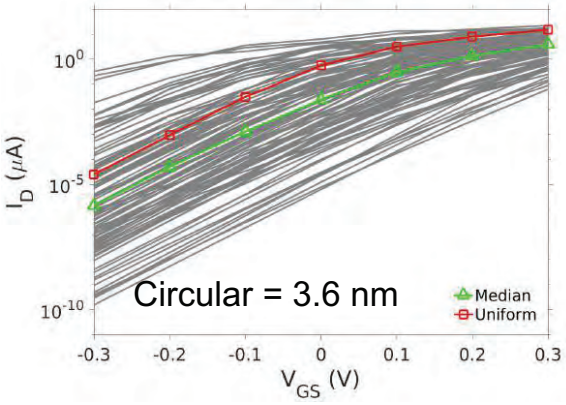


Simulations of junctionless nanowires





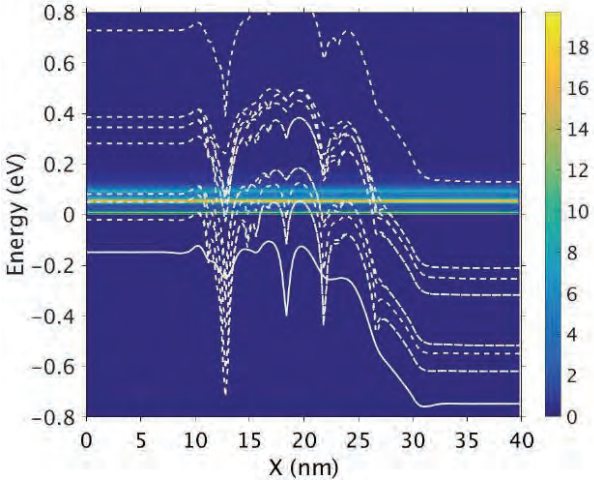
I_D-V_G characteristics at V_{DS} = 0.6 V for the device with a square cross-section and L_G = 10 nm.



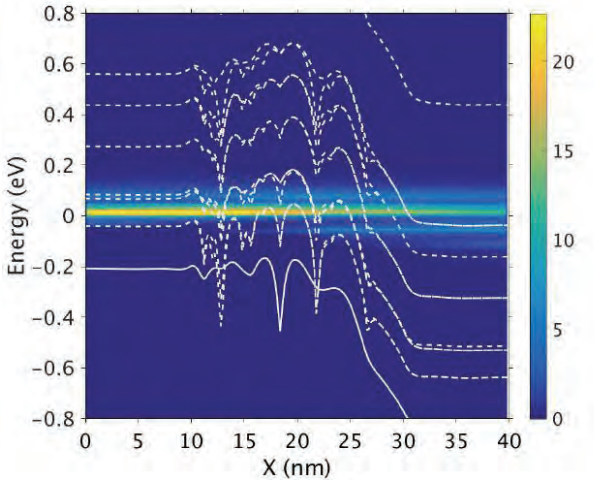
I_D-V_G characteristics at V_{DS} = 0.6 V for the device with a square cross-section and L_G = 5 nm.

Simulations of junctionless nanowires

Ballistic

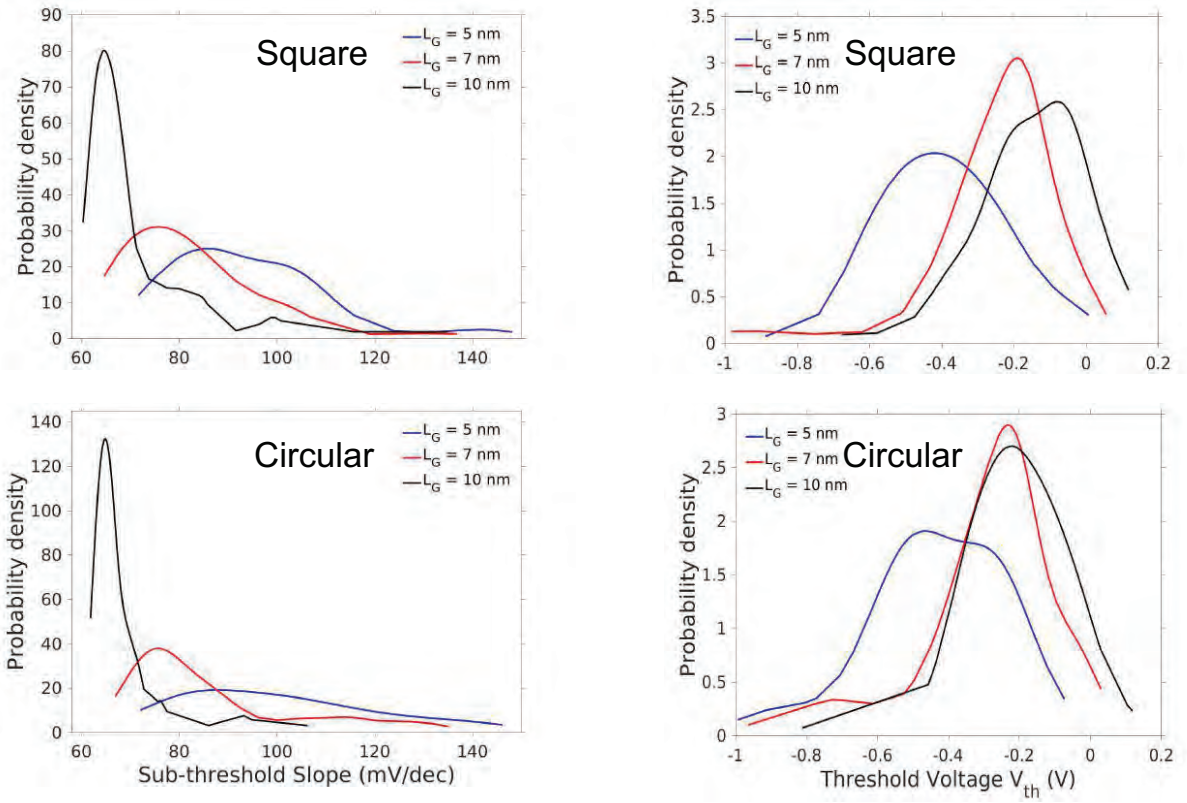


With phonons

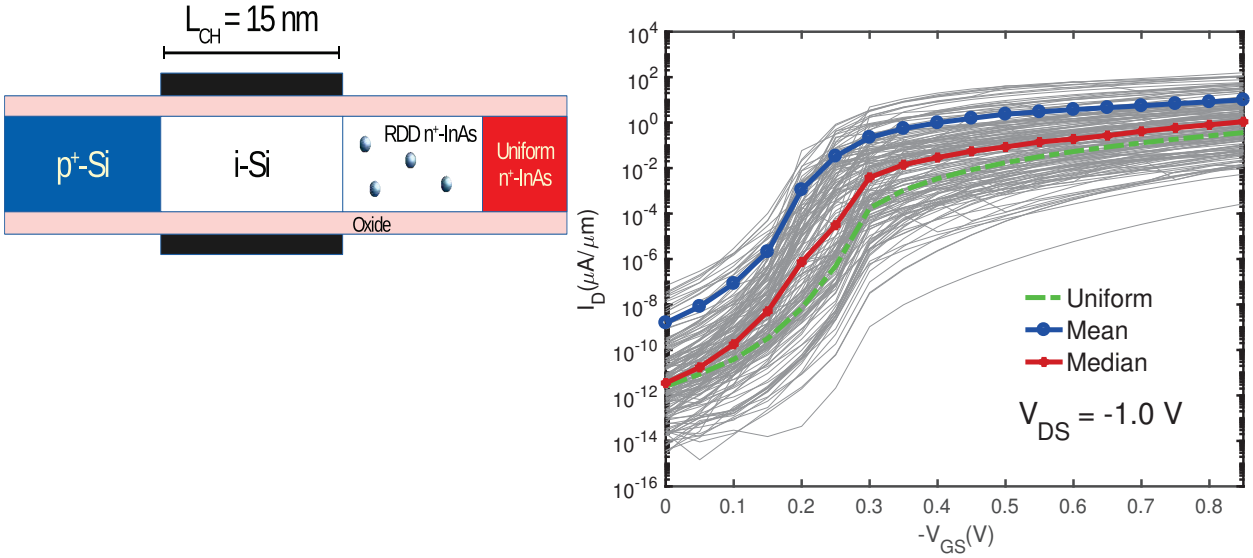


Current spectrum in μA/eV for the square device with L_G = 10 nm at V_{GS} = 0.3 V and V_{DS} = 0.6 V in ON-state (I_D = 13.59μA). The Fermi levels at the source and drain are respectively at 0 and -0.6 eV. The sub-bands are plotted in dashed lines. The solid line is the bulk conduction band in the middle of the device.

Simulations of junctionless nanowires

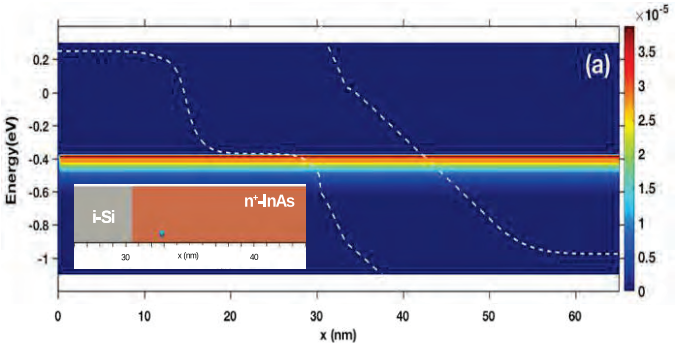


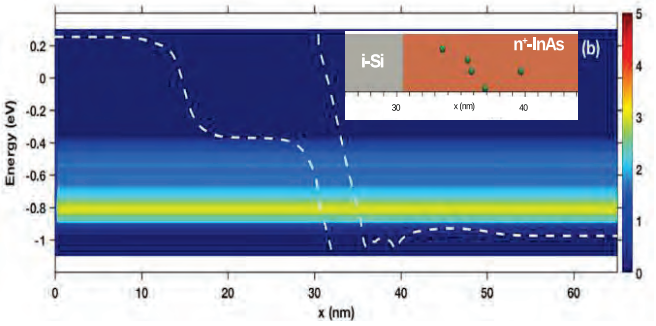
Simulations Si-InAs nanowire TFETs



$I_D - V_{GS}$ characteristics of the 150 Si-InAs nanowire TFETs with randomly distributed dopants (gray curves). The statistical mean and median are also plotted. The Si-InAs nanowire TFET with a uniform doping profile is shown as reference. The current is normalised by 2πR.

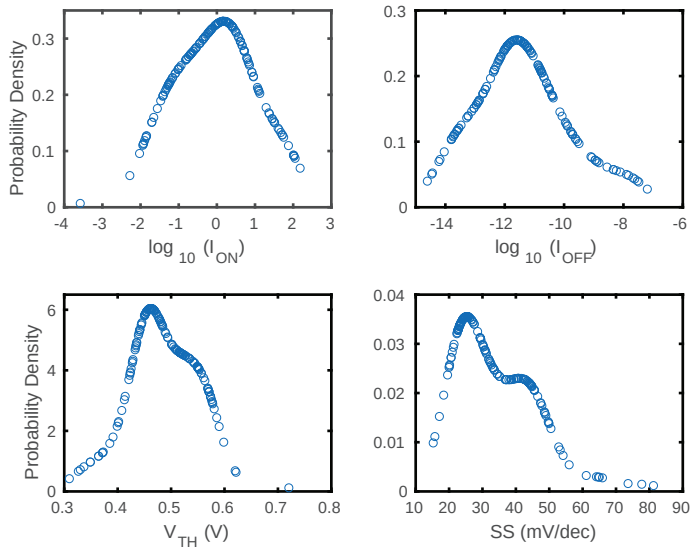
Simulations Si-InAs nanowire TFETs



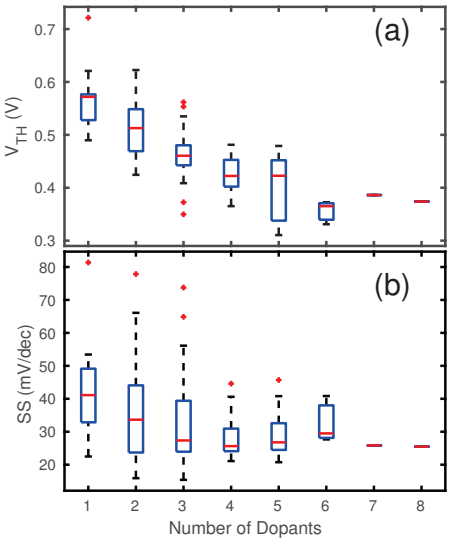


Simulated ON-state current-spectra of the Si-InAs nanowire TFETs with (a) one and (b) five dopants. The units are μA/eV. The insets show their position in each TFET. The white dashed-lines denote the highest valence and the lowest conduction sub-bands.

Simulations Si-InAs nanowire TFETs

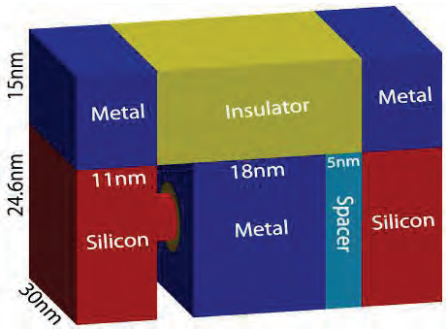


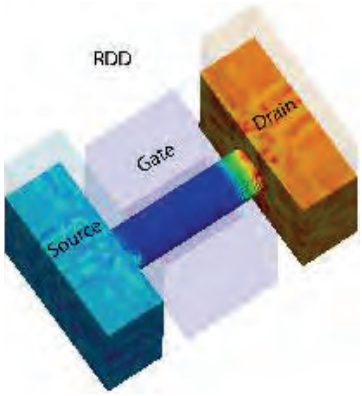
Probability density functions of the most important Figures of Merit obtained from the simulation of the ensemble of 150 Si-InAs nanowire TFETs.

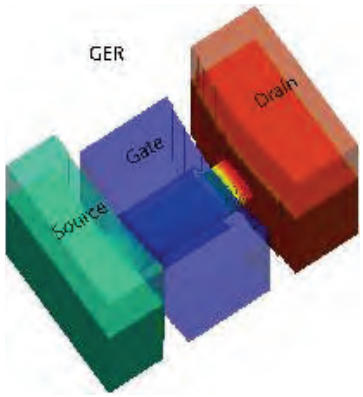


Statistical analysis of (a) threshold voltage and (b) subthreshold.

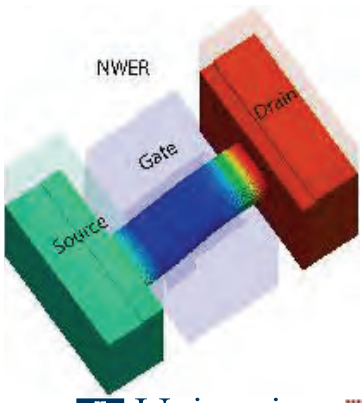
Statistical simulations of a Si nanowire transistor

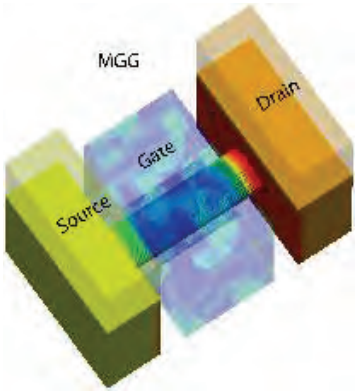




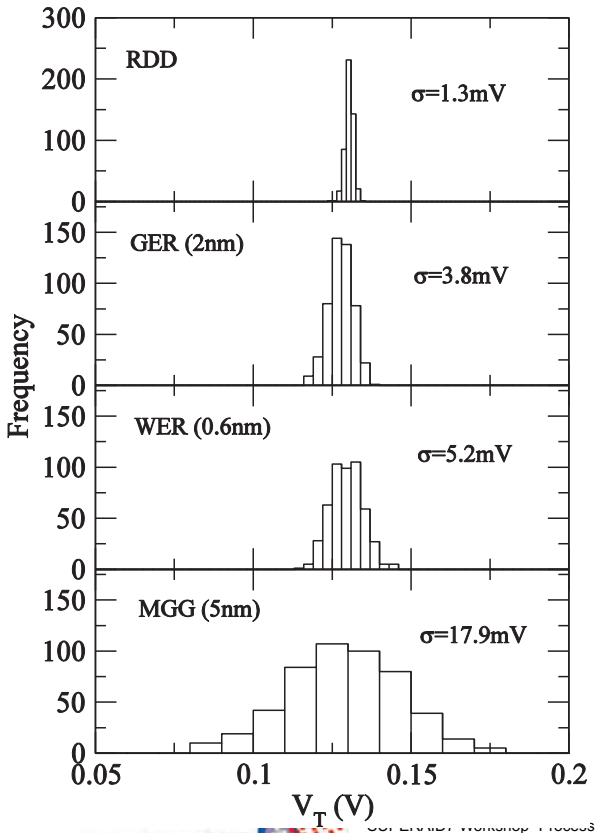


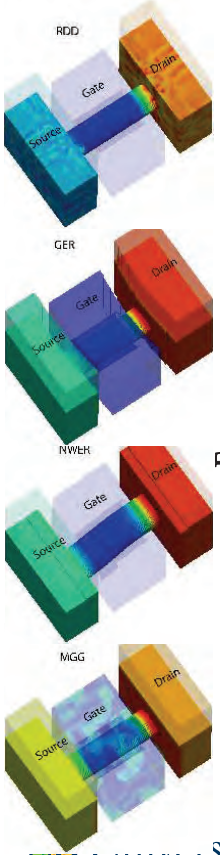
M2 Pitch	36nm
M1 Pitch	36nm
Gate Pitch	50nm
Fin Pitch	30nm
V_{DD}	0.7V
EOT	1.2nm
Leakage	3nA/μA

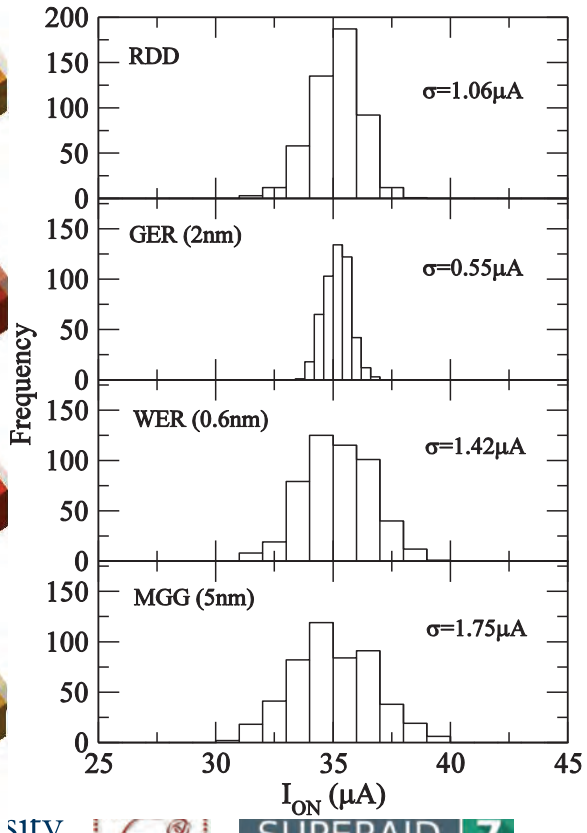




Statistical simulations of a Si nanowire transistor 1000 devices

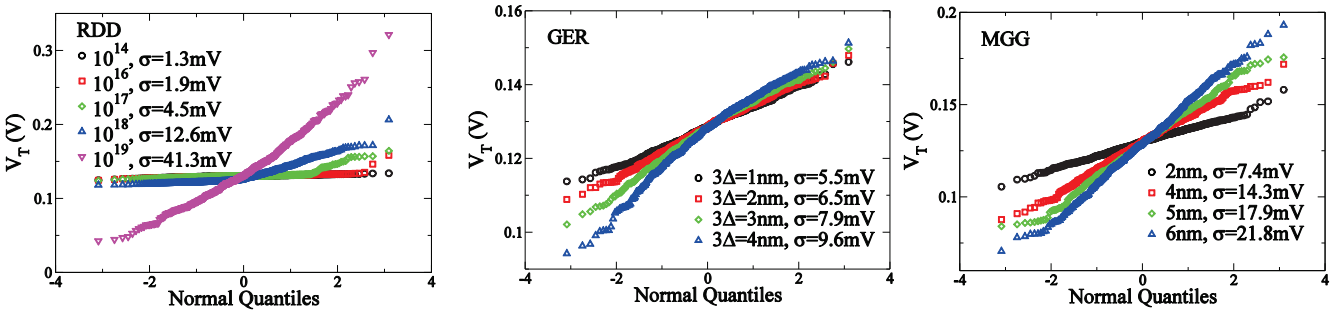




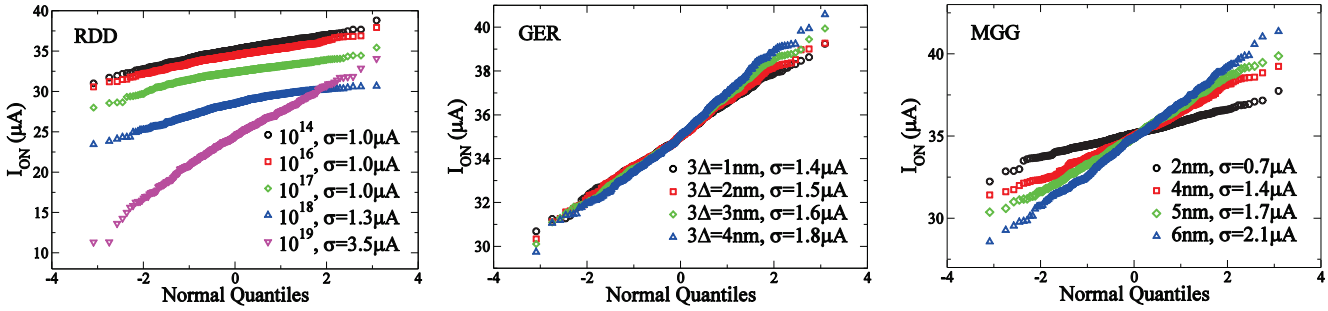


Statistical simulations of a Si nanowire transistor

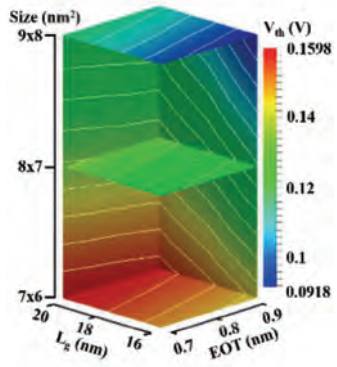
V_T – variability



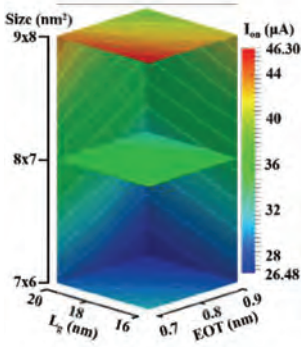
I_{ON} – variability

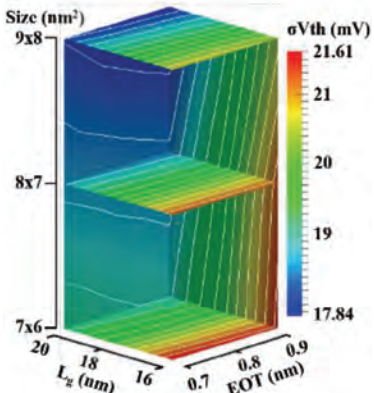


Statistical simulations of a Si nanowire transistor

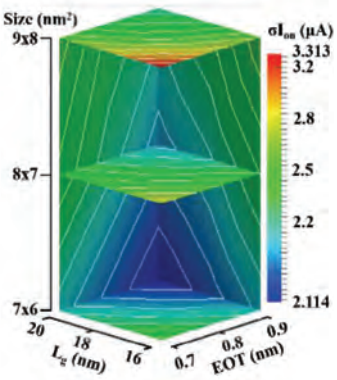


Global Variability





Local &
Global Variability



Conclusions and outlook

- Variability is one of the major challenges associated with scaling
- There is global and local variability
  - Local (statistical) variability has significant impact on the current technology
  - Sources of variability: RDD, MGG, GER, NWER
- Variability should be taken into account in design and fabrication process

Leti-NSP model: SPICE model for advanced multigate MOSFETs

O. Rozeau, T. Poiroux, S. Martinie, J. Lacord, F. Triozon, S. Barraud and J.C. Barbé, CEA-Leti, Grenoble, France

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

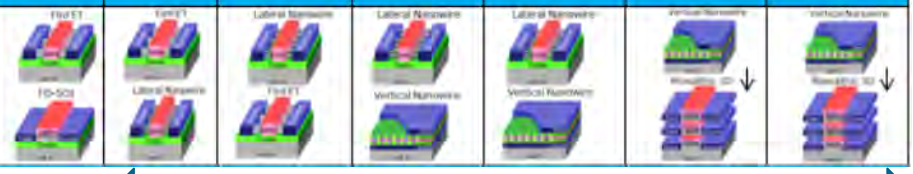
September 3, 2018, Dresden, Germany

Outline

- Introduction
- Innovative solution for SPICE modeling
- Quantum confinement and mobility models
- Model features
- Model validation
- Code and user’s manual
- Conclusion and outlook

Introduction

- Context: more Moore from International Roadmap for Devices and Systems

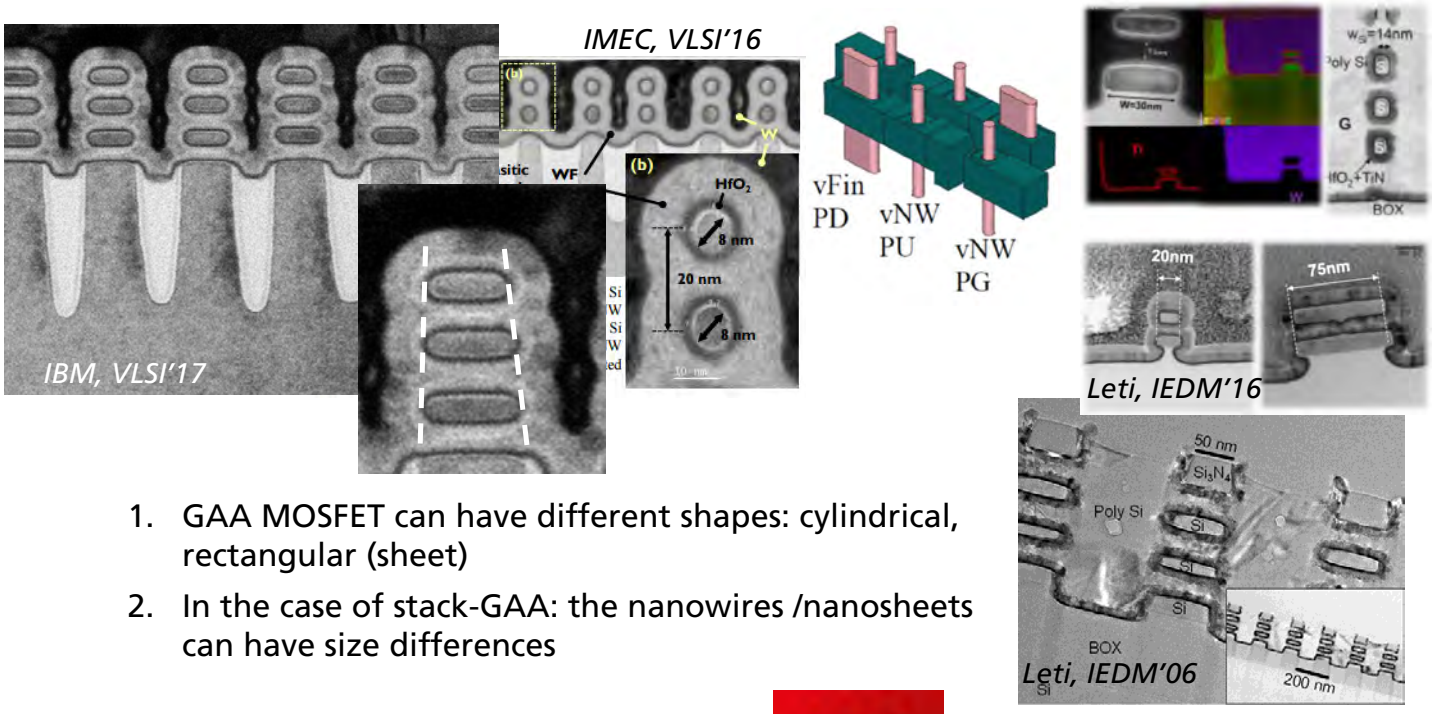
YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							
LGAA = Vertically stacked NS/NW GAA MOSFET *VGAA = Vertical NS/NW GAA MOSFET*							

From irds.ieee.org: More Moore report 2017 edition

- Advanced Gate All Around (GAA) MOSFET are introduced for sub-7nm nodes: require SPICE models for IC design

Introduction

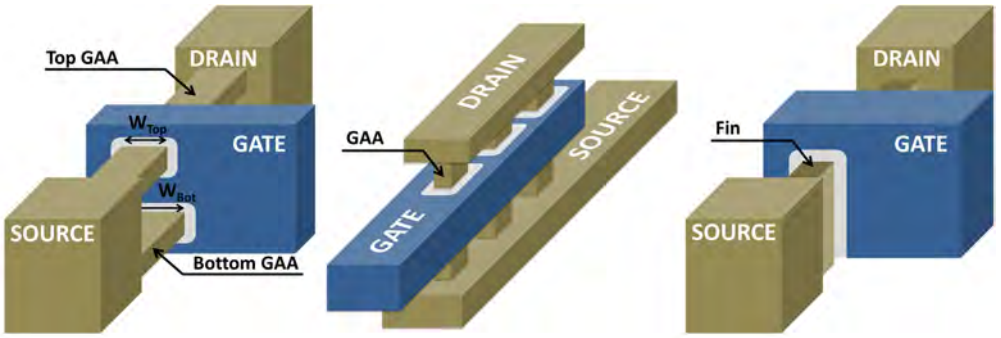
- Challenges of GAA MOSFET modeling



1. GAA MOSFET can have different shapes: cylindrical, rectangular (sheet)
2. In the case of stack-GAA: the nanowires /nanosheets can have size differences

Introduction

- Our solution is Leti-NSP model dedicated to advanced multigate MOSFET.
- Leti-NSP model can simulate:
  - Vertically stacked GAA MOSFET (nanosheet and/or nanowire)
  - Vertical channel GAA MOSFET (nanosheet and/or nanowire)
  - FinFET / Trigate MOSFET



Vertically stacked GAA MOSFET | *Vertical channel GAA MOSFET* | *FinFET/Trigate MOSFET*

Introduction

- Model's core: modeling of vertically stacked GAA is complex and challenging
- Main goals: find a compact formalism for
  - Accuracy: physical approach
  - CPU time efficiency: single instance
- Main difficulties:
  - the surface potential is not constant along the NW/NS perimeter
  - GAA can have different sizes: surface potentials are not the same for all GAA

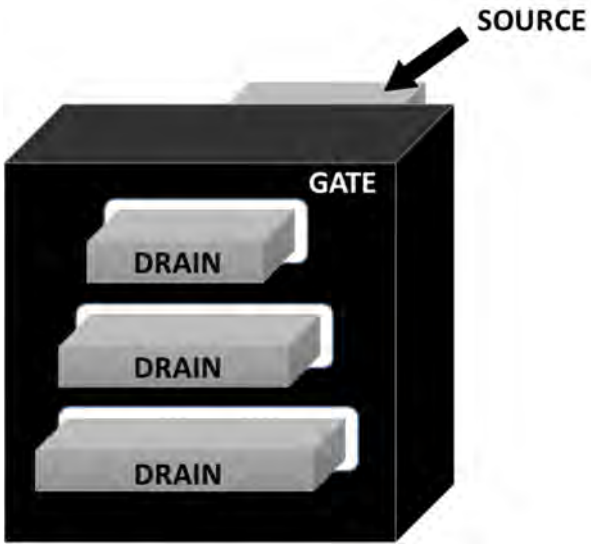
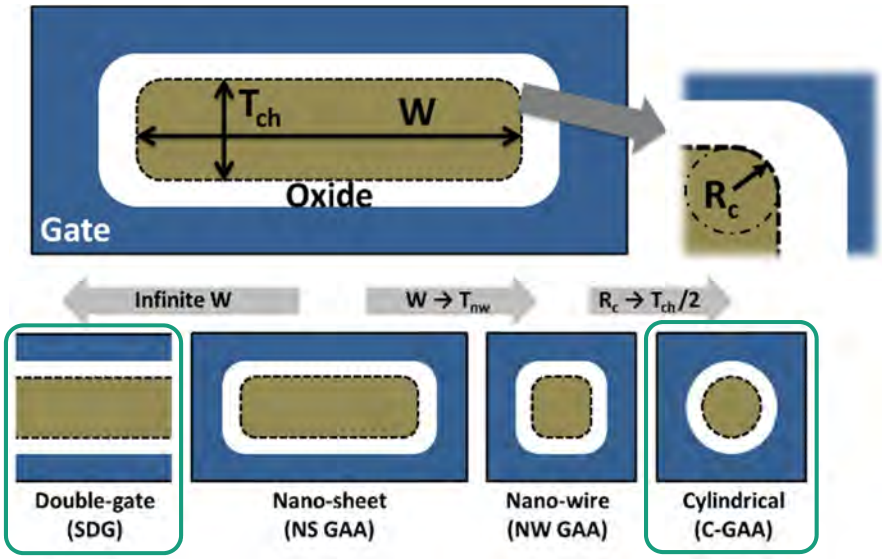


Illustration of vertically stacked GAA MOSFET: 3 Nanosheets

Innovative Solution for SPICE Modeling

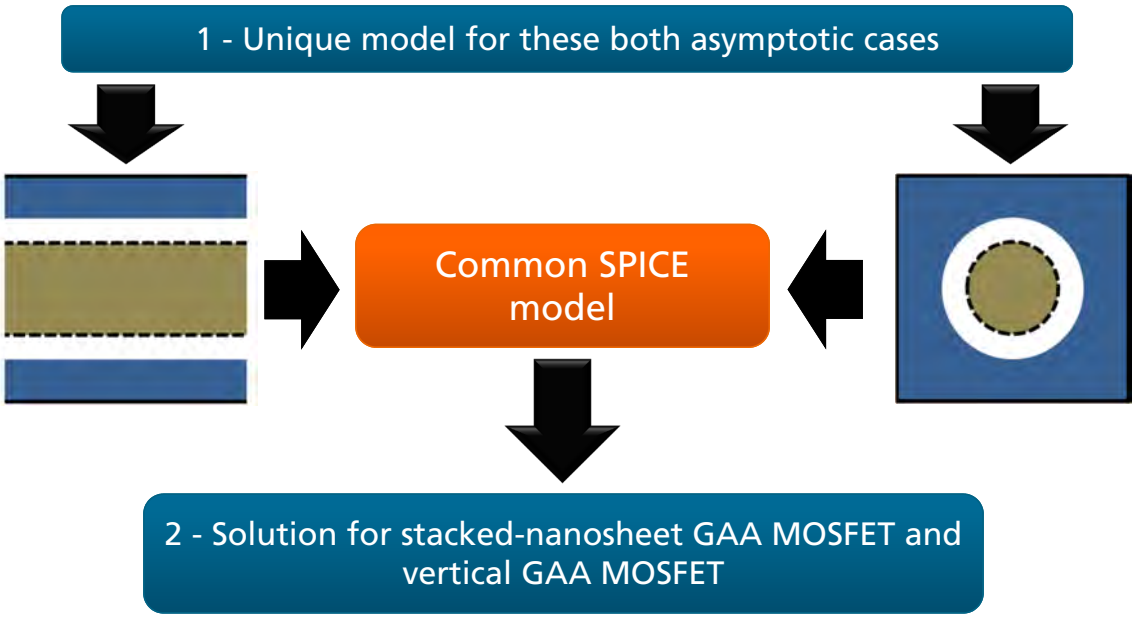
- Concept of Leti-NSP model: GAA MOSFET architecture and its asymptotic cases



- 2 asymptotic cases: Symmetrical double gate and cylindrical GAA MOSFET

Innovative Solution for SPICE Modeling

- Concept of Leti-NSP model: GAA MOSFET architecture and its asymptotic cases



SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

Innovative Solution for SPICE Modeling

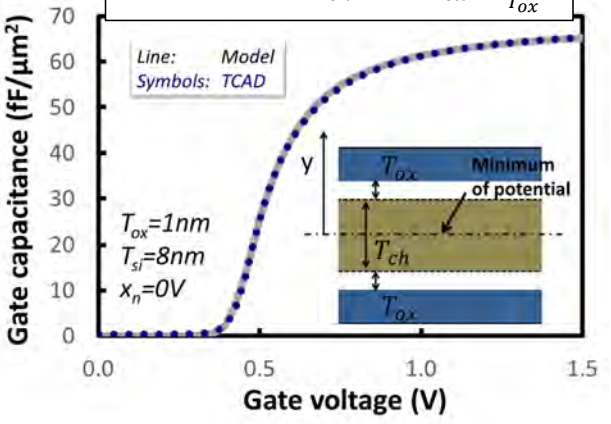
- Asymptotic cases: unique equation (Poisson's equation + boundary conditions)

$$(x_g - x)^2 + \frac{4 \cdot \varepsilon_{si}}{H \cdot C'_{ox}} \cdot (x_g - x) = \delta \cdot exp(x - x_n)$$

See O. Rozeau et al, IEDM'16

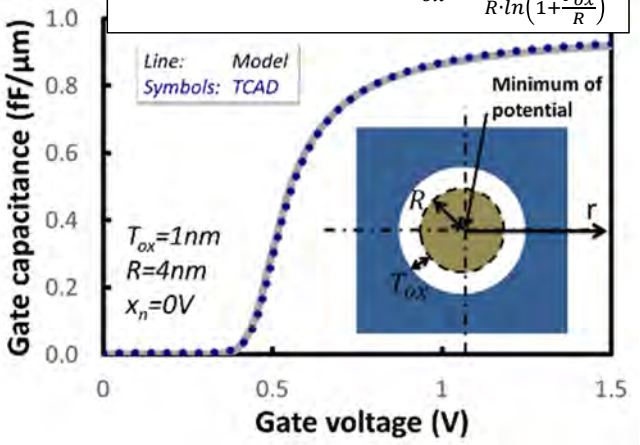
Planar SDG

$W = 1\mu m$, $H = T_{ch}$ and $C'_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}$



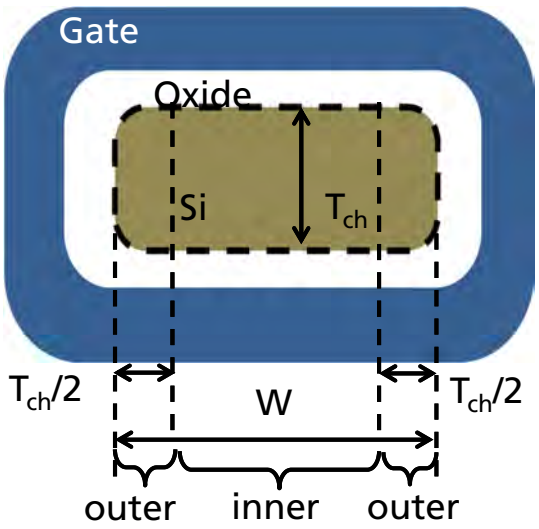
Cylindrical

$W = 2\pi R$, $H = R$ and $C'_{ox} = \frac{\varepsilon_{ox}}{R \cdot ln\left(1+\frac{T_{ox}}{R}\right)}$



Innovative Solution for SPICE Modeling

- Nanosheet GAA MOSFET partitioning



Outer parts: W_{outer} , $C'_{ox,outer}$, H_{outer}

Inner part: W_{inner} , $C'_{ox,inner}$

$$W_{eff} = W_{outer} + W_{inner}$$

$$H = \frac{W_{outer}}{W_{eff}} \cdot H_{outer} + \frac{W - T_{ch}}{W_{eff}} \cdot T_{ch}$$

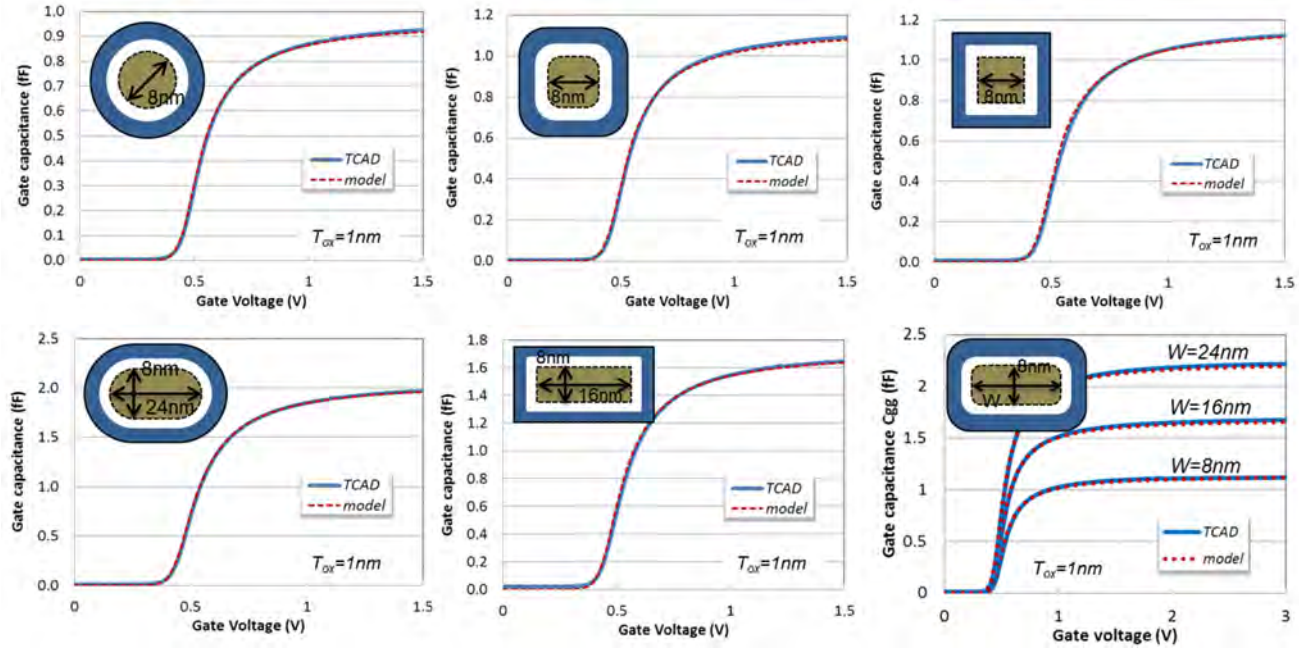
$$C'_{ox} = \frac{W_{outer}}{W_{eff}} \cdot C'_{ox,outer} + \frac{W - T_{ch}}{W_{eff}} \cdot C'_{ox,inner}$$

$$C'_{si} = \frac{\varepsilon_{si}}{H}$$

- Innovative solution in NSP model: an unique effective surface potential is obtained by the resolution of an unified equation for nanosheet

Innovative Solution for SPICE Modeling

- NSP-model can reproduced all GAA shapes without fitting parameters



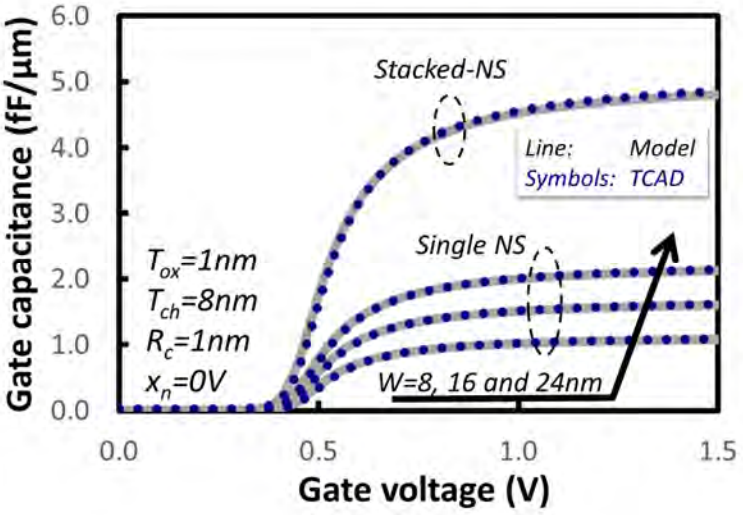
Innovative Solution for SPICE Modeling

- Case of stacked-nanosheet GAA MOSFET

$$C'_{ox} = \sum_{i=1}^{N_W} \frac{W_i}{W_{total}} \cdot C'_{ox,i}$$

$$H = \sum_{i=1}^{N_W} \frac{W_i}{W_{total}} \cdot H_i$$

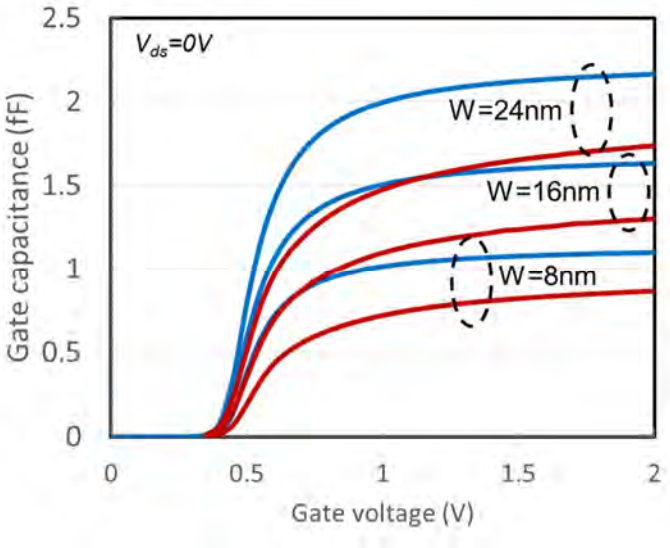
$$W_{total} = \sum_{i=1}^{N_W} W_i$$



- The inversion charge is accurately and analytically modeled without fitting parameters

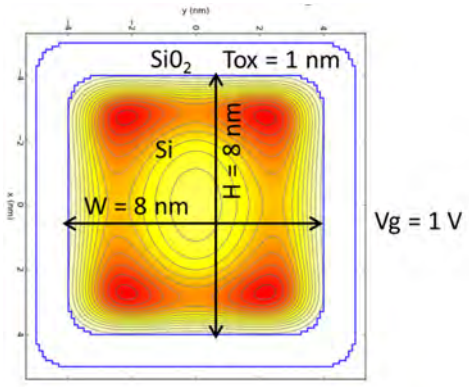
Quantum Confinement and Mobility Models

- Case of stacked-nanosheet GAA MOSFET



Blue: classical TCAD simulations

Red: 2D Poisson-Schrödinger



Simulations: TB_SIM

- Effective mass: 6 bands k.p (higher than 10 sub-bands are solved)

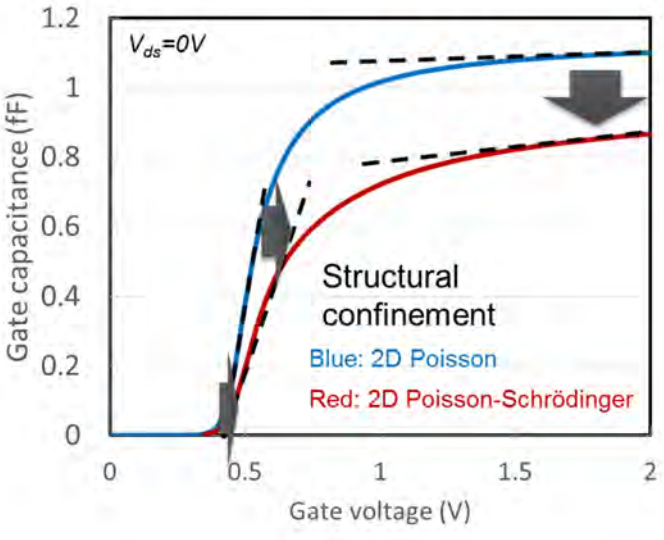
- Quantum confinement has a significant impact on the inversion charge

Quantum Confinement and Mobility Models

- Dedicated compact model for GAA MOSFET (IEDM'16)

- Triangular-potential approximation (Stern 72)

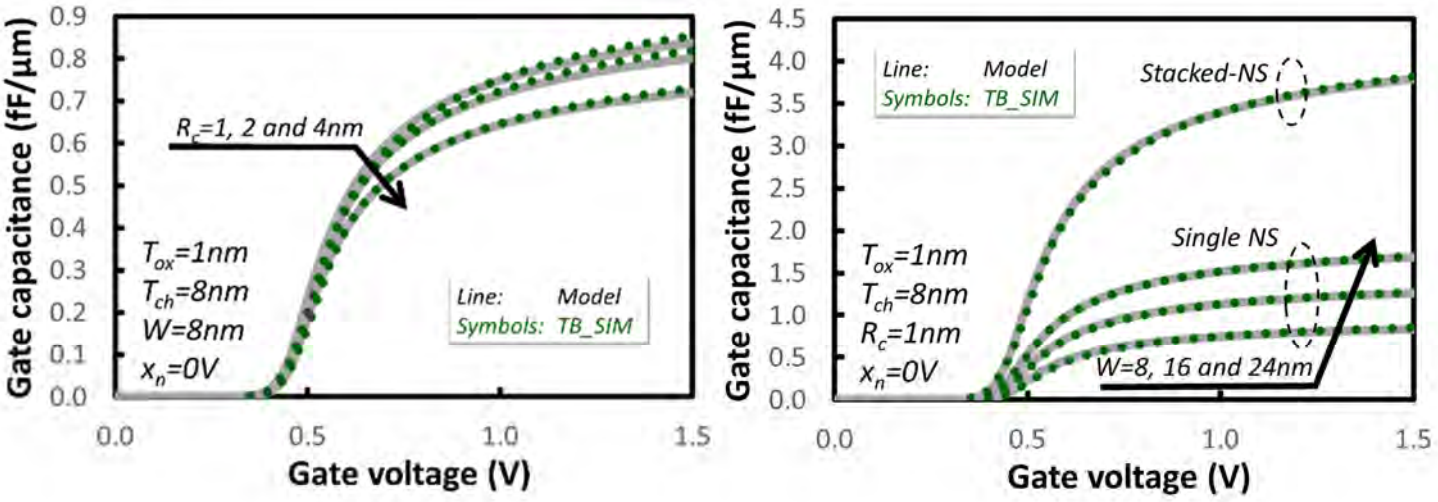
- Structural confinement has a stronger impact on C_{inv} in GAA than in planar bulk MOSFET



- For Leti-NSP model: <u>dedicated solution</u> including accurate modeling of Cgg slope without fitting parameter for the user

Quantum Confinement and Mobility Models

- MODEL versus Simulations: Stacked-NS MOSFET (IEDM'16)

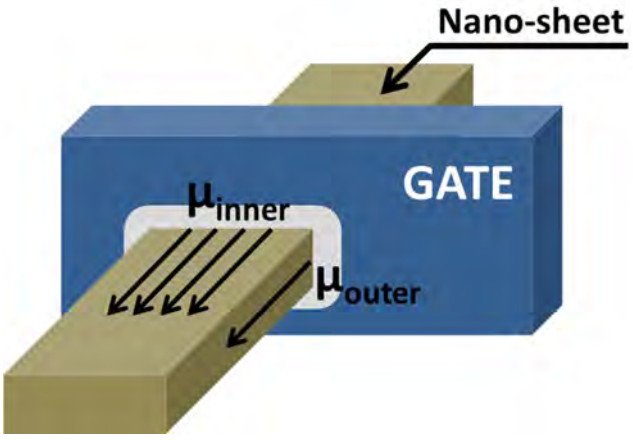


- Single effective mass: defined as a function of device polarity, Si orientation and Ge concentration for pFET <u>without fitting parameters</u> for users

Quantum Confinement and Mobility Models

- Mobility partitioning in GAA MOSFET

- In NSP model, 2 distinct mobility models is implemented for inner part and outer parts



$$\mu_{inner} = \frac{\mu_0}{1 + \left(f_{\mu E} \cdot E_{eff}\right)^{\theta_\mu} + C_S \cdot \left(1 + \frac{q_{ieff}}{q_{ith}}\right)^{-\theta_{CS}}}$$

$$\mu_{outer} = \frac{\mu_{0S}}{1 + \left(f_{\mu ES} \cdot E_{eff}\right)^{\theta_{\mu S}} + C_{SS} \cdot \left(1 + \frac{q_{ieff}}{q_{ith}}\right)^{-\theta_{CSS}}}$$

High field effect

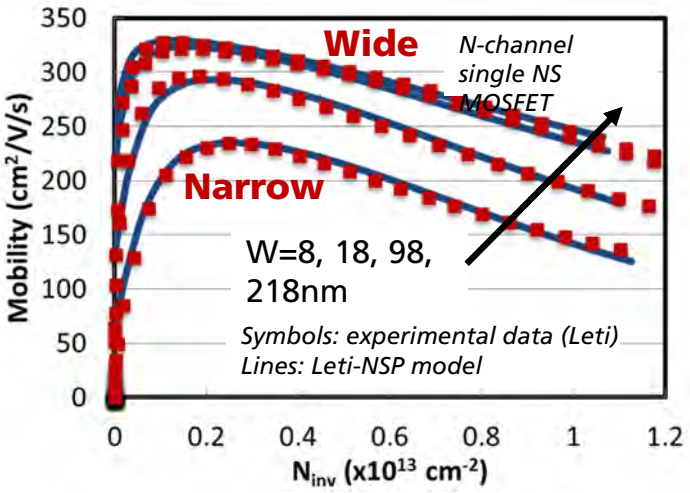
Coulomb scattering

- For model accuracy, quantum confinement is included in the inversion charge and electrical field calculations

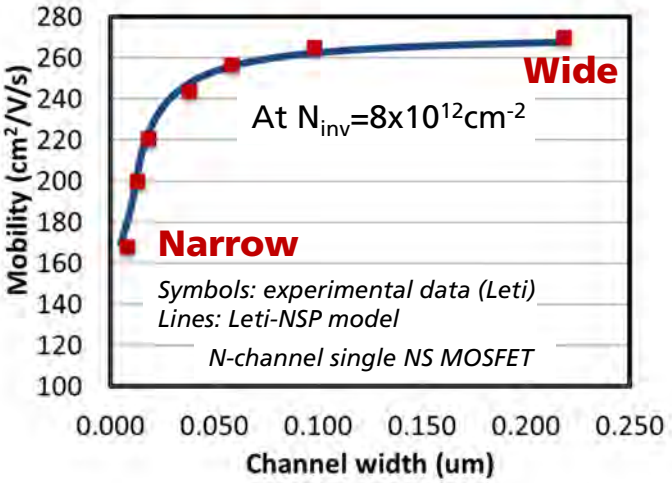
Quantum Confinement and Mobility Models

- Model evaluation: nfet

Electrical field dependence



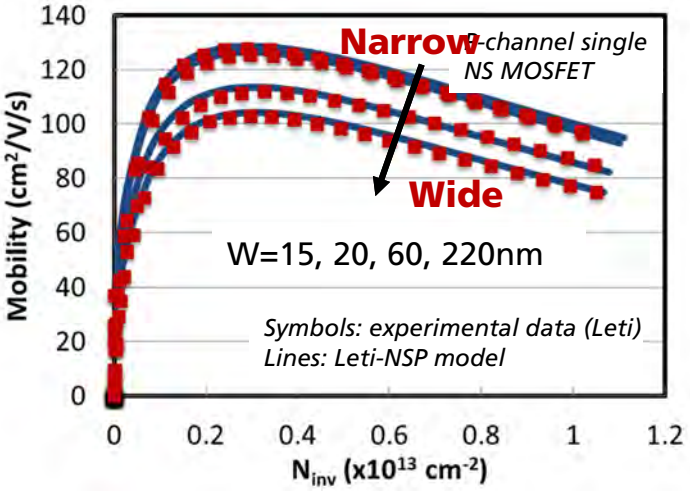
Width dependence



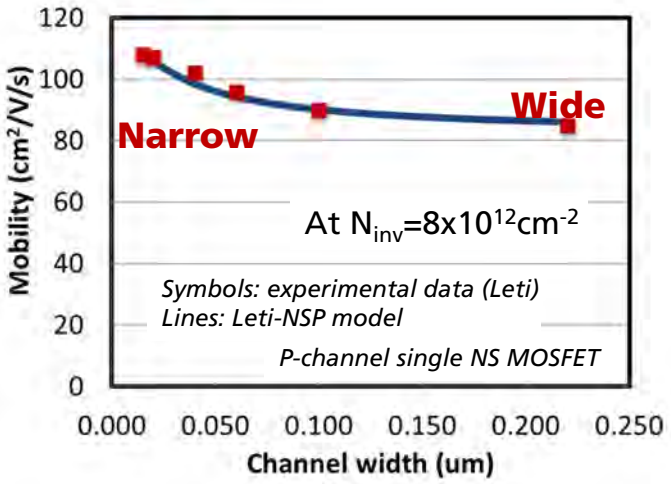
Quantum Confinement and Mobility Models

- Model evaluation: pfet

Electrical field dependence



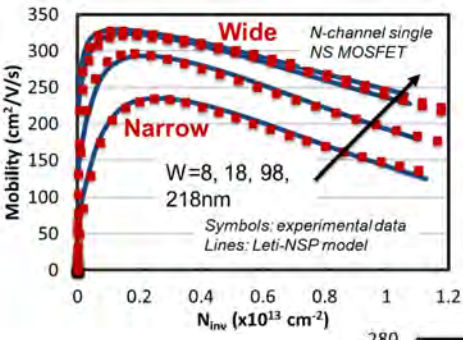
Width dependence



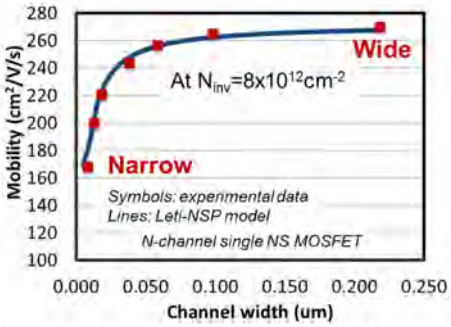
Overview of Model Features

- For all device sizes

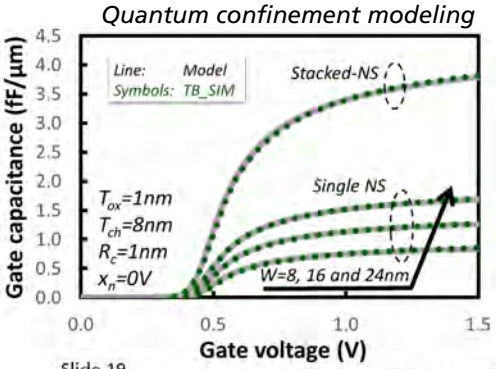
Model features: Leti-NSP model v1.0.0
Interface states
Quantum mechanical effect (confinement)
Channel doping effect
Management of SiGe channel for pfet
Mobility model including sidewall effects
Temperature scaling and self-heating effect



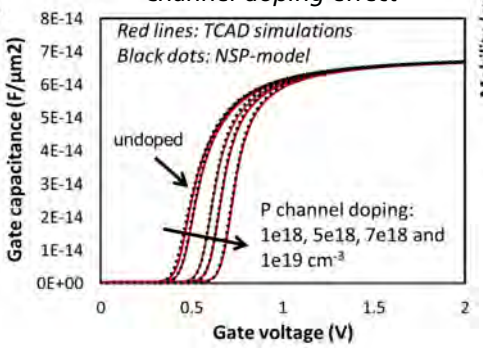
Mobility model including sidewall effects



Quantum confinement modeling



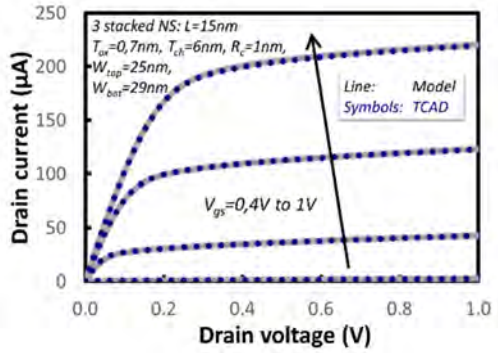
Channel doping effect

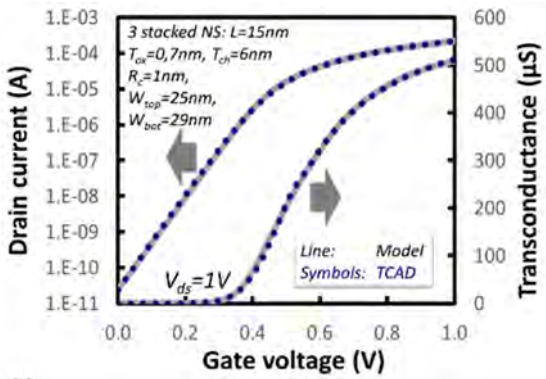


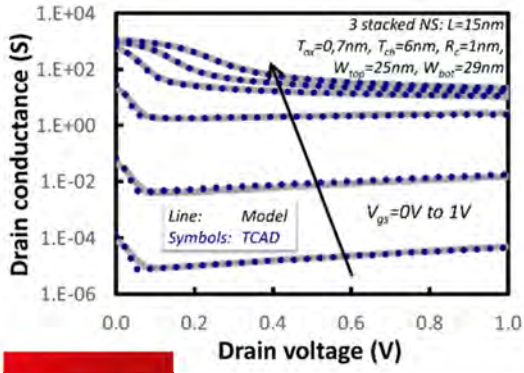
Overview of Model Features

- Short channel effects

Model features: Leti-NSP model v1.0.0
Threshold voltage roll-off
L-scaling of mobility model
Drain Induced Barrier Lowering
Velocity saturation
Channel length modulation in saturation
Series resistances with bias dependence





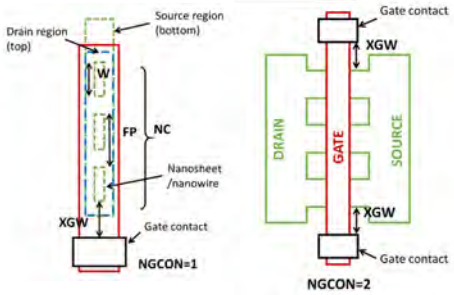


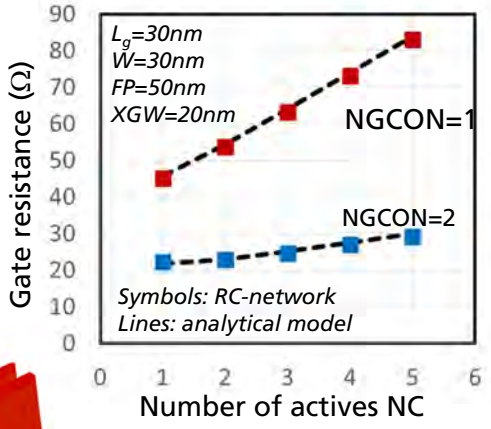
Overview of Model Features

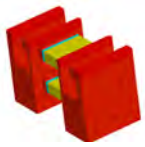
- Other parasitic effects

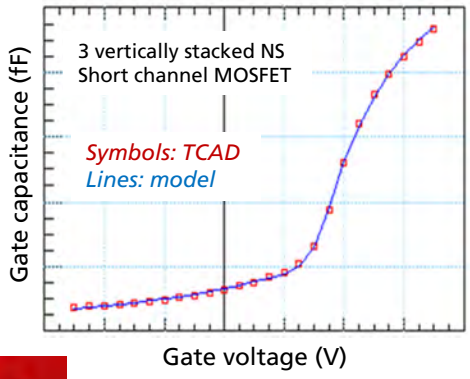
Model features: Leti-NSP model v1.0.0
Inner and Outer fringe capacitances
All external parasitic capacitances including device to substrate capacitances
External access resistances
Gate resistance with scaling effects
Gate tunneling currents
GIDL/GISL currents
Junction currents and charges

Dedicated instance parameters for all GAA geometries







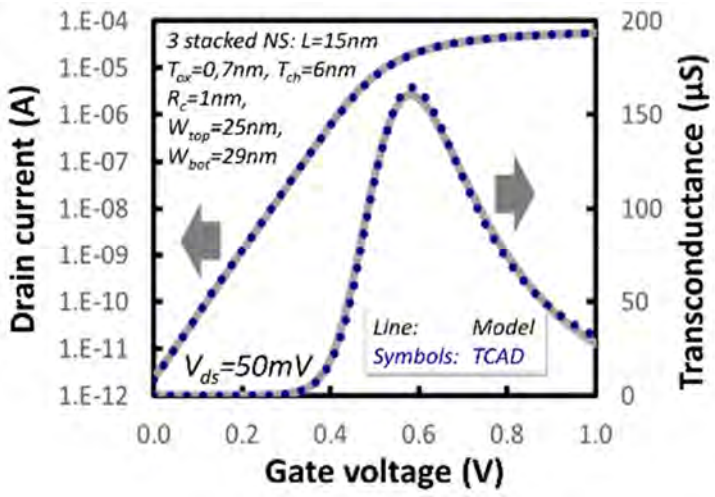


Model Validation

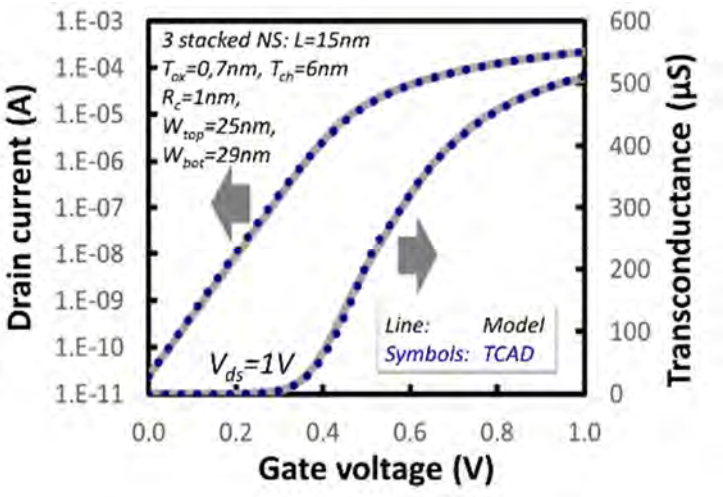
- MODEL versus TCAD simulations from Leti

Example of drain current and transconductance versus gate voltage

Linear



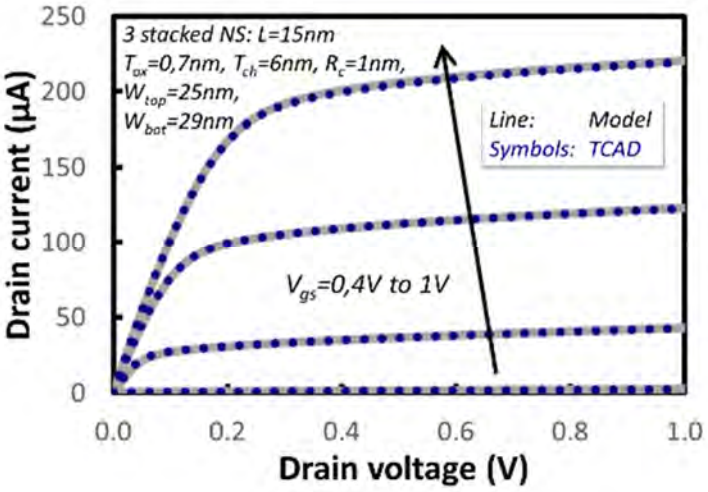
Saturation

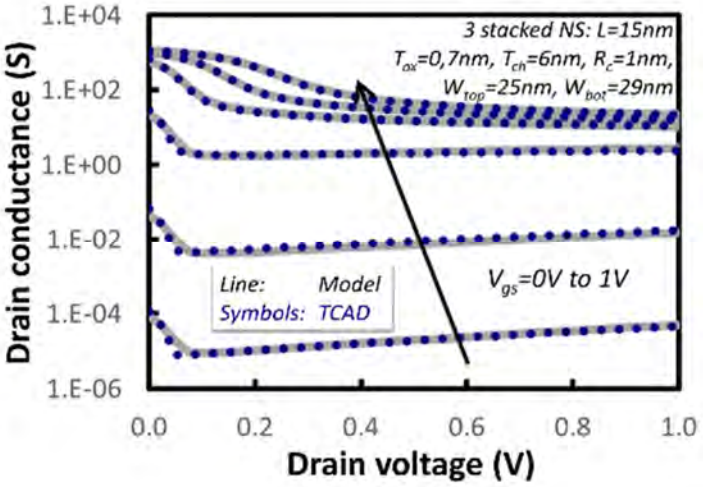


Model Validation

- MODEL versus TCAD simulations from Leti

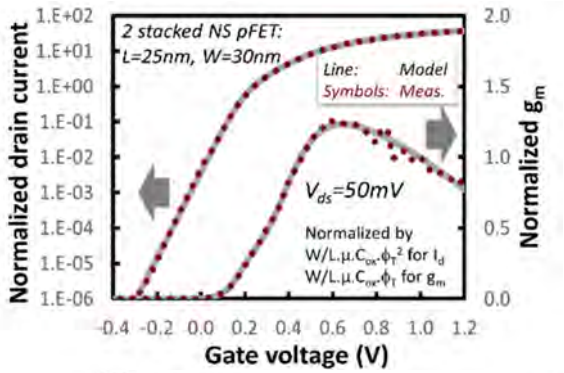
Example of drain current and drain conductance versus drain voltage

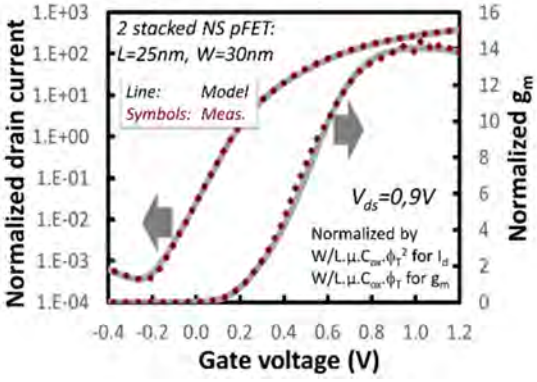


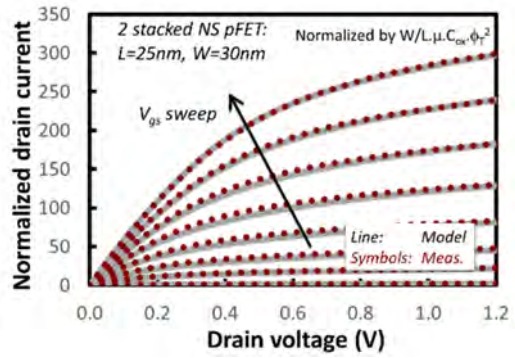


Model Validation

- Experimental data from Leti







Note: other validations on hardware have been done but can't show here (confidential)

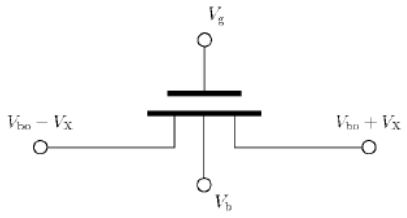
Model Validation

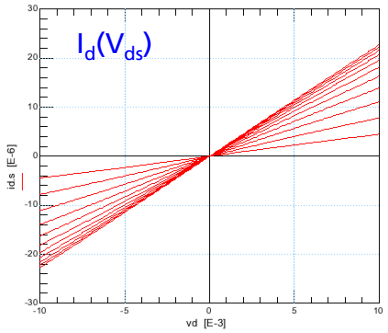
- Leti-NSP model versus standard model requirements

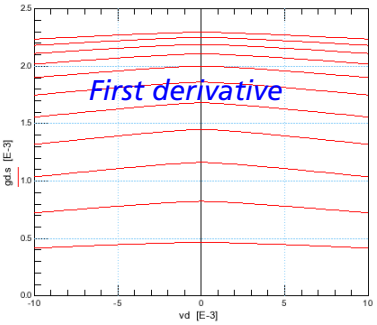
Requirements	Leti-NSP	Comments
Physical representation (currents, charges and derivatives)	√	See previous slides
2nd and 3rd continuous derivatives in all transitions and regimes	√	Checked
Symmetry and Gummel test	√	See next slide
Large signal analysis	√	By model itself
No model defects	√	Not detected
Model calculation efficiency	√	Optimized code
Physical and structurally meaningful model parameters	√	Physical model
Geometrical scaling	√	Done
Empirical parameters	√	Similar to PSP model
Model binning	√	Next release
Model extraction efficiency	√	Optimized and checked on several extractions
Operating Point output	√	Done

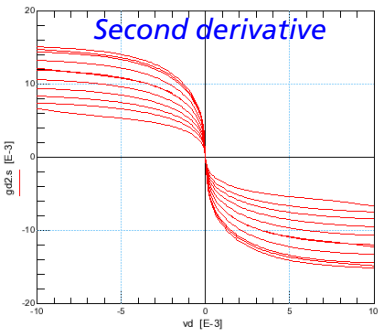
Model Validation

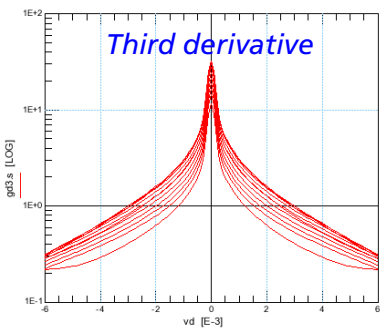
- Leti-NSP mode: symmetry test at near to V_{ds}=0V







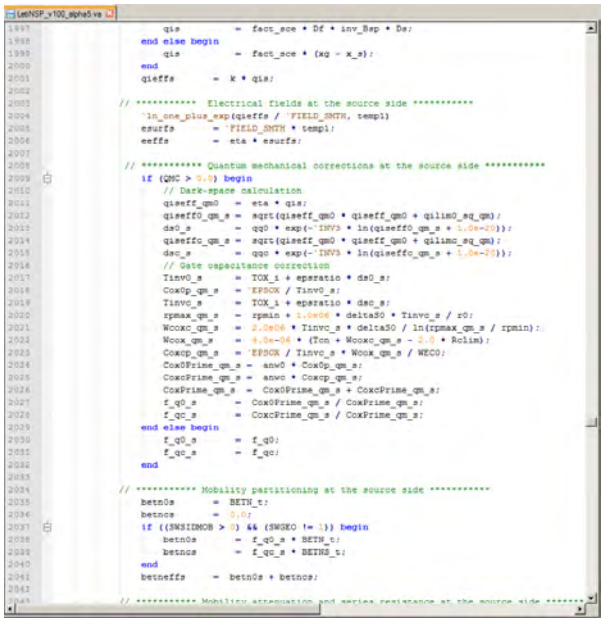




Gummel test is ok with all effects activated.

Code and User's Manual

- Leti-NSP model: code and manual are available - ready for IC design



Conclusions and Outlook

- History:
  - Model development has been started in 2015
  - 6 versions were provided to our partners (use in PDK)
- For next releases, we plan to include:
  - binning parameters
  - noise models (Flicker, thermal and induced gate noise)
  - model for junction-less MOSFET (dev. on going)
  - non-quasi static effects
  - model for tunnel-FET (partially dev.)
- Leti-NSP model is available and compatible with the CMC requirement for standardization

Simulation Tools for DTCO of Advanced Technology Nodes

Campbell Millar, Synopsys, Glasgow, UK

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

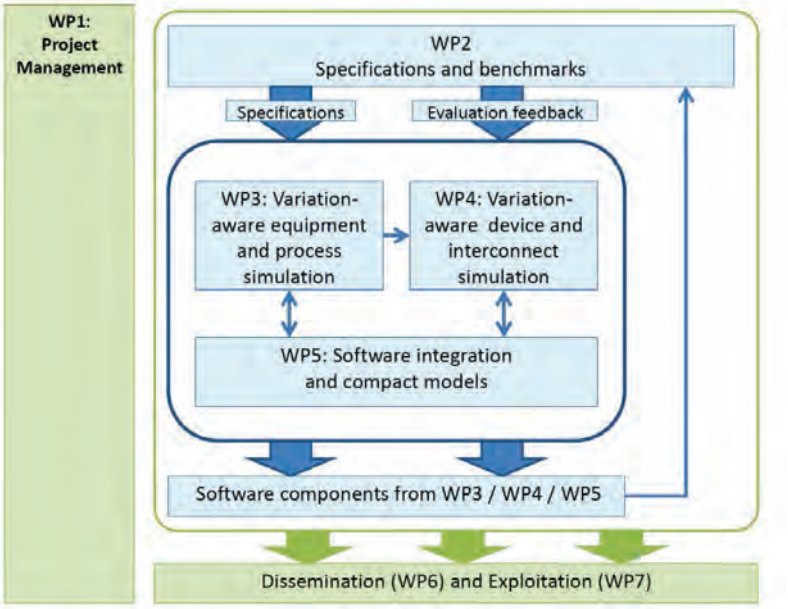
September 3, 2018, Dresden, Germany

Outline

- Introduction
  - Project Context and Goals
- DTCO and Technology
- Tools and Software for DTCO
- Example FinFET PPY Analysis
- Conclusions and Outlook

Introduction – Project Context

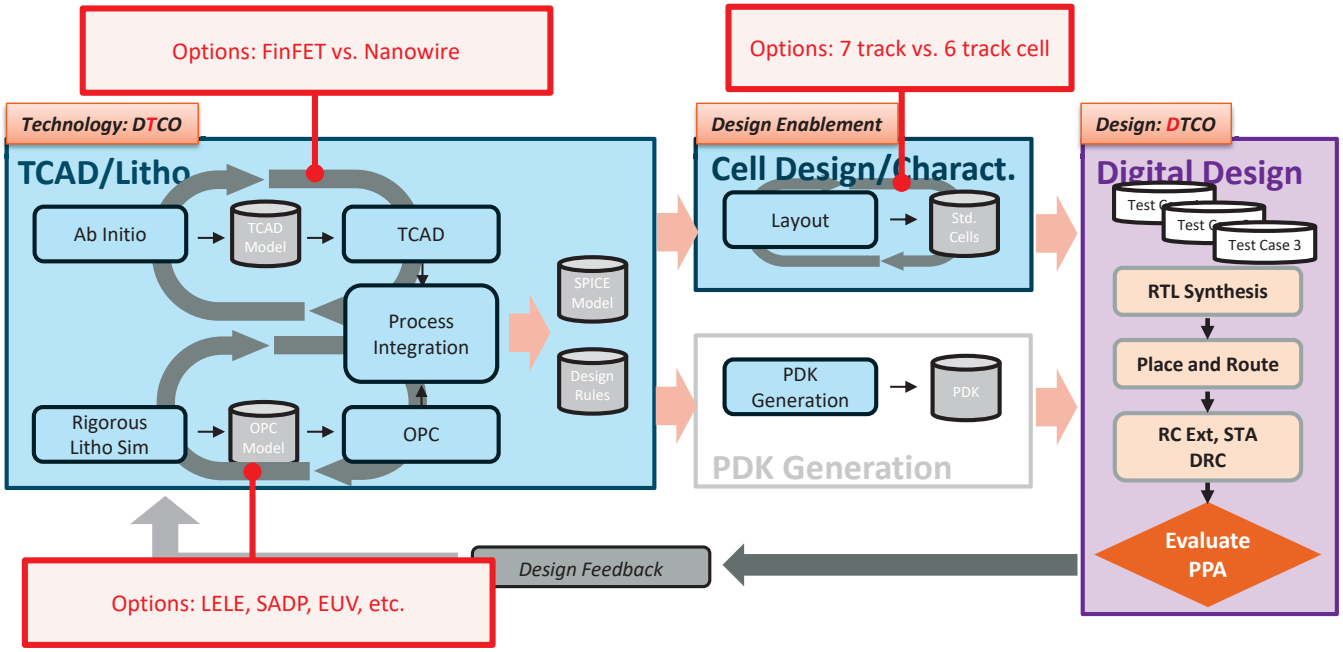
- Synopsys/GSS contributions are utilizing inputs from many WPs and partners.
- Tools and methodologies developed as part of WP3 and 4
- Extensive R&D into toolchain and data integration carried out in WP5
- Inputs and integration with tools and flows from WP3



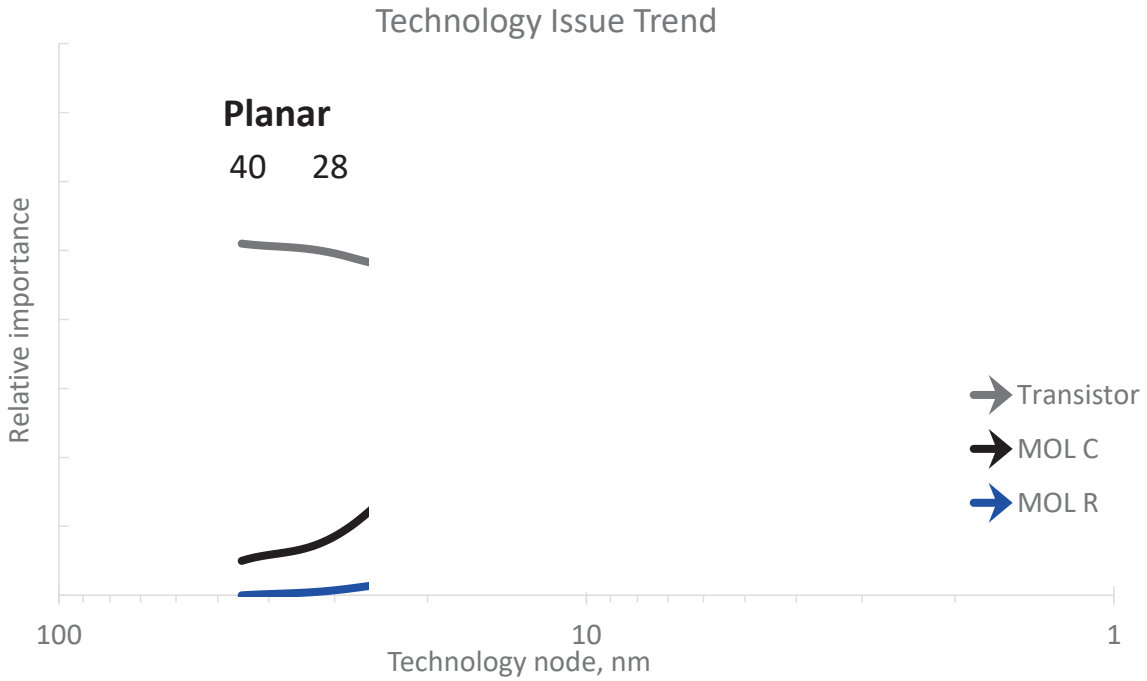
Introduction: The DTCO Concept

- What is Design Technology Co-Optimisation (DTCO) ?
  - A holistic approach to the development of technology and design in order to deliver an optimal product.
- DTCO is utilised in Foundries but it based on Silicon which limits turnaround and number of possible options
- Simulation based DTCO provides an efficient and rapid methodology for the estimation of PPA (Y)
  - Architecture choices
  - Process options
  - Performance booster assessment
  - Design rule optimisation
  - Assessment of the impact of process choices on PPA(Y)

Introduction: The DTCO Concept

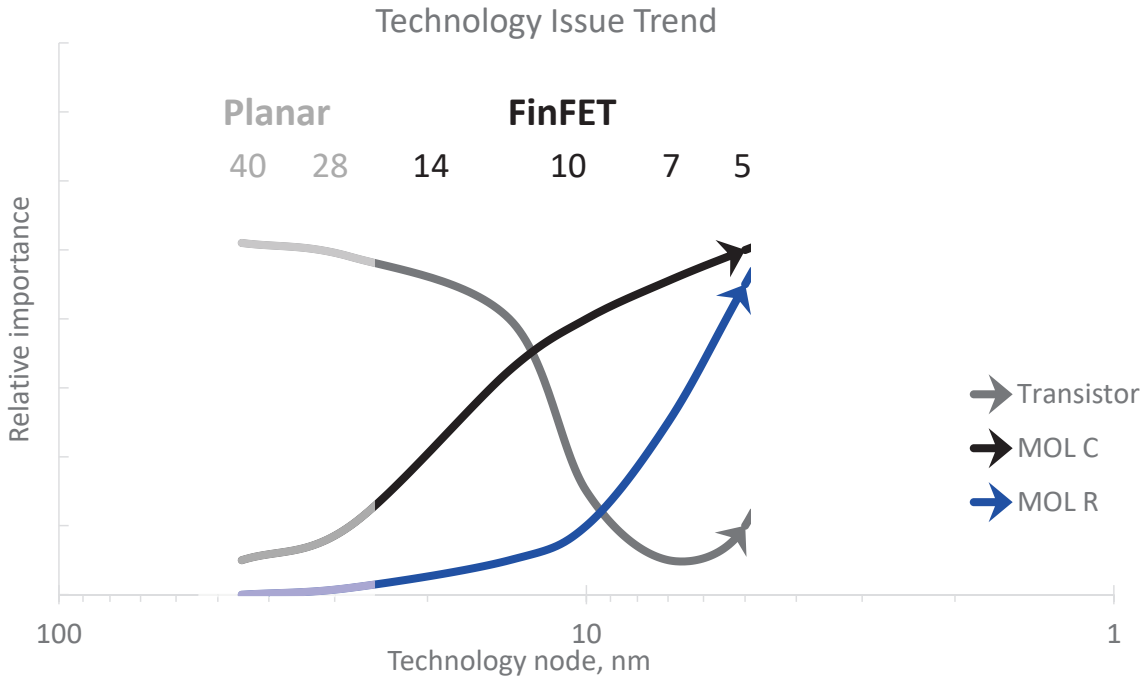


Major Technology Issues Addressed by DTCO



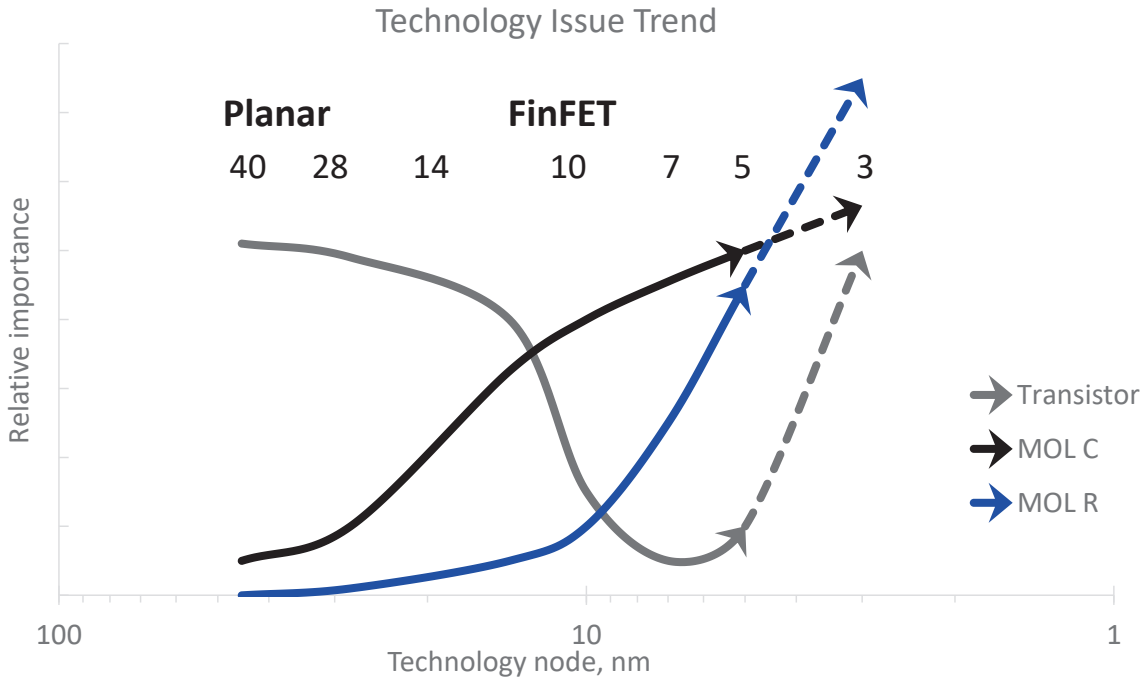
- For planar MOSFET, DTCO was mainly about transistor tuning

Major Technology Issues Addressed by DTCO



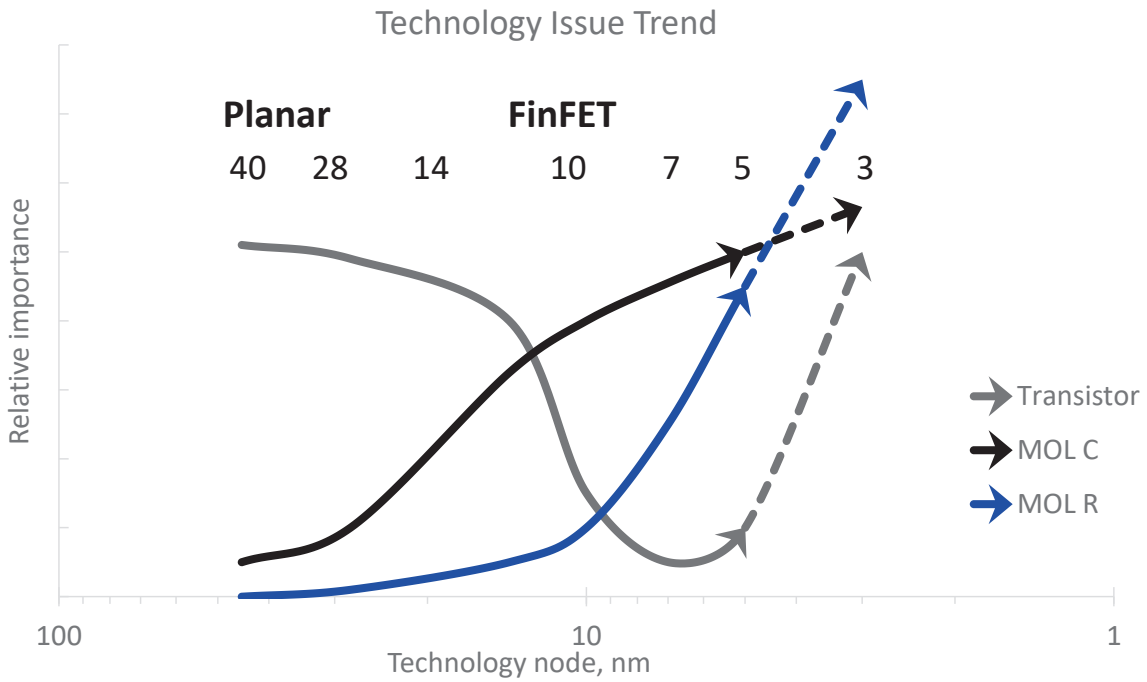
- For FinFETs, transistors became less of an issue
- MOL capacitance became a critical issue instead
- At 7nm, MOL resistance emerged as a critical issue and it keeps getting worse with scaling

Major Technology Issues Addressed by DTCO



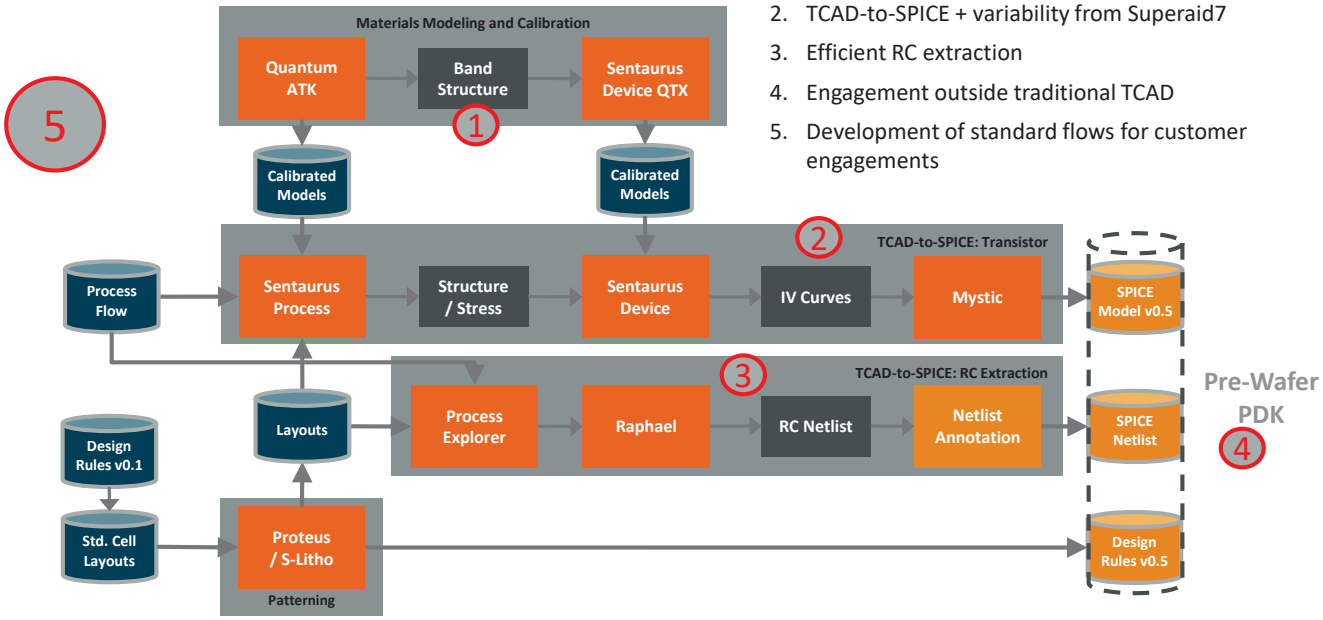
- The potential transition to nano-wires or nano-slabs brings back the focus on transistor
- PEX issues are only getting worse with scaling

Major Technology Issues Addressed by DTCO



- The potential transition to nano-wires or nano-slabs brings back the focus on transistors
- PEX issues are only getting worse with scaling: C and R
- **DTCO tool flows address all of these issues simultaneously!**

Example : Pre-Wafer DTCO *Flow*

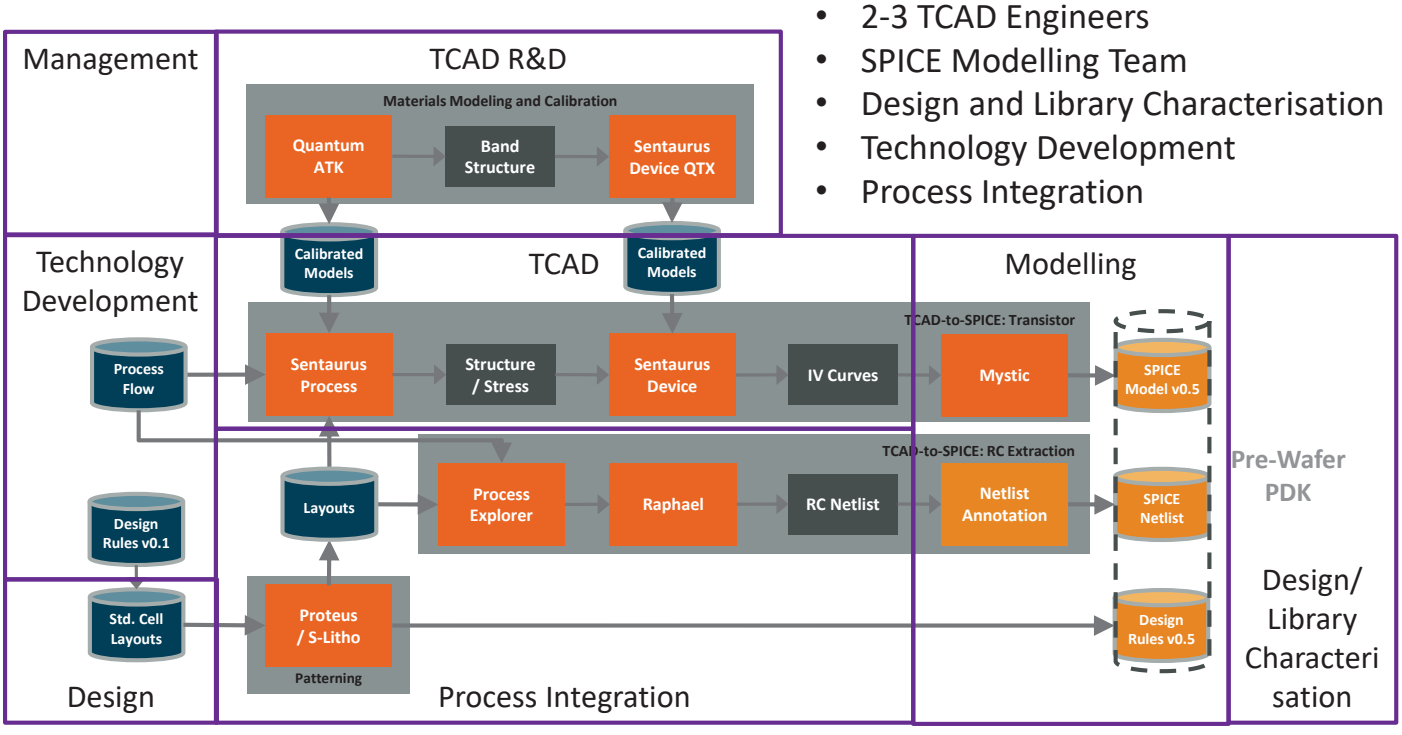


1. Materials Modelling and predictive simulation.
2. TCAD-to-SPICE + variability from Superaid7
3. Efficient RC extraction
4. Engagement outside traditional TCAD
5. Development of standard flows for customer engagements

Superaid7: DTCO Tool Flows

- DTCO tool flows are complex and non-linear
  - Requires interaction between expert users with domain specific knowledge
  - Require efficient information interchange
  - Need highly integrated and robust tools (WP4)
- Addressed in Superaid7 via
  - Development of integrated DCTO workflows in WP5
    - Toolchain integration via Enigma, SWB and Data management
  - Advanced spice modelling methodologies
    - Capturing process and statistical variability
  - Significant automation
    - Device simulator autocalibration
    - RC extraction

Example : Pre-Wafer DTCO *Flow*



- 2-3 TCAD Engineers
- SPICE Modelling Team
- Design and Library Characterisation
- Technology Development
- Process Integration

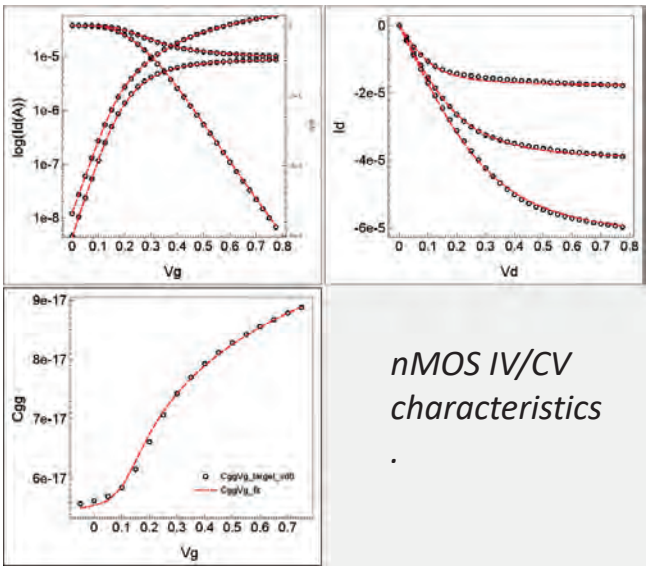
FinFET DTCO Example

Aims

- Provide a SPICE model with variability capabilities
- TCAD as the primary (only) calibration data provider
- Enable users to perform
  - Quick PPA analysis
  - Process optimisation
  - Process corner analysis

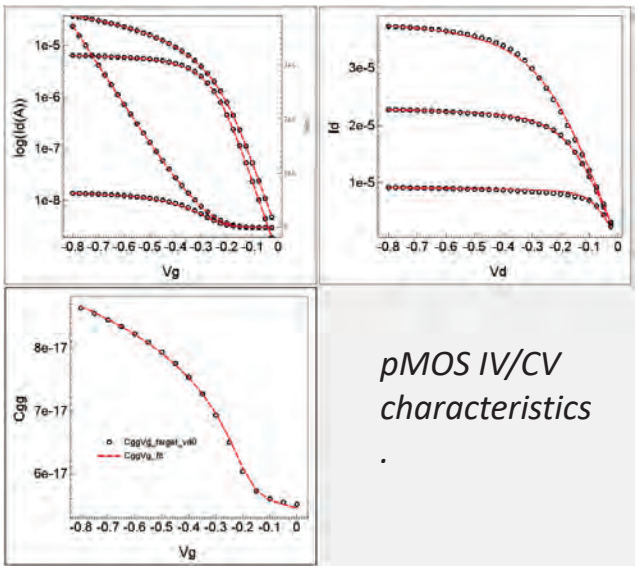
Base model extraction - Mystic

Automated spice model extraction methodologies and software. (WP4)



nMOS IV/CV characteristics

.



pMOS IV/CV characteristics

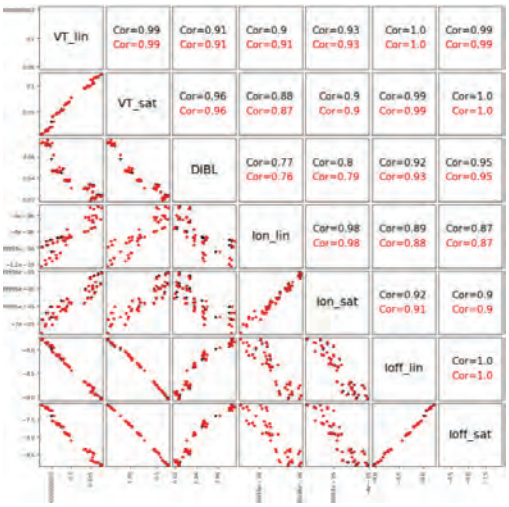
.

Base model extraction - Mystic

- Script based Mystic extraction.
- Targeting robustness and re-usability.
- Linked to TCAD
  - Sprocess and Sdevice via SWB and Enigma
- 14nm FinFET example:
  - ***86 TCAD splits*** and ***5 process variations*** modelled.
  - Single extraction strategy.

Parameter	Nominal	Range	Comment
L	25	+/- 2nm	Gate length variation
H	40	+/-2nm	Gate height
W	8	+/-2nm	Fin thickness
A_fin	88	+/-1	Fin angle factor
T_spacer	8	+/-2nm	Spacer thickness

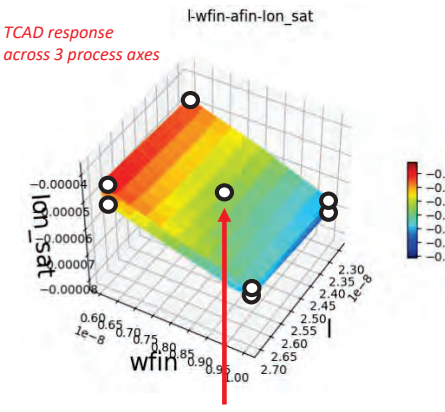
nMOS fitting across the DoE:



Process variation modelling

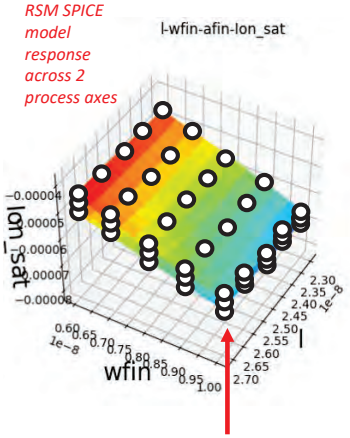
- TCAD to SPICE approach w/RandomSpice allows users to generate a response-surface model to handle arbitrary process variations
  - Spice modelling methodology developed as part of WP5

TCAD response across 3 process axes



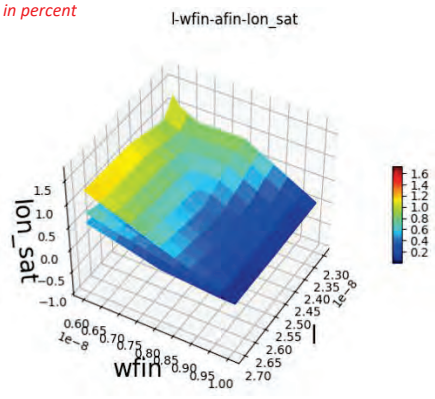
*TCAD simulation points: 5 axis optimal grid = **43 TCAD simulations***

RSM SPICE model response across 2 process axes



*SPICE model simulation points 5 axis full grid = 5^5 = **3125 SPICE simulations***

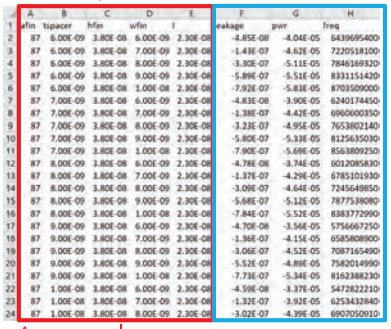
Relative error in percent



Process variation modelling

- Allows users to evaluate circuit behaviour across a wide range of process splits (as well as interpolating between TCAD simulation points

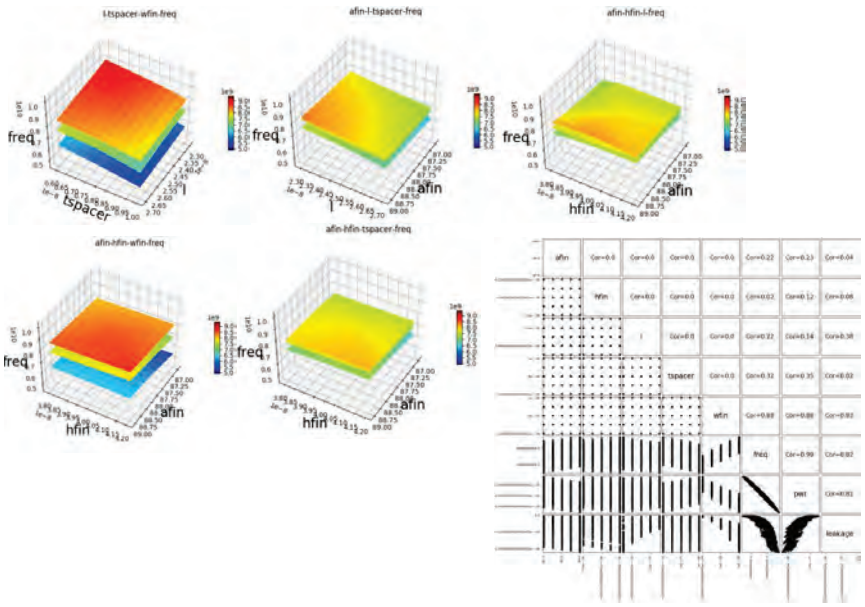
Raw data outputs:



Axes

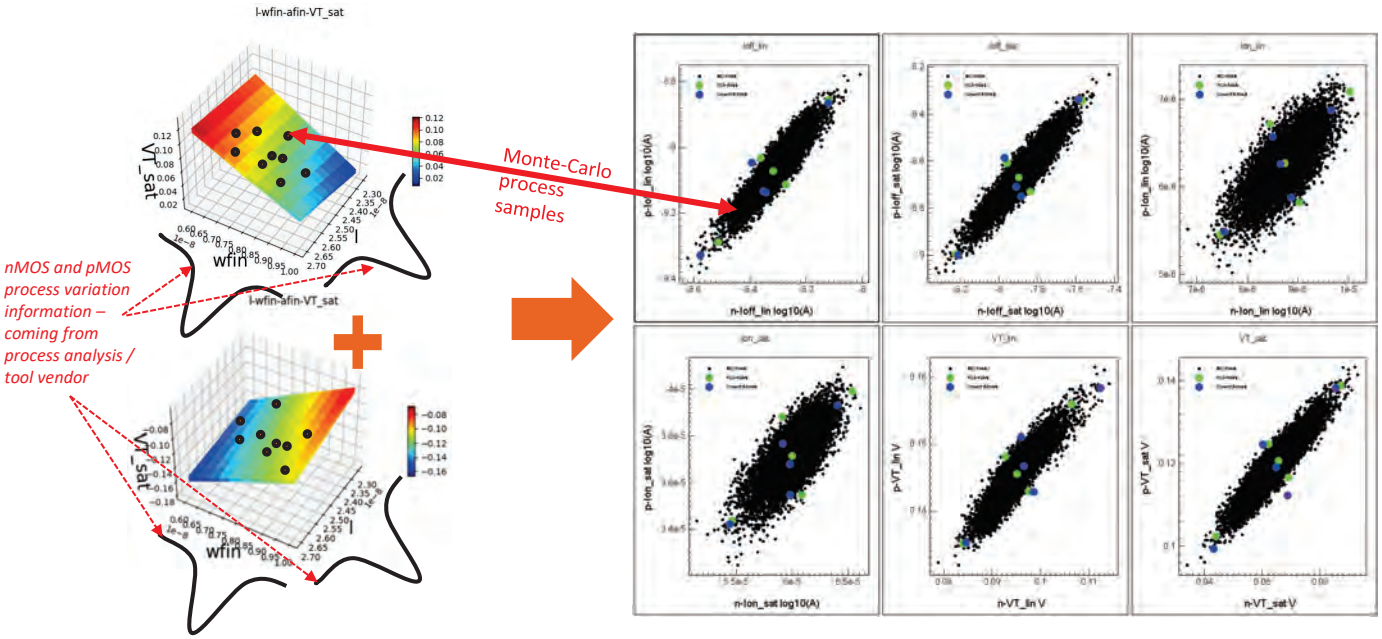
RO response

3125 SPICE simulations



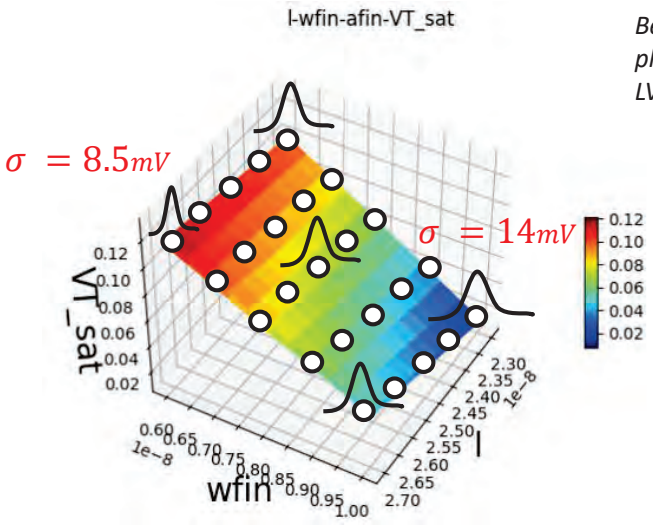
Process corners

- Introduce Monte-Carlo process variation via RSM SPICE model.
  - Apply distributions to DoE axes
- Extract process corners based on expected variations.



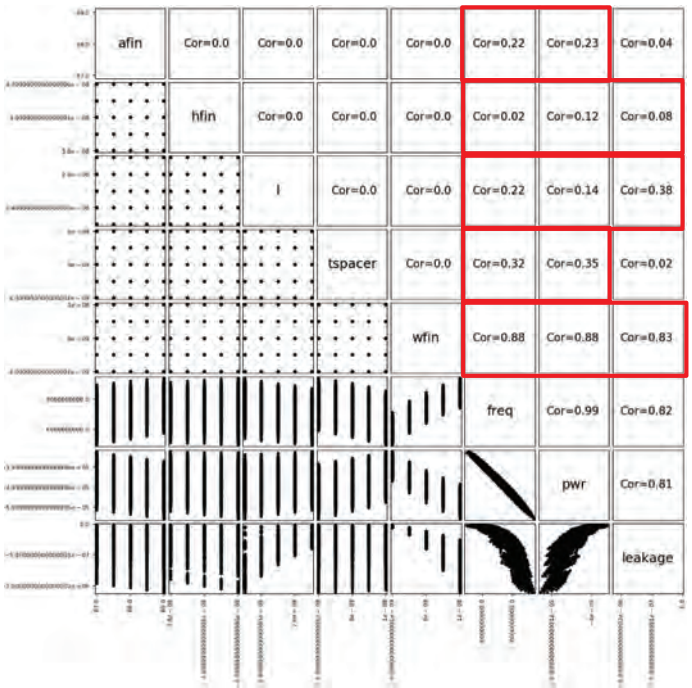
Local variation (LV) modelling

- Local variation simulations are performed across the DoE and added to the RSM using Garand (WP4)



Because LV data is underpinned by physical TCAD simulation we capture LV changes across the PV space.

RO Response Analysis



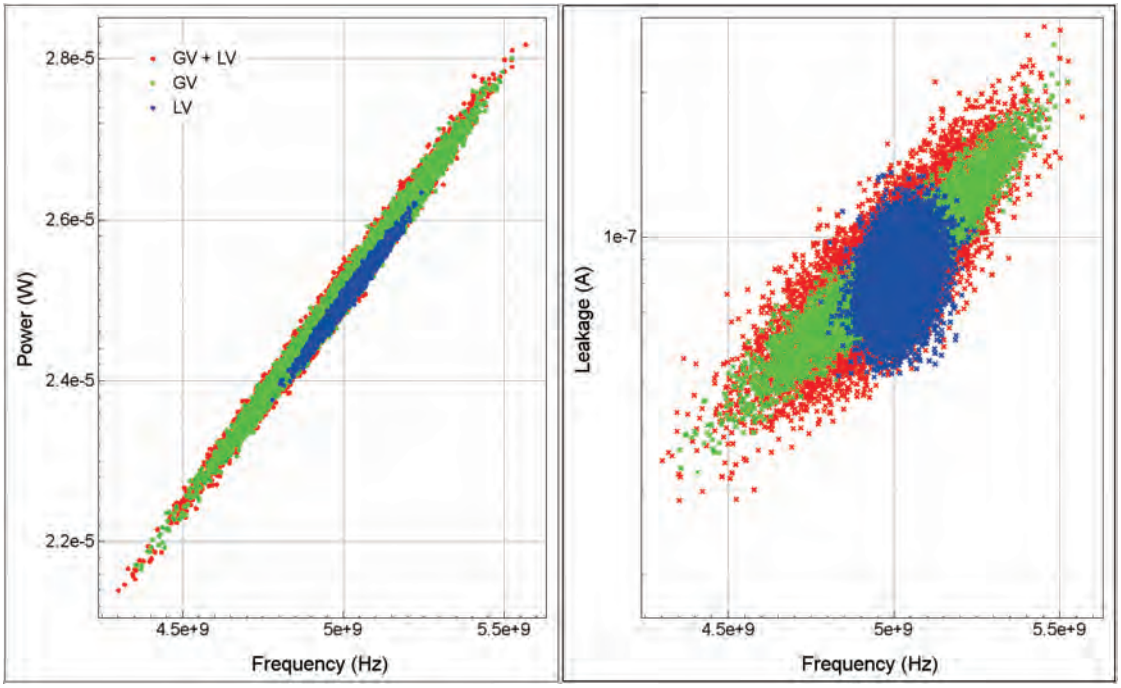
	Frequency	Power	Leakage
Afin	Small	Small	None
Hfin	None	None	None
Lg	Small	None	Medium
Tspacer	Medium	Medium	None
Wfin	High	High	High

Wfin dominates impact on RO response

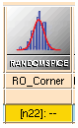
RO Monte-Carlo response – Nfin =1

Individual and combined variability simulation results for nominal design point.

Analysis with Nfin=1



RO Corner analysis



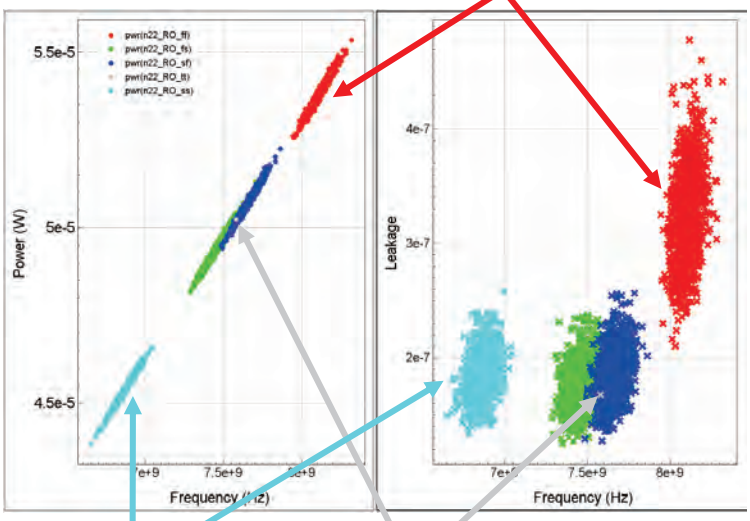
Analysis run at Nfin=2

From GV: FF to SS corner spread:
~ 1.6GHz

From GV+LV: FF to SS corner spread:
~ 1.6GHz

As previously seen, the global variation dominates the RO response

FF process corner with local variability enabled



SS process corner with local variability enabled

Nominal device point

Conclusions and Outlook

- Technology scaling is presenting increasing challenges
  - The relative impact of various factors is changing rapidly
  - DTCO is helping to address these challenges
- DTCO flows are, by nature, complex and require tightly integrated working practices and toolchains that support this.
- Developments during Superaid7 are helping to make true DTCO a reality
  - Project outputs are already part of commercialized software and flows

3D Devices: Experiment & Simulation

S. BARRAUD, CEA, LETI, Minatec Campus, Grenoble, FRANCE

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

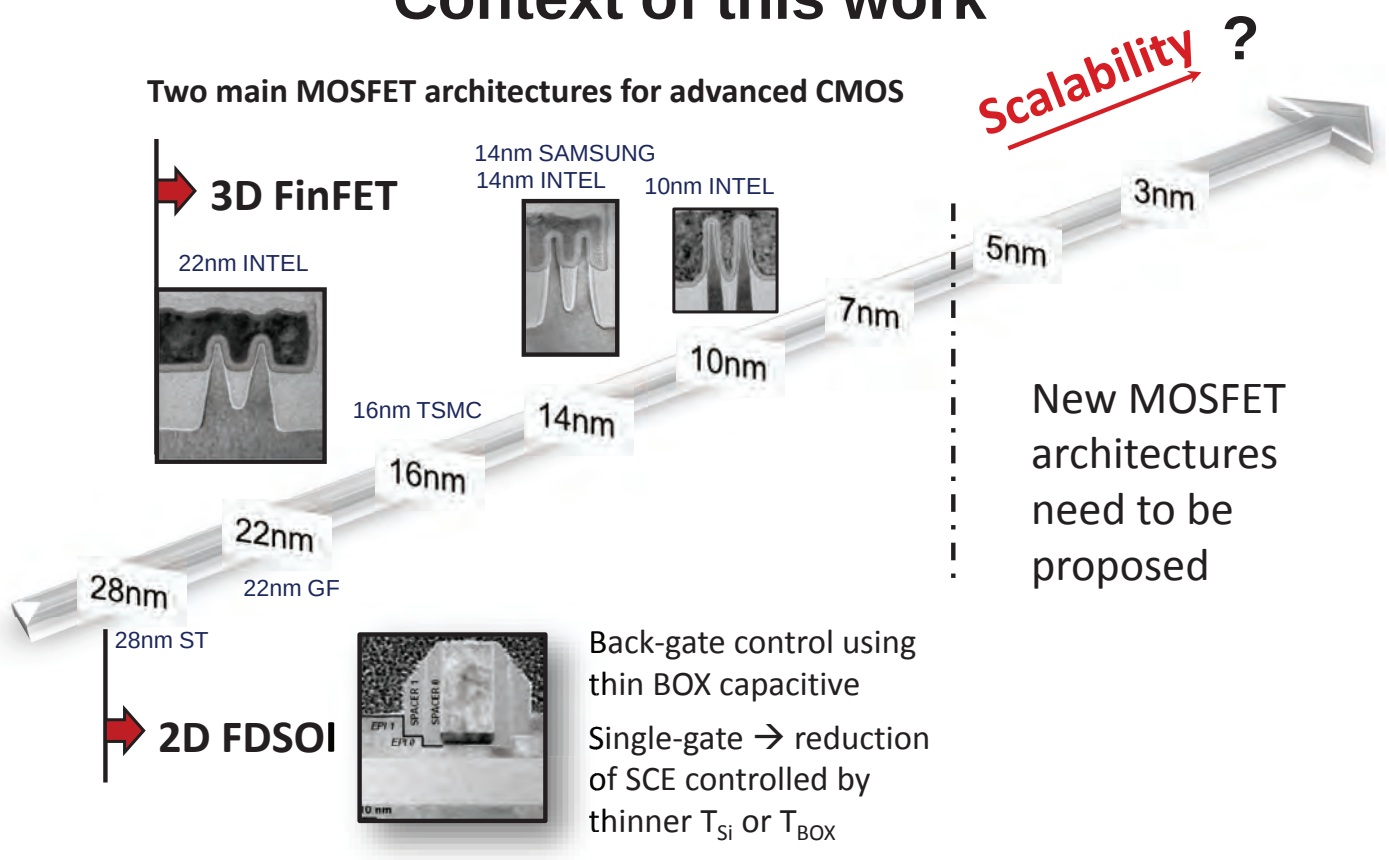
September 3, 2018, Dresden, Germany

Outline

- Introduction and Motivation
- Performance and Design Consideration
- 3D Process Integration for Stacked-Wires FETs
- Electrical Characterization
- Conclusions and Outlook

Context of this work

Two main MOSFET architectures for advanced CMOS



Context of this work

Recent press release

May | 2017

Samsung set to lead the future of foundry with comprehensive process roadmap down to 4nm

4LPP (4nm Low Power Plus): 4LPP will be the first implementation of **next generation device** architecture – MBCFET™ structure (Multi Bridge Channel FET). MBCFET™ is Samsung's unique GAAFET (**Gate All Around FET**) technology that uses a **Nanosheet device** to overcome the physical scaling and performance limitations of the FinFET architecture.

https://news.samsung.com/global/samsung-set-to-lead-the-future-of-foundry-with-comprehensive-process-roadmap-down-to-4nm

June | 2017

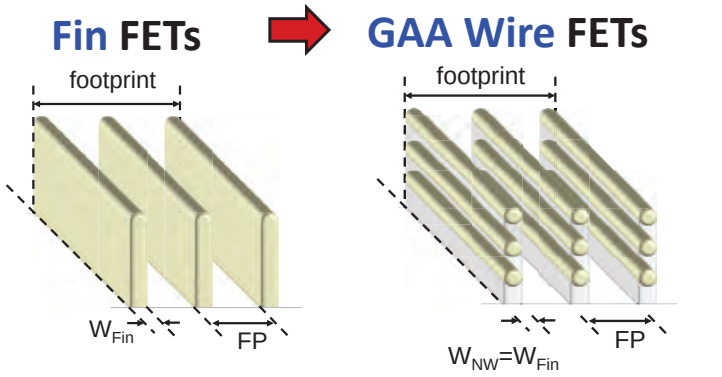
IBM claims 5nm Nanosheet breakthough

IBM researchers and their partners have developed a new transistor architecture based **on Stacked Silicon Nanosheets** that they believe will make FinFETs obsolete at the 5nm node

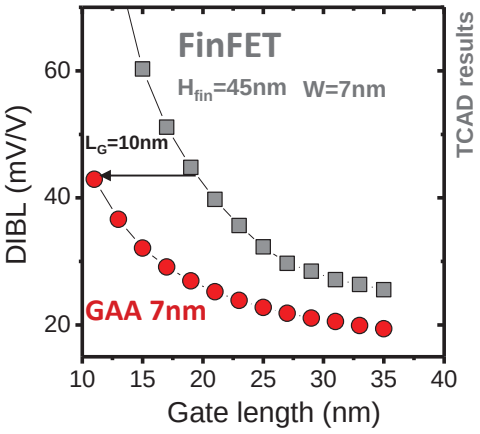
http://www.eetimes.com/document.asp?doc_id=1331850&

GAA MOSFET devices are becoming an industrial reality

Motivation

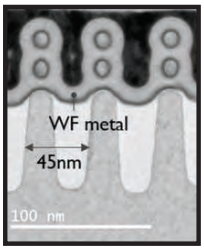


- Wire FETs can be view as an evolutionary step from the FinFET
- Wire FETs share many of the same process steps as the FinFET
- GAA FETs provides a better electrostatics than FinFET

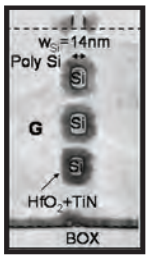


14nm INTEL [1]

IMEC [2]



LETI [3]



[1] S. Natarajan et *al.*, IEDM, 2014.
[2] H. Mertens et *al.*, VLSI Technology, 2016.
[3] C. Dupré et *al.*, IEDM, 2008.

Introduction – Goals and Strategy

Main Objective of SUPERAID7

Simulation of the impact of systematic and statistical process variations on devices, interconnects and circuits down to the 5nm node

WP1 Project managment

WP2: Specifications and benchmarks

Define specifications for two generations of devices (**7nm Trigate and 5nm GAA Stacked-Wires FETs**) – process-flow/morphological data/electrical data…

→ **to provide input data for the calibration/validation of simulation tools**
→ **to give a feedback to other WP after the comparison between simulation and experiment**

WP3: Variation-aware equipment and **process simulation**

WP4: Variation-aware **device and interconnect simulation**

WP5: Software integration and **compact models**

Dissemination (WP6) and exploitation (WP7)

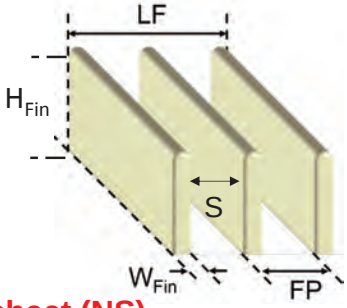
Outline

- Introduction and Motivation
- Performance and Design Consideration
- 3D Process Integration for Stacked-Wires FETs
- Electrical Characterization
- Conclusions and Outlook

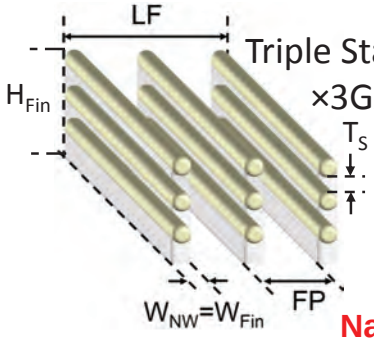
Performance and Design Consideration

FinFET (FF)

FF
FP=25nm
H_{Fin}=43nm
W_{Fin}=7nm



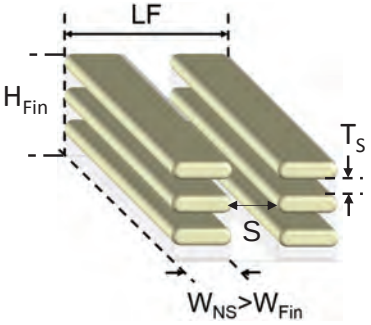
Nanowire (NW)



Triple Stack (3S) ×3GAA

NW
FP=25nm
H_{Fin}=43nm
T_S=8nm
H_{NW}=6.3nm
W_{NW}=7nm

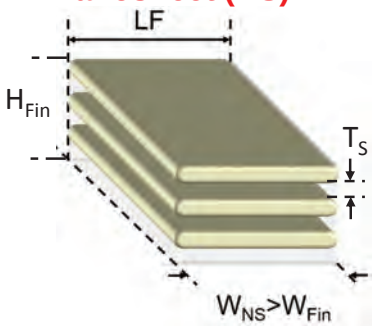
Nanosheet (NS)



NS
H_{Fin}=43nm
H_{NS}=6.3nm
W_{NS}>W_{NW}
T_S=8nm

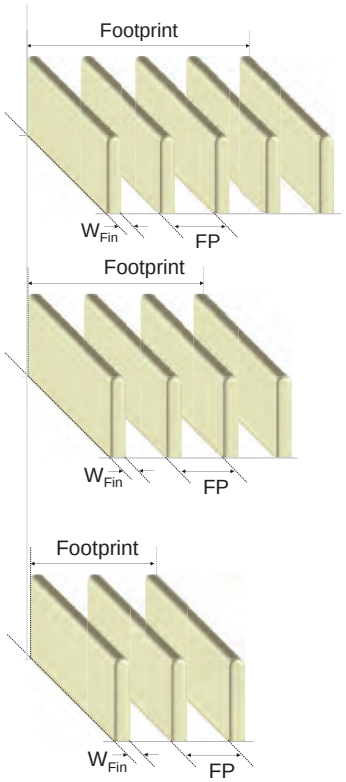
Double Stack (1S) ×3GAA

Nanosheet (NS)

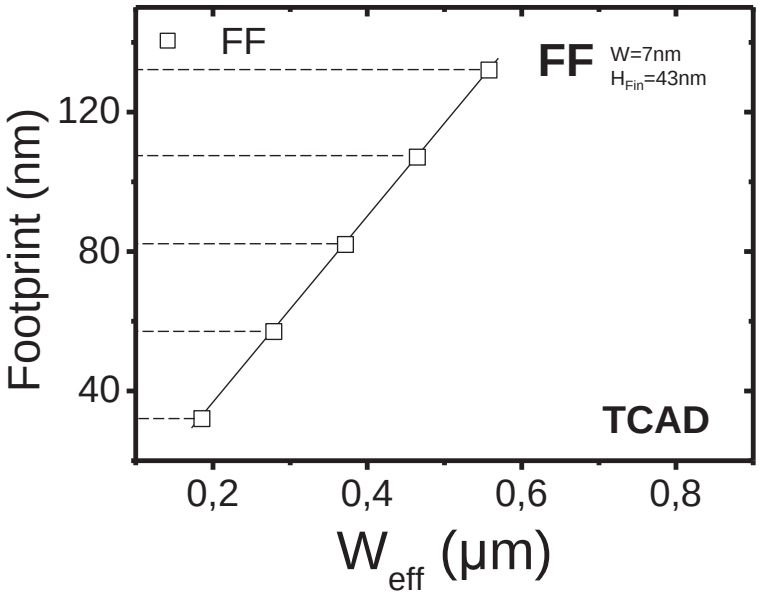


Single Stack (2S) ×3GAA

Effective width of FinFET

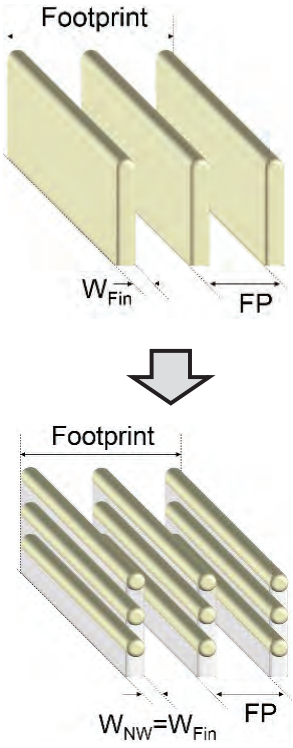


$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

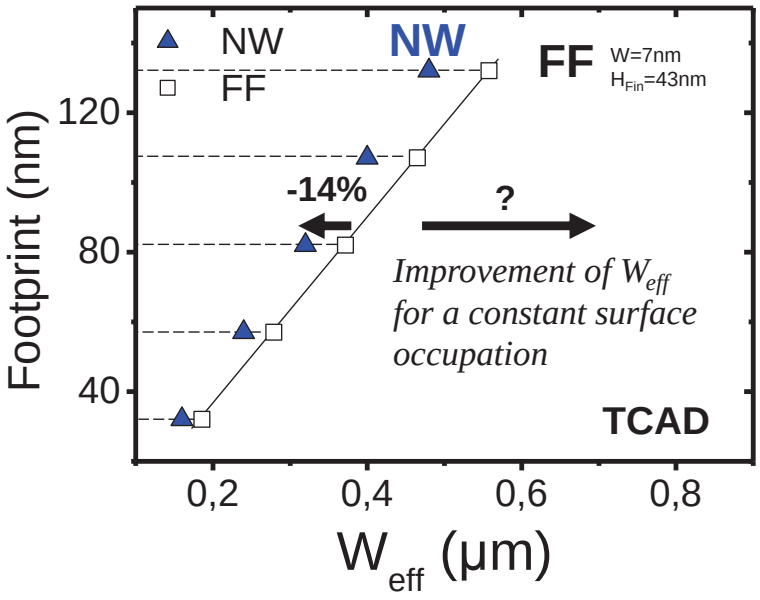


S. Barraud et al., IEDM 2017

FinFET versus GAA Nanowires



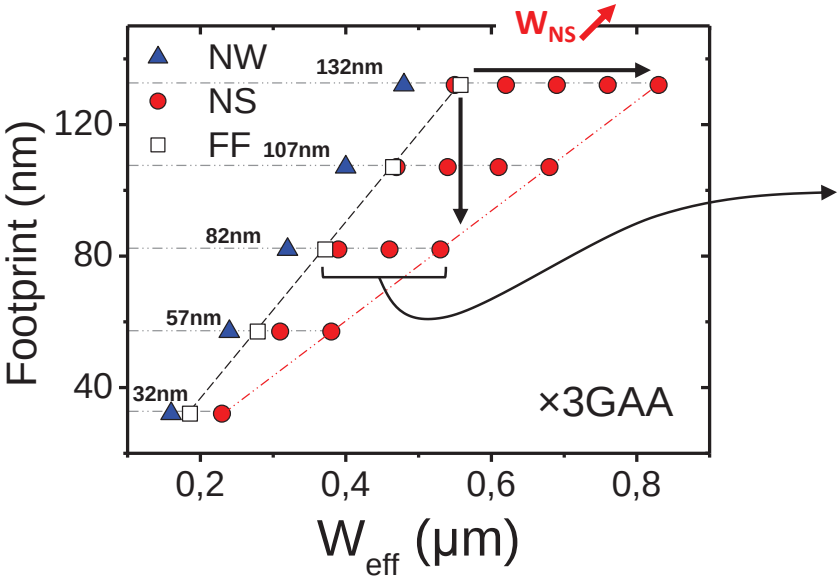
$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

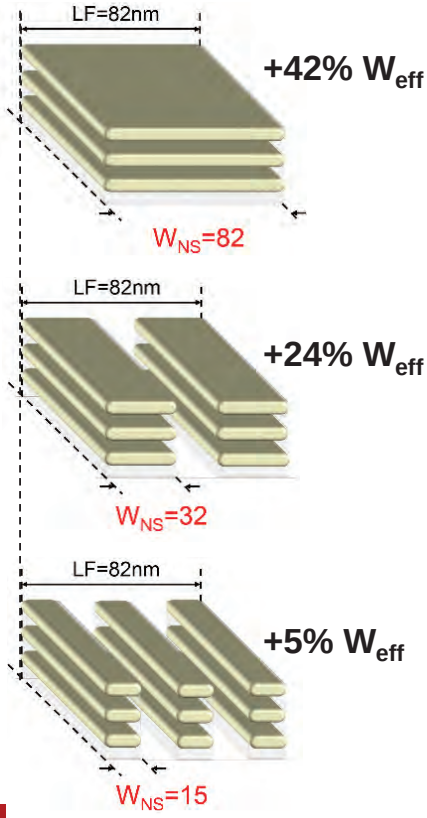


S. Barraud et al., IEDM 2017

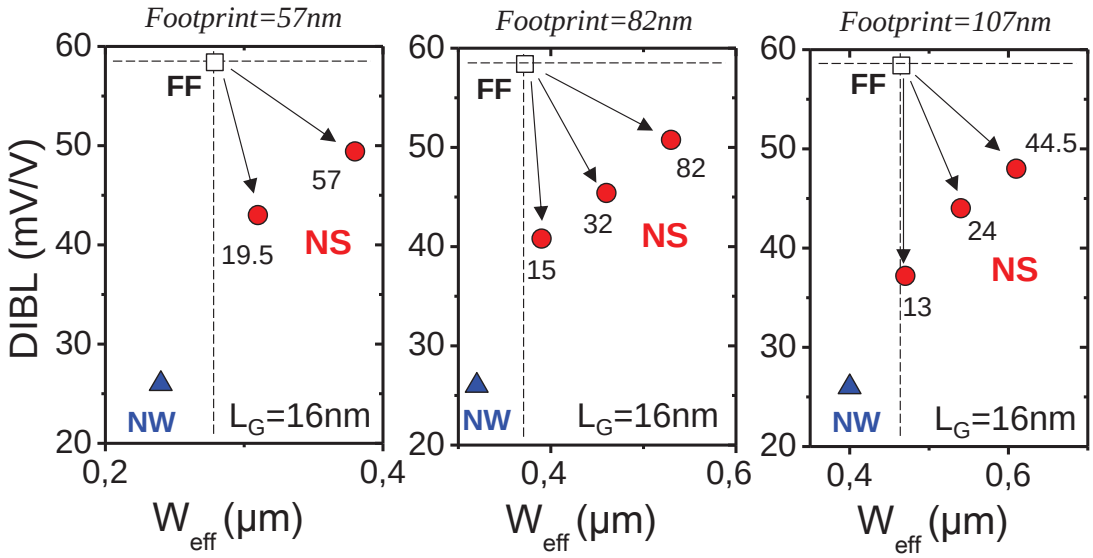
GAA Nanowires versus GAA Nanosheets

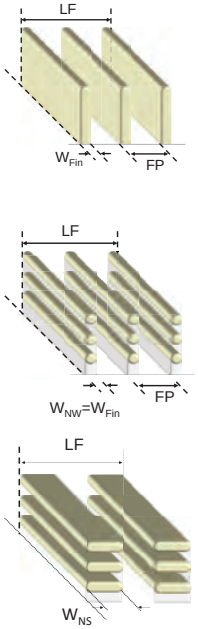
$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$





Tradeoff between SCE and W_{eff}

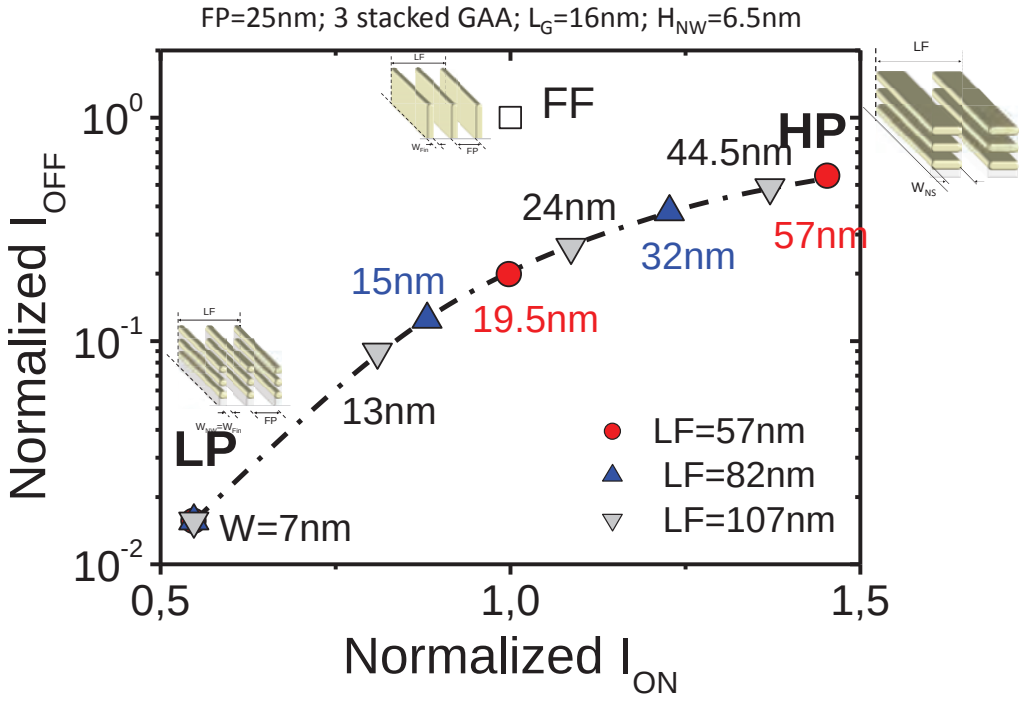




GAA stacked-nanosheets maximize W_{eff} (*i.e.* drive current) per layout footprint with improved channel electrostatics.

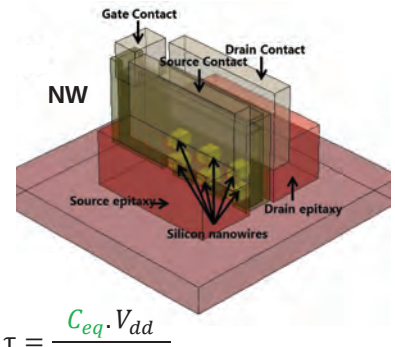
S. Barraud et al., IEDM 2017

Power/Performance Optimization



Parasitic capacitances and delay

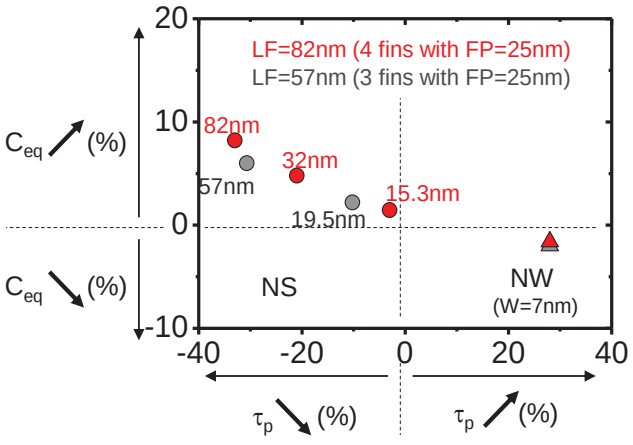
A delay reduction of around 20% is expected for W_{NS}~30nm



$$\tau = \frac{C_{eq}.V_{dd}}{N_{stack}.I_{eff}}$$

$$C_{eq} \approx (\mathrm{M} + 2.\mathrm{FO}).C_{gd0} + {}^{3}/_{4}.\frac{\varepsilon_{SiO_2}.L_g.w_{eff}}{t_{inv}}.\mathrm{FO} + \frac{C_{back-end}}{2}$$

τ: Delay
I_{eff}: Effective drive current
$I_{eff}=(I_H+I_L)/2$
$I_H=I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$
$I_L=I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD})$
Supply voltage V_{DD}=0.7V
FO=3
L_G=16nm
Spacer size: 4.2nm
EOT=0.67nm
$C_{back-end}$=2fF
M=2: Miller effect in inverter



What have we learned?

- GAA NS structures could be used to maximize the effective width which will improve the drive current without increasing power density (lower DIBL than in short-channel FinFET devices).
- A delay reduction of around 20% is expected for W_{NS}~30nm
- Nanosheet transistors offer more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width

Outline

- Introduction and Motivation
- Performance and Design Consideration
- 3D Process Integration for Stacked-Wires FETs
- Electrical Characterization
- Conclusions and Outlook

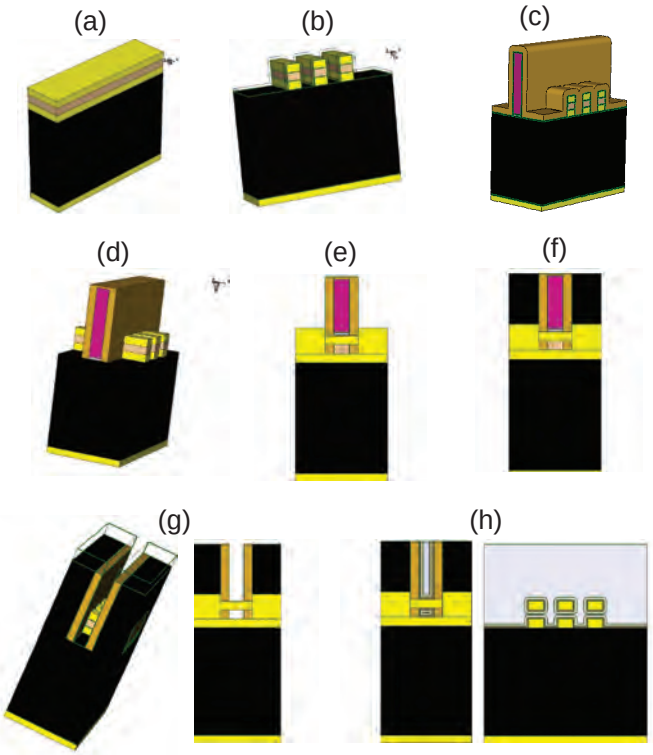
SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts" September 3, 2018, Dresden

Process Flow of GAA Stacked Wires FETs

RMG process
Self-Aligned Contacts (**SAC**)
SIT Fin patterning (FP=40nm)

- (a) SOI substrate
- (a) SiGe/Si epitaxy
- (b) Fin patterning (SIT process)
- Dumy gate deposition / CMP
- (c,d,e) Dummy gate patterning
- (c,d,e) Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- (f) ILD deposition / CMP
- (g) Dummy gate removal
- Release of Si NW (SiGe etching)
- Gate dielectric (HfO_2 2nm)
- (h) TiN deposition
- Fill metal (W) deposition / CMP
- Self-aligned contact (SAC) + M1 BEOL

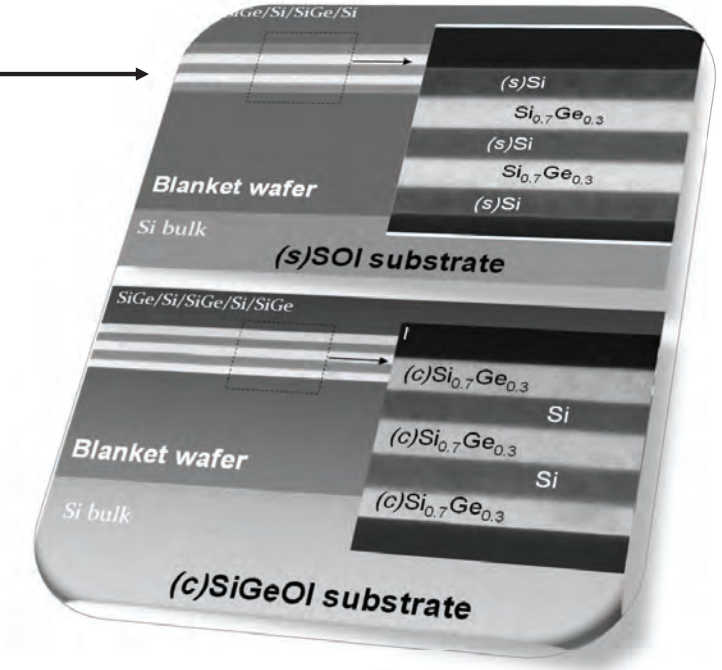
* Blue module: specific technical requirements for stacked wires FETs (as compared to FinFET devices)



Device Fabrication – (Si/SiGe) multilayer

Vertically Stacked GAA Si Nanosheet FET

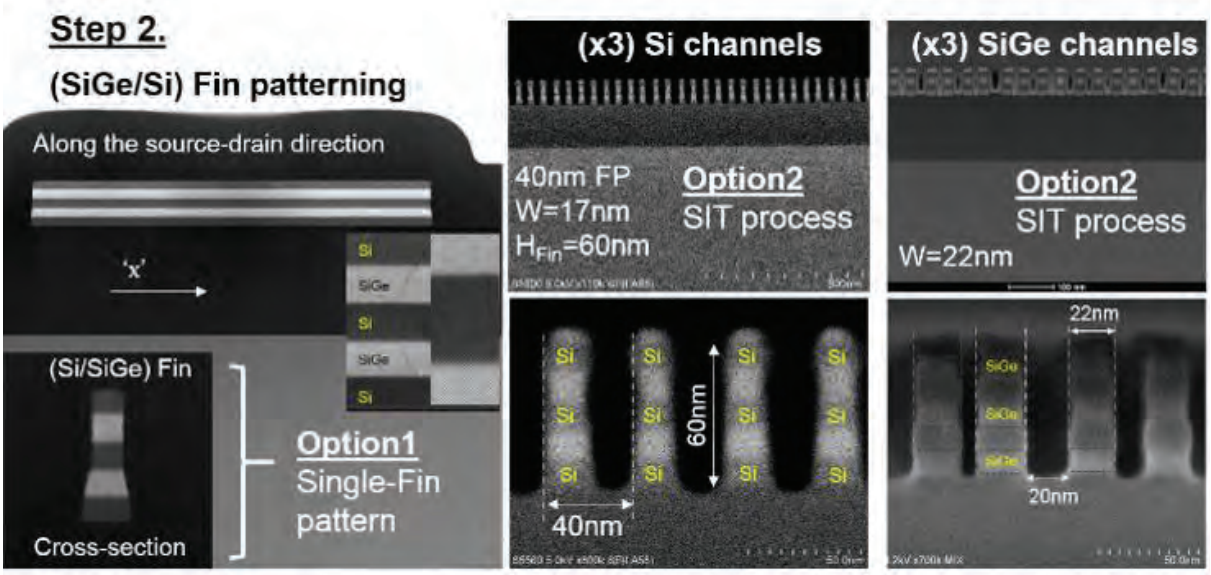
- SOI substrate
- SiGe/Si epitaxy
- Fin patterning (SIT process)
- Dumy gate deposition / CMP
- Dummy gate patterning
- Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- ILD deposition / CMP
- Dummy gate removal
- Release of Si NW (SiGe etching)
- Gate dielectric (HfO_2 2nm)
- TiN deposition
- Fill metal (W) deposition / CMP
- Self-aligned contact (SAC) + M1 BEOL



Epitaxial growth of ($Si_{0.7}Ge_{0.3}$/Si) multilayers

S. Barraud et al., IEDM 2016

Device Fabrication – Fin patterning



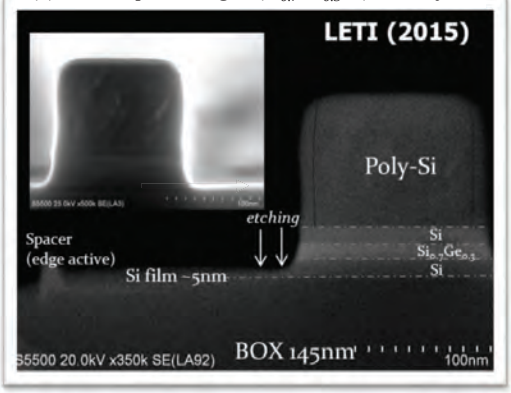
TEM images after etching of **(Si/SiGe) fins**. Two types of fins patterning were used: **(Left) single-Fin process and (Right) dense arrays of fins with a SIT process**s. Our SIT-based patterning technique yields **40 nm-pitch fins which are 60 nm high and 20 nm wide** for both Si and SiGe channels

Device Fabrication – Outer/Inner Spacer

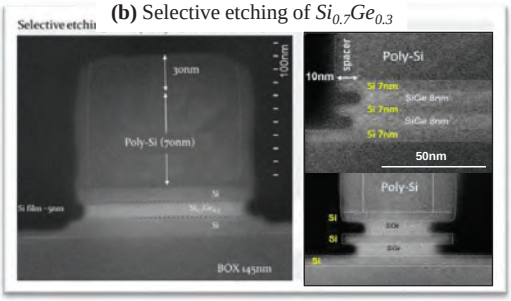
Vertically Stacked GAA Si Nanosheet FET

- SOI substrate
- SiGe/Si epitaxy
- Fin patterning (SIT process)
- Dumy gate deposition / CMP
- Dummy gate patterning
- Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- ILD deposition / CMP
- Dummy gate removal
- Release of Si NW (SiGe etching)
- Gate dielectric (HfO_2 2nm)
- TiN deposition
- Fill metal (W) deposition / CMP
- Self-aligned contact (SAC) + M1 BEOL

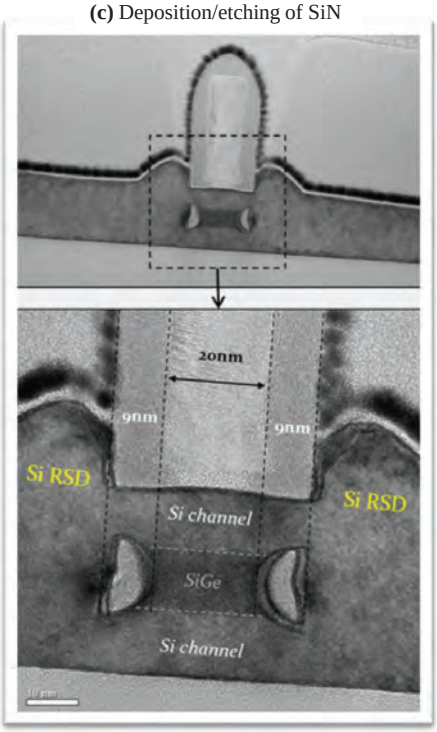
(a) Anisotropic etching of ($Si_{0.7}Ge_{0.3}$/Si) multilayers



(b) Selective etching of $Si_{0.7}Ge_{0.3}$



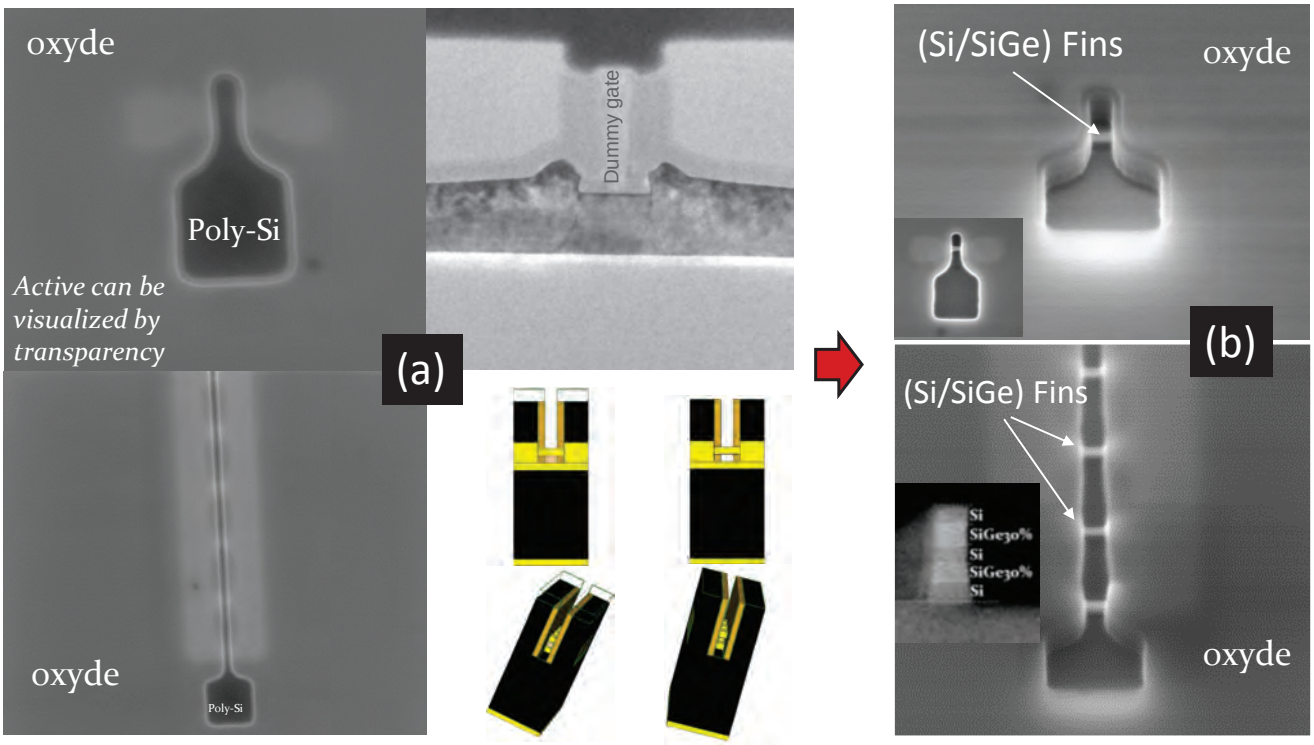
(c) Deposition/etching of SiN



Device Fabrication – RMG module

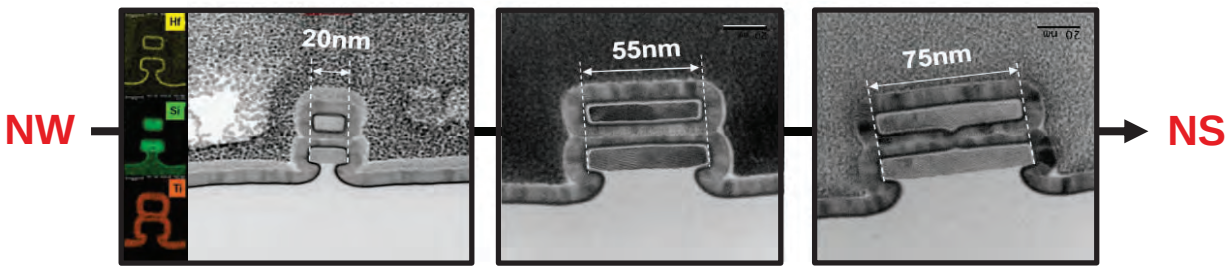
Hard mask removal

Dummy-Gate removal

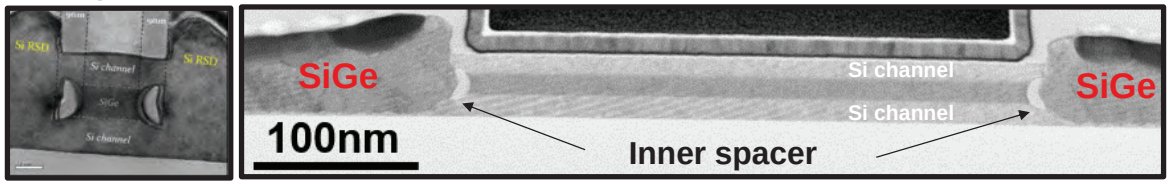


Vertically Stacked-Wires FETs

NW/NS Cross-section

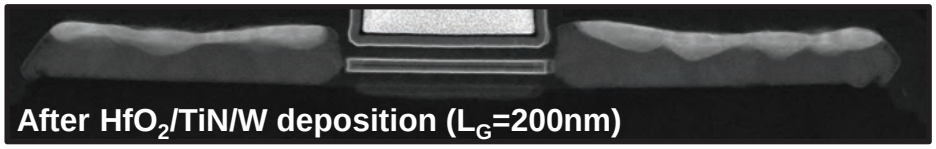


Along source-drain direction



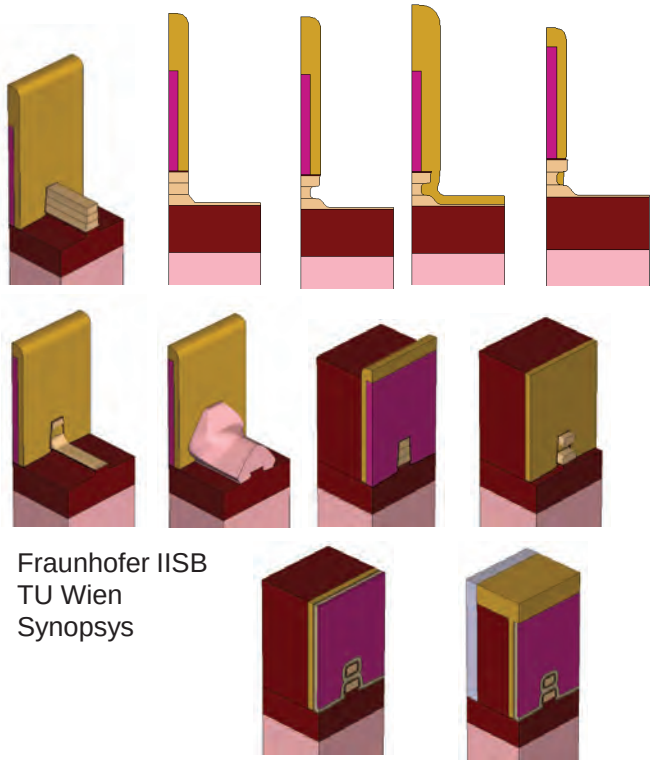
Short-L_G (20nm)

Long-L_G (>300nm)



S. Barraud et al., IEDM 2016

Simulation of Device Fabrication (WP3)



Fraunhofer IISB
TU Wien
Synopsys

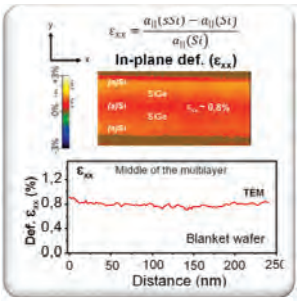
- SOI substrate
- SiGe/Si epitaxy
- Fin patterning (SIT process)
- Dumy gate deposition / CMP
- Dummy gate patterning
- Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- ILD deposition / CMP
- Dummy gate removal
- Release of Si NW (SiGe etching)
- Gate dielectric (HfO_2 2nm)
- TiN deposition
- Fill metal (W) deposition / CMP
- Self-aligned contact (SAC) + M1 BEOL

• LETI data (SEM, TEM, strain mapping, …) provided for the **calibration/validation of process simulation**
• **Identification of relevant process parameter for variability**
• **Influence** of process parameters **on electrical performance of 3D devices**

Strain Characterization

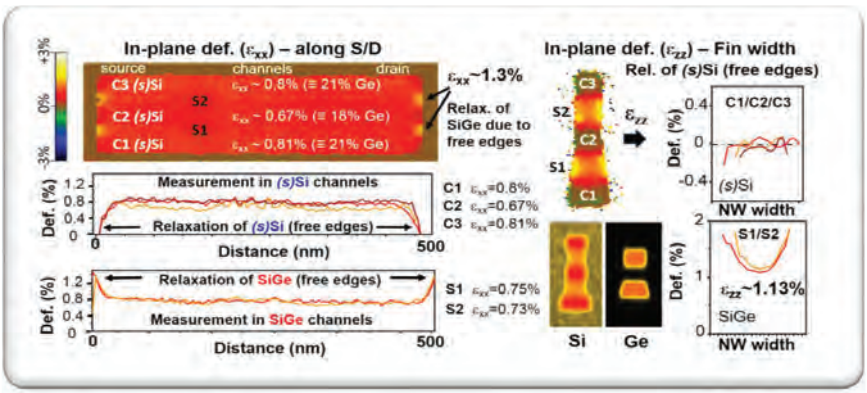
1. Superlattice (SiGe/Si)
2. Fin Patterning
3. Dummy Gate Deposition & RIE
   Spacer Deposition and RIE
   Inner spacer formation
   Source/Drain Epitaxy
   ILD & CMP
   Dummy Gate Removal
   Formation of Suspended NW (release of NW)
4. Gate Stack Formation
   Contact/BEOL

Is initial strain (substrate-induced strain) can be used to boost performances?



Strain engineering is another key factor for stacked-wires FETs.

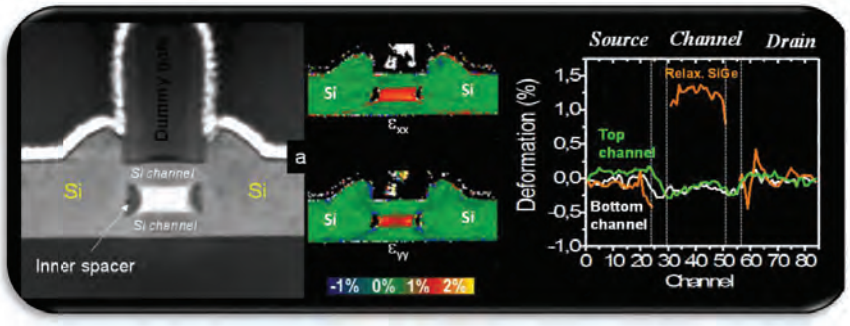
Strain maps were obtained by TEM using Precession Electron Diffraction technique*



* M.P. Vigouroux et *al.*, APL **105**, 191906 (2014)
* D. Cooper et *al.*, Nano Lett. **15**, 5289 (2015)

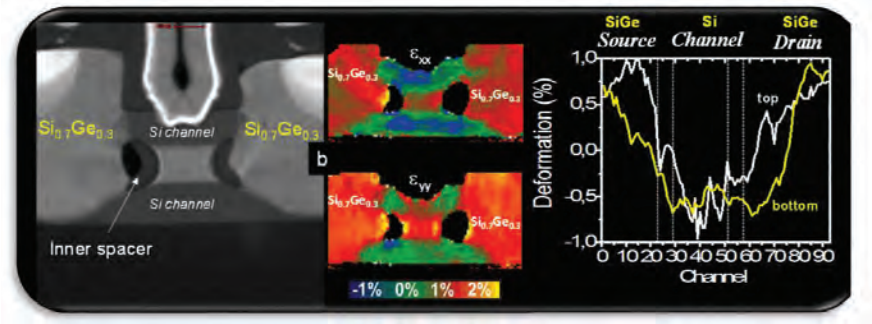
Strain Characterization

Deformation maps acquired by PED after Si Source/Drain



The silicon channels as well as the source and drain are unstrained → A deformation close to 0% is observed

Deformation maps acquired by PED after SiGe Source/Drain



Optimized engineering of process-induced stress techniques can be efficient in 3D stacked-NWs devices

S. Barraud et al., IEDM 2016

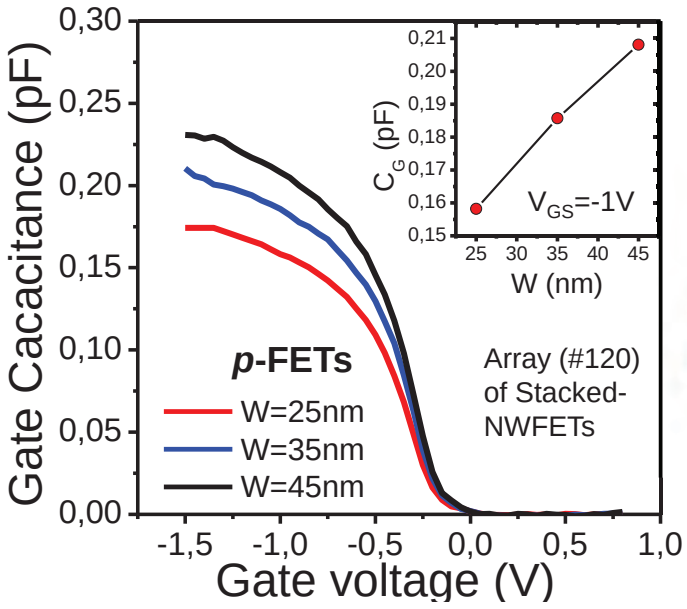
What have we learned?

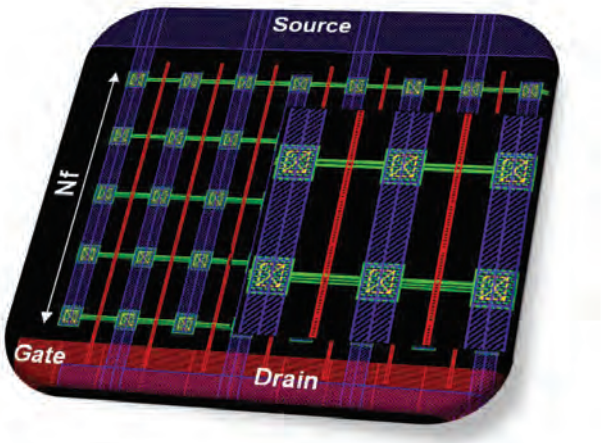
- Horizontal GAA NW and NS also have the advantage of being fabricated with minimal deviation from FinFET (FF) devices in contrast to vertical NWs which require more disruptive technological changes.
- The benefits of epitaxially regrown SiGe:B S/D junctions was evidenced, with a significant compressive strain (~1%) injected in top and bottom Si *p*-channels → need to be extrapolated at 5nm design rules.
- Process Simulation well reproduces morphological characterization → relevant process parameter can now be used for variability studies.

Outline

- Introduction and Motivation
- Performance and Design Consideration
- 3D Process Integration for Stacked-Wires FETs
- **Electrical Characterization**
- Conclusions and Outlook

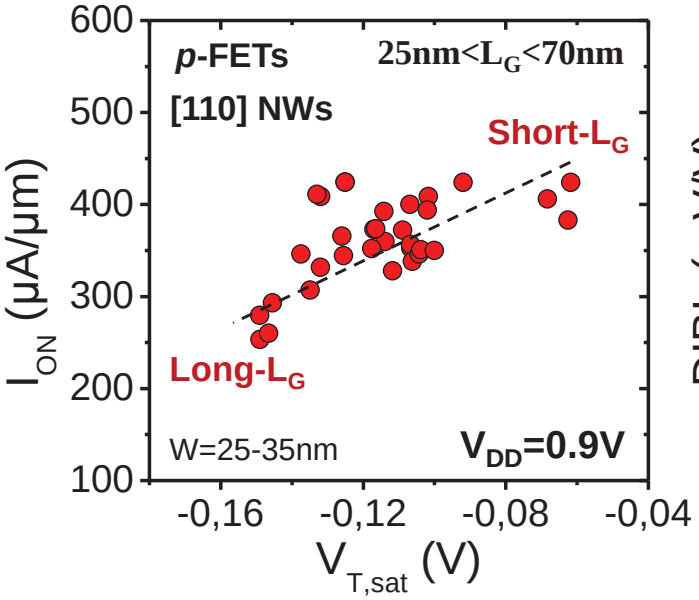
Electrical Characterization

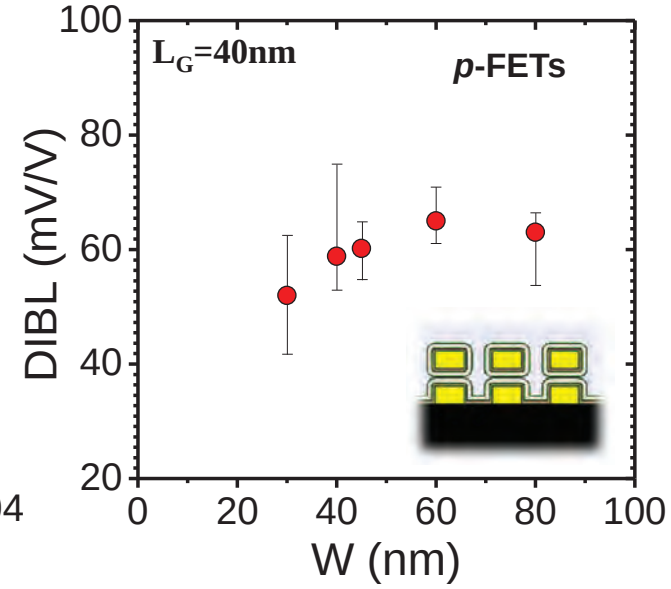




The CV curves, obtained from a multi-fingers gate and an array (#120) of stacked wires

Electrical Characterization

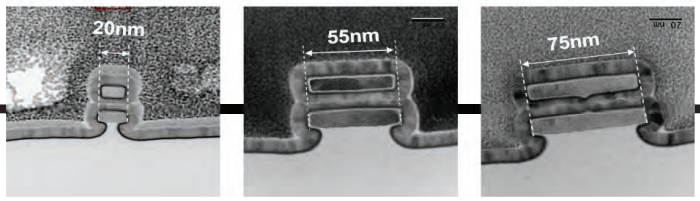




DIBL is constant above W=60nm

Electrical Characterization

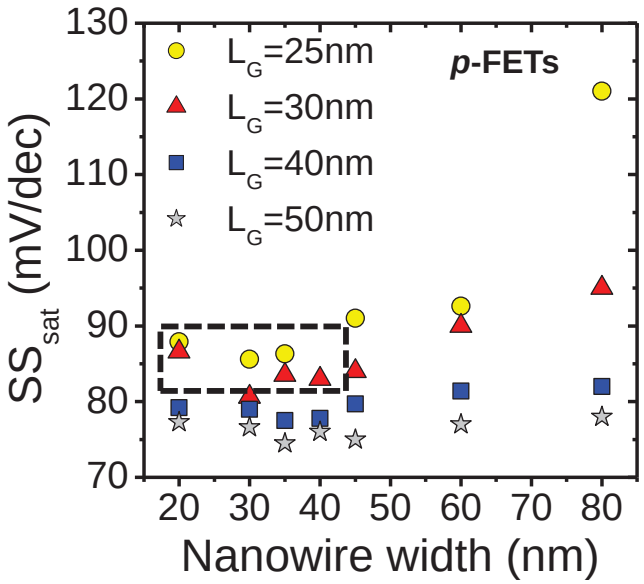
Stacked-NW



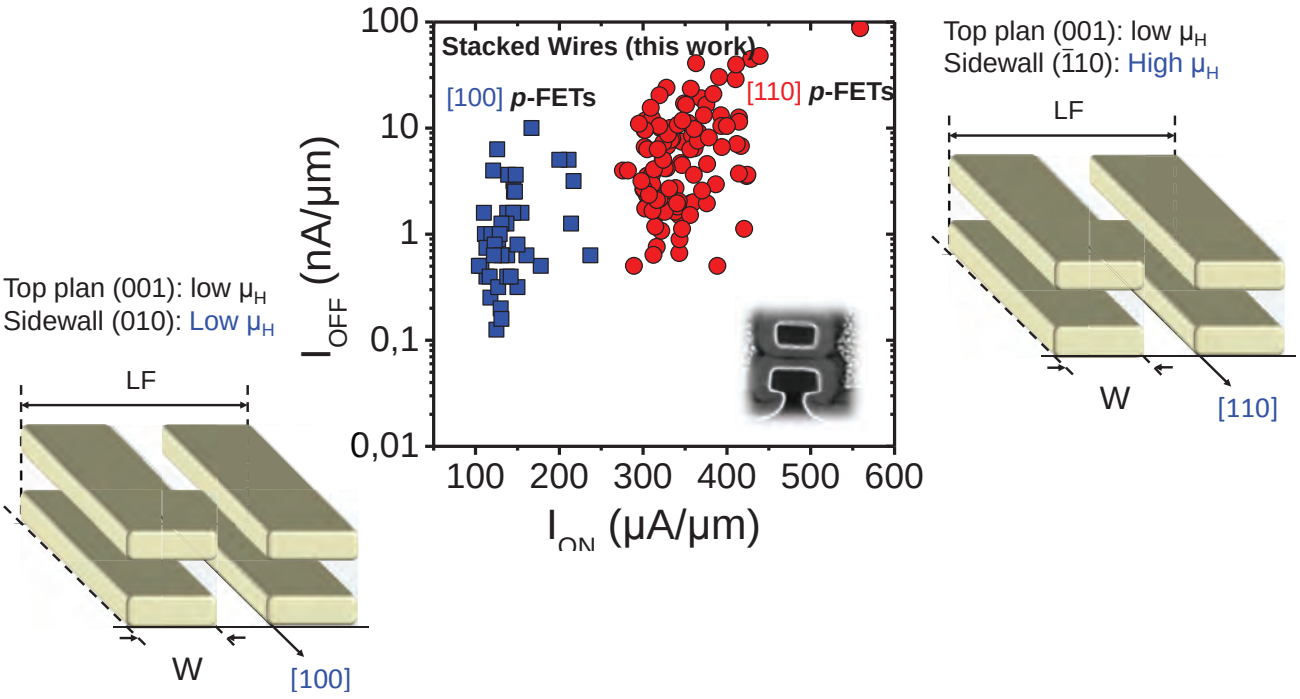
Stacked-NS

No increase of SS_{sat} up to 40nm

→ High W_{eff} can be used with a good electrostatics control



Electrical Characterization



Conclusions and Outlook

- Fabrication of vertically stacked Nanosheet MOSFETs (RMG process) are now demonstrated (inner spacers, SiGe:B S/D, 44/48nm CPP - IBM).
- Horizontal GAA Nanosheet also have the advantage of being fabricated with minimal deviation from FinFET (FF) devices in contrast to vertical NWs which require more disruptive technological changes.
- Strain characterization at different steps of fabrication (PED)
  Efficiency of process-induced strain (SiGe S/D) → significant compressive strain (~0.5 to 1%) in top and bottom Si *p*-channels.
- Design flexibility: Nanosheet transistors offer more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width.
- Morphological/Electrical data provided to partners for the calibration & the validation of advanced simulation tools.

Thank you!

Summary and Open Discussion

Jürgen Lorenz
Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie IISB, Erlangen, Germany

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

Summary

- The impact of various kinds of systematical and stochastic variations on sub-10nm devices and circuits is important and needs to be assessed and minimized
- A hierarchical simulation approach is necessary and presented in this workshop to deal with the impact of variations, ranging from equipment simulation to statistical device simulation and compact model extraction
- Accurate and efficient process and device models are needed for variability studies
- The most relevant sources of variations must be identified and used in a DoE to minimize the complexity of simulation

Summary (II)

- Systematic variations may influence several quantities in parallel, and partly cause correlations between these quantities. Such correlations must be considered in circuit simulation
- The importance of process variations and of the simulation and minimization of their impact will be further growing
- The approach presented in this workshop needs to be customized to the industrial process flow in question, especially regarding the large variety of systematic process variations which depend on details of the technology used.

Acknowledgements

- Contribution of all colleagues at partners highly appreciated
- Valuable inputs from EC review team and from SUPERAID7 ISAB
- Funding from EC highly appreciated

The research leading to these results has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688101 SUPERAID7.

THANK YOU FOR YOUR ATTENTION!