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SUPERAID7

Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

D5.5: Demonstration of correlation-aware simulation of impacts of statistical and systematic variability

(Synopsys)

Confidentiality level: Public

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1 Abstract

Within this public deliverable, the overall concept for process variability-aware compact models, developed and implemented in the SUPERAID7 project, is described. To this end, innovative concepts were needed, addressing all levels of the hierarchical simulation approach spanning from equipment to circuit simulation. This deliverable focuses on the link between

- systematic process variations which must be traced via process simulation,
- the simulation of the impact of variations of device geometry and doping on device performance,
- and finally, the enabling of compact models to treat aggressively scaled highly three-dimensional transistors and interconnects, including the impact of systematic and stochastic variations..

The simulation approach and tool flows include improved and tightly integrated topography simulations and a new set of advanced models for nanodevice simulation, which were developed in the SUPERAID7 work packages WP3 and WP4, respectively.

2 Introduction

"Design-Technology Co-Optimisation" (DTCO) has, since its adoption by Intel more than 10 years ago, developed into a key methodology to reduce technology development costs and speed up time to market. Starting from technological specifications and customer requests Technology Computer Aided Design (TCAD) is used to simulate the performance of transistors and interconnects. This is followed by compact model and resistor-capacitor (RC) extraction for SPICE simulation, and the assessment of key technology performance metrics such as SRAM yield and Ring Oscillator performance.

The hierarchical simulation approach adopted in SUPERAID7 has extended and enhanced traditional DTCO insofar as it captures the impact of both systematic and stochastic process variations in a holistic fashion. Systematic process variations are caused by non-idealities of process equipment or by layout/pattern effects, and require that a simulation flow should start at the equipment level, in such a way as to be able to trace the variations through the entire process flow, device operation, and at the circuit level where their impact can be finally assessed. Generally speaking, SPICE compact modelling is the workhorse for the assessment and optimisation of circuit performance. With ever increasing impact of systematic and stochastic process variations, traditional SPICE models must be extended to accurately capture the effects of these variations, in order to minimize them. Furthermore, highly three-dimensional devices such as those addressed in SUPERAID7 were beyond the scope of compact models available before SUPERAID7, and therefore require the development of new ones. Finally, due to their increasing impact on circuit performance, interconnects and their variations must be included in any assessment of circuit performance.

This deliverable describes the approach adopted by the project, and sketches results obtained to achieve these targets. New compact models have been developed specifically for complex three-dimensional transistors. Hierarchical equipment, process and device simulation is used to provide the data necessary for the extraction of the compact model parameters. The hierarchical variability-aware statistical compact model extractor of Synopsys, Mystic, has been enhanced for advanced *More Moore* transistors for extracting comprehensive compact models, including process/systematic and statistical variability and capturing all correlations. Following this, we can investigate the performance and yield of variability-critical circuits using the statistical circuit simulator RandomSpice from Synopsys, whose capabilities have been extended to take advantage of the additional capabilities

provided by the enhanced compact modelling strategy. The hierarchical simulation tool chain and methodology implemented are essential for the development of early Process Development Kits (PDK), for evaluation of future technology options and for Design-Technology Co-Optimisation of advanced technologies, which are in urgent need by the semiconductor industry.

3 Integration and tool flow

To derive compact models that include the effects of process variations and their correlations, a hierarchical simulation approach is utilised, as shown in Figure 1.

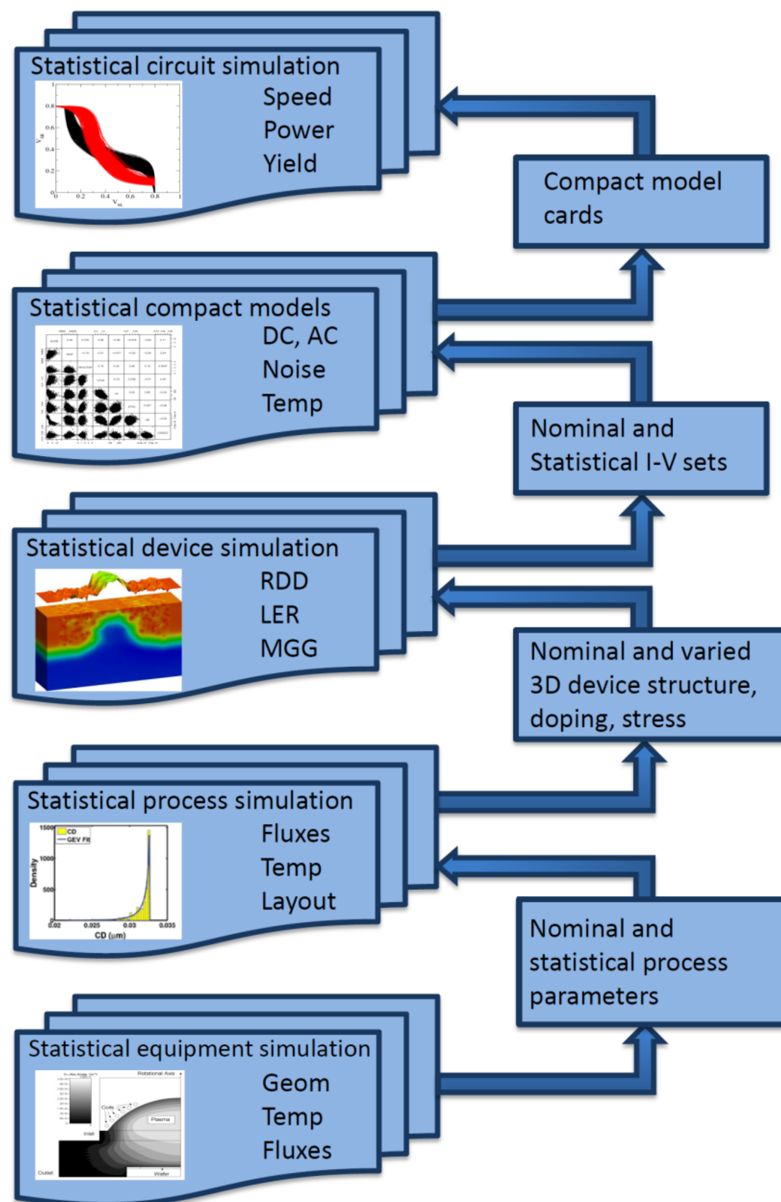


Figure 1: Impacts of variations to be considered at various levels of simulation

3.1 Equipment and Process Simulation

Process simulation is used not only to generate the nominal dimensions, dopant and stress distribution of the transistor to be investigated, but also to predict the changes of these

quantities in the case of systematic variations of the processes occurring. On a case-by-case basis, dedicated equipment simulation programs such as Q-VT [1], which are mostly based on computational fluid dynamics and plasma physics, are used as pre-processors to extract variations of critical quantities across the wafer, like the flux of reacting species just above the wafer. These quantities are then used as inputs to feature-scale process simulation. Lithography steps are specific, as it is not possible to differentiate between the equipment and the process level. The imaging properties of the lithography stepper, and the energy deposition in the photoresist and its development, must be simulated in parallel, and therefore with the same tool. For the simulation of the topography steps, i.e. lithography, etching and deposition, the programs Dr.LiTHO [2], ANETCH [3] and DEP3D [4] from IISB are used in an integrated version, whereas the other process steps are simulated with Sentaurus Process from Synopsys [5]. Nominal devices were then simulated with Sentaurus Device [5]. Process and potentially also equipment simulation is carried out for each instance of the variations to be considered. The Design-of-Experiment approach needed and applied to limit the number of simulations is outlined below in Section 5. Here, the three most interesting variations are considered, with three instances each (mean value and corners), leading to 27 variants of the final device for each pMOS and nMOS, before considering statistical variations.

3.2 TCAD-to-SPICE flow

Taking device structures that are generated using process and topography simulation tools through TCAD electrical device simulations, compact model extraction and finally circuit simulation to evaluate the effects of technology decisions on circuit and system design is a complex procedure covering several disciplines and fields of expertise. Producing a tool flow that is easy to use requires tight integration between the tools used at each stage, a user-friendly workflow environment and as much automation as possible. Tool integration, and the set-up of such a flow, has been one of the key development tasks within Work Package 5, and a necessary facilitator for the project as a whole, described in detail in Deliverable D5.1. In this deliverable, all stages of the flow are required, in order to capture variation in key process parameters within device compact models that can be used to look at the effect of such variation of circuit performance.

Sentaurus Workbench (SWB) [6] is the industry-standard workbench environment for advanced-node TCAD simulation. Integration of the former-GSS tools within SWB has been an on-going development as part of the integration work within SUPERAID7. Custom tool modules have been added to SWB for each of the GSS tools allowing them to be directly added like other Synopsys tools. Compatibility with Synopsys file formats has been improved allowing direct links between Synopsys Process and the Garand variability simulator, and output in TDR and PLT format allows visualisation in Sentaurus Visual.

All of these integration developments mean that the TCAD-to-SPICE flow can be used seamlessly to take device structures from process simulation (from Sentaurus Process and partner tools as described above) through process and statistical variability TCAD simulations and variability-aware compact models, to SPICE circuit simulations, all within an integrated SWB deck. This greatly streamlines the whole process, particularly as the Enigma tool takes care of the flow of simulation data through all stages, by use of a database.

4 Process simulation of nanowire devices

The fabrication of nanowire transistors has been demonstrated by CEA Leti [7]. Detailed information about their fabrication process was provided to the project partners in the form of technical specifications as well as electron micrographs (see, for example, Figure 2). At Fraunhofer IISB the process flow was modelled using the Synopsys process simulation software Sentaurus Process. For critical topography process steps, the simulation tools

ANETCH, BNDEDIT, DEP3D, Dr.LiTHO developed or extended within the project by Fraunhofer IISB were applied while using Synopsys Sentaurus Workbench as connecting framework for the individual tools. This framework allows us to execute the complete process sequence, and to inspect the intermediate results from a single unified interface, despite the different simulation tools used, while allowing it to be subsequently integrated with the TCAD-to-SPICE flow for the device and circuit simulations. Furthermore, we can define process parameters that are accessible by all connected software tools. This is not only relevant for process simulation, but also for the following statistical analysis that is implemented within the same framework.

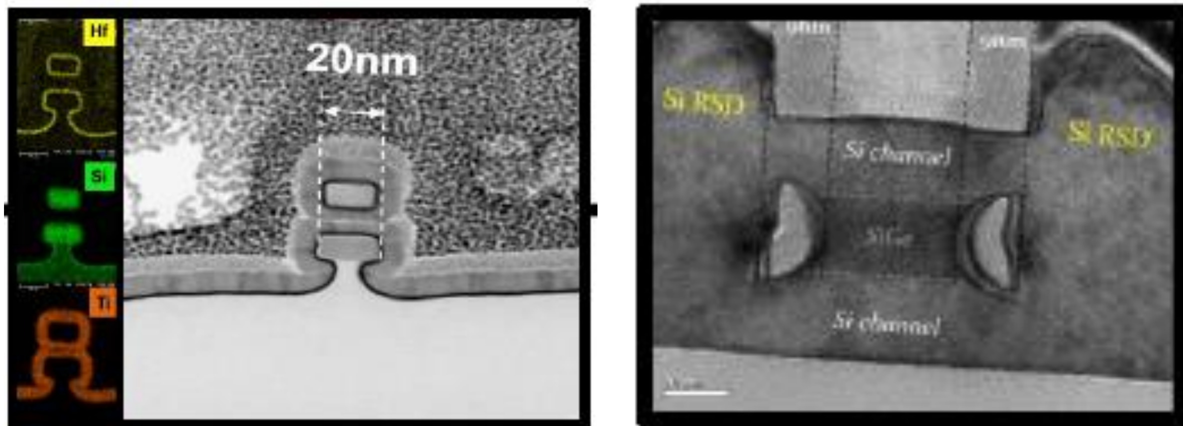


Figure 2: Example of nanowire transistors considered in this work: Cross section (left), along source-drain direction, with SiGe spacers (right)

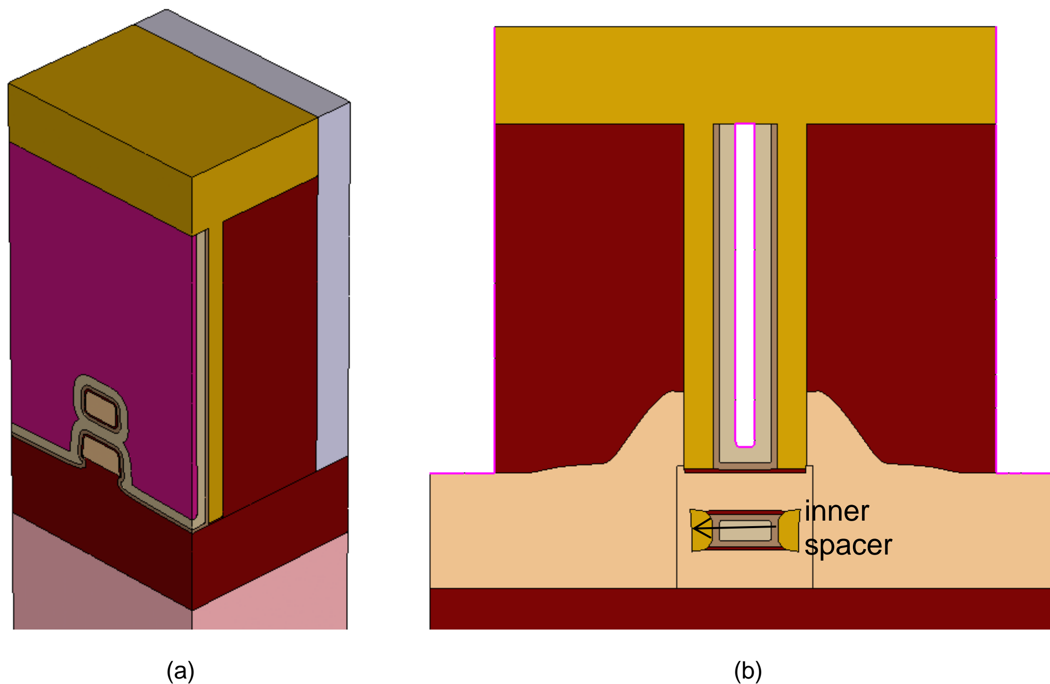


Figure 3: Simulated nanowire transistor: (a) Half of the structure cut across the nanowires, and (b) cross section along source-drain direction (right)

The simulated process flow starts with the definition of an SOI substrate on which the SiGe sacrificial layer (thickness H_{sac}) and the upper Si channel layer (thickness H_{cha}) are deposited. Etching of the layer stack to obtain fin structures is separated into two parts: First, a self-aligned double patterning (SADP) process including 193 nm immersion lithography is simulated using the tools Dr.LiTHO, ANETCH and DEP3D. Multiple sources of variations can be identified for the SADP process. For our study, we consider the defocus of the lithography

setup (F_{fin}) and the relative deviations of the thickness of the deposited nitride layer (d_{SADP}) and of the nitride etch depth (e_{SADP}) from their nominal values. Due to the physical simulation of deposition and etching, the actual thicknesses depend on the position on the structure e.g. due to shadowing effects. From the SADP structure the final width of the spacers is extracted and subsequently used as a mask width for the actual fin etching, which is performed with ANETCH. We consider the flows of neutrals ($\Psi_{fin,0}$) and ions ($\Psi_{fin,ions}$) in the plasma reactor as sources of variations. Gate lithography is simulated with Dr.LiTHO using 193 nm immersion technology. Defocus of the lithography setup is considered as a source of variations (F_{gate}). Dummy gate etching is simulated with the solid modelling tool BNDEDIT of Fraunhofer IISB as an ideal anisotropic process. The structure updates calculated with project tools are imported into Sentaurus Process to continue the simulation flow. This allows strain and doping effects to be respected. The following process steps consist of spacer fabrication, source/drain epitaxy, dummy gate removal, nanowire release, and gate stack deposition. Sources for variation within these steps included in this study were the annealing temperature for dopant diffusion T_{diff} as well as the germanium content x_{Ge} of the sacrificial SiGe layer (located between the two silicon channel layers). The latter has an influence on the shape of the inner spacers (marked in Figure 3) because of the dependence of the SiGe etch rate on the germanium content for the wet chemical process applied for inner spacer fabrication.

5 Process parameter sensitivity and choice of DoE parameters

A group of ten parameters was selected to be candidates for the benchmark study. These parameters are expected to have a measurable influence on the device characteristics and are easily accessible within the process flow. The influence of variations of the process parameters were evaluated via process simulation using the simulation flow described above and device simulation of the transfer characteristics using Sentaurus Device. We investigated the nominal device in comparison to two devices for each parameter representing the upper and lower limit of the respective variations. The range of variations considered here was based on internal knowledge of the project partners.

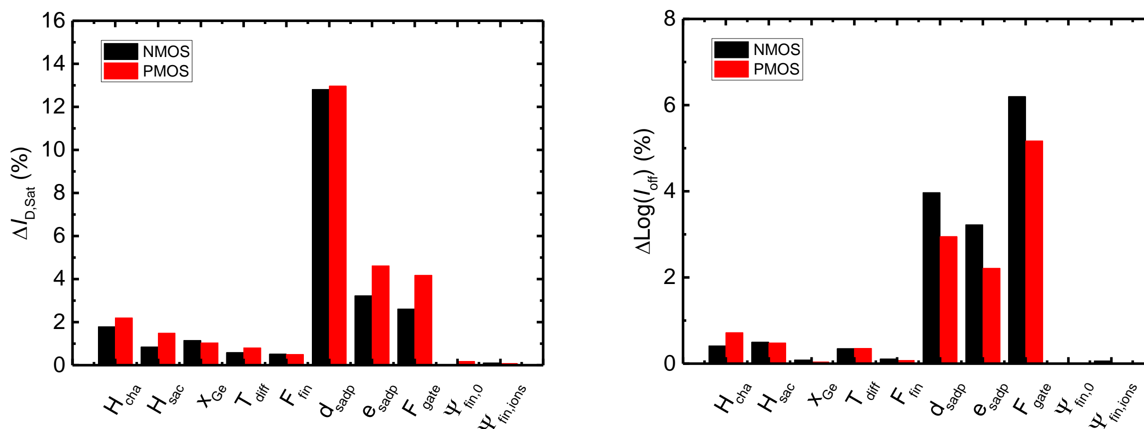


Figure 4: Influence of the variations of single parameters on the saturation current (left) and the logarithm of the off current (right).

The influence of the parameter variations on the saturation current and the off-current are displayed in Figure 4. For the statistical analysis of the device performance, we restrict the number of investigated process parameters to three. In principle, the selected parameters should represent the strongest influences on the device characteristics. This would include the parameters d_{SADP}, e_{SADP}, F_{gate}. However, the parameters should ideally cover different processes, such as etching, deposition, and lithography, in order to demonstrate the applicability of the SUPERAID7 approach to different scenarios. Furthermore, the influence of the parameters on the device characteristics should include indirect pathways that cannot

be described by variations of classical geometric FET properties like gate length, L, or channel width, W, to make use of the integrated SUPERAID7 framework in comparison to previously existing software solutions. For this reason, we decided to include the Germanium content of the sacrificial layer x_{Ge} in our study which influences position and shape of the inner spacers and thus an inherent property of nanowire devices. As d_{SADP} and e_{SADP} represent a similar influence on the device characteristics via the fin width W_{fin}, only d_{SADP} was included. Finally, the defocus of the lithography setup (F_{gate}) is included to form the three-parameter DoE space.

In the initial demonstrator presented in the previous deliverable (D5.4), quite conservative values were used for the variations in x_{Ge} and d_{SADP}. We found that it was difficult to resolve the structural changes induced by the parameter variation sufficiently above the numerical noise inherent in the mesh-based process simulation, resulting in small, and inconsistent variation in device characteristics. In addition, for the response-surface models that form the core of the variability-aware compact modelling methodology, it is important that the DoE variation cover at least 3σ of the expected process parameter variation. Therefore, for this final demonstrator we have increased the variation of x_{Ge} and d_{SADP}. The parameters, and their respective values and variation, that will be used in the following work are summarised in Table 1.

Process Parameter	***Symbol***	***Nominal***	***Variation***
SiGe mole fraction	x_{Ge}	30 %	± 3%
Gate litho defocus	F_{gate}	0	± 40 nm
Fin SADP deposition factor	d_{sadp}	1	± 10%

Table 1: Process parameters selected for the compact modelling study.

6 Device simulations

The Synopsys TCAD-to-SPICE flow is applied to take device structures produced from process simulation through to the extraction of compact models that represent the electric behaviour of the device. This requires several different stages of device simulation to obtain the electrical characteristics from which compact models can be extracted.

6.1 Process variability simulations

Sentaurus Device simulations are taken as the reference device simulations. Sentaurus Device is used for all of the “uniform” simulations, i.e. those that do not include sources of statistical variability. To capture the effects of the process variations across the DoE, Sentaurus Device simulations of the required I_D-V_D and I_D-V_G characteristics are run at each point in the DoE. The minimum requirement of I-V characteristics for uniform compact model extraction are I_D-V_G characteristics at low (V_D=0.05V) and high (V_D=0.9V) drain bias, and full I_D-V_D characteristics at multiple gate biases. These I-V characteristics produced at each point in the DoE will be sufficient for the extraction of process-variability-aware compact models.

In Figure 5 we present an analysis of the effects of varying each individual process parameter on key figures of merit (FoM). Here the blue lines show the effect of x_{Ge}, the orange lines show d_{sadp} and the yellow lines show F_{gate}. Each line has three data points with the centre point representing the nominal parameter value, while the left and right points respectively represent the negative (-ve) and positive (+ve) variation in parameter value, as provided in Table 1.

Compared to the trends observed in Deliverable D5.4, the larger variations applied to x_{Ge}, and d_{sadp} here overcome the noise present in the previous results, leading to more consistent trends. The “V”-shaped response to F_{gate}, that was analysed in detail in D5.4, remains

present. It is also clear that d_{sadp} has a strong influence on the on-current, which is something that was observed in the original sensitivity analysis of the different process parameters.

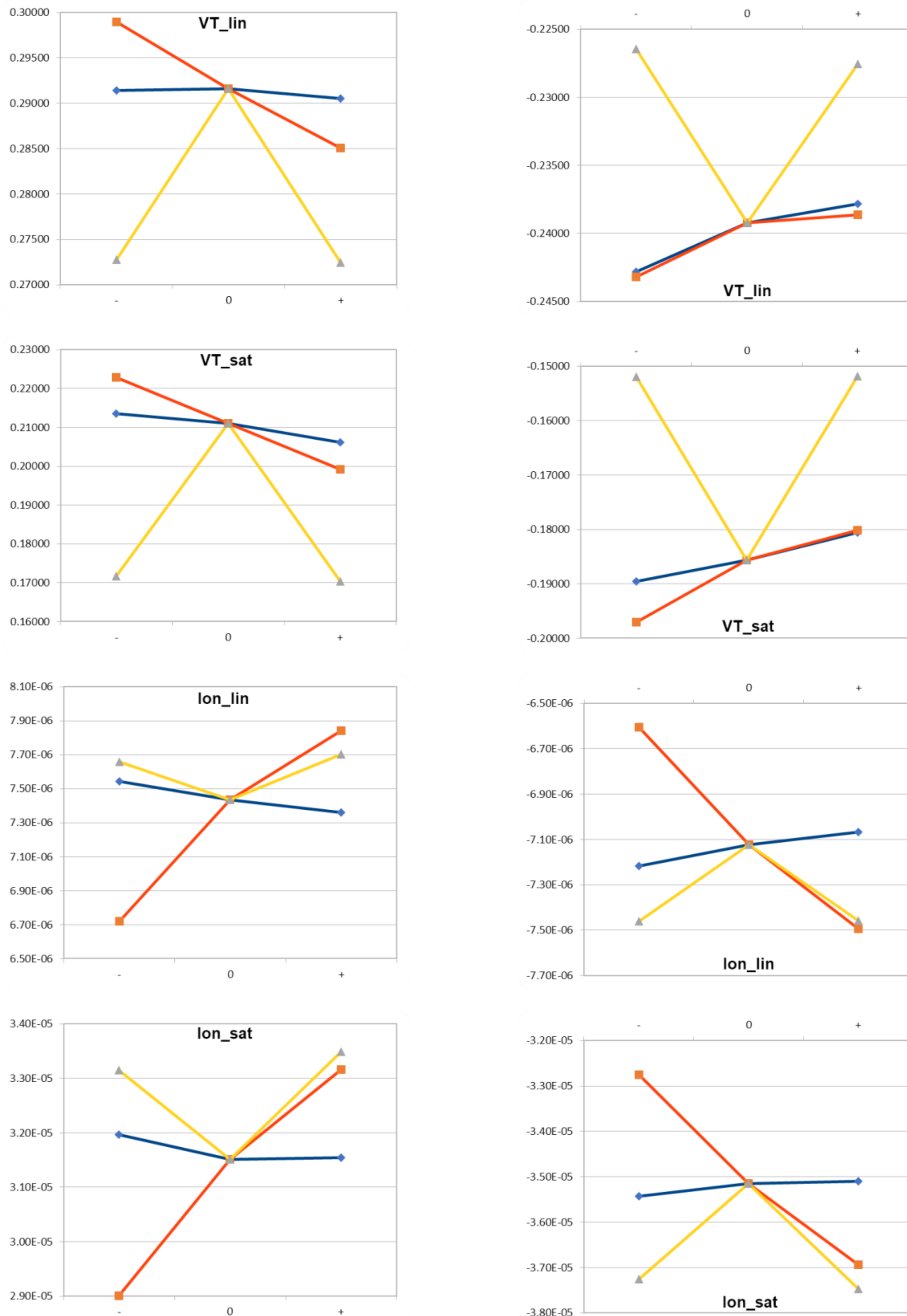


Figure 5: Variation of key figures of merit with the -ve, nominal and +ve variation of each process parameter for left: nMOS and right: pMOS. Key: blue - x_{Ge}; orange - d_{sadp}; yellow - F_{gate}

6.2 Statistical variability simulations

To capture the statistical variability effects, the dedicated statistical variability (SV) simulator Synopsys Garand is used. This simulator was developed by GSS and Synopsys specifically to address the issue of statistical variability in nanoscale MOSFETs, having the capability to automatically introduce the key sources of SV, such as random discrete doping, line edge roughness, and granularity of metal or polysilicon gates.

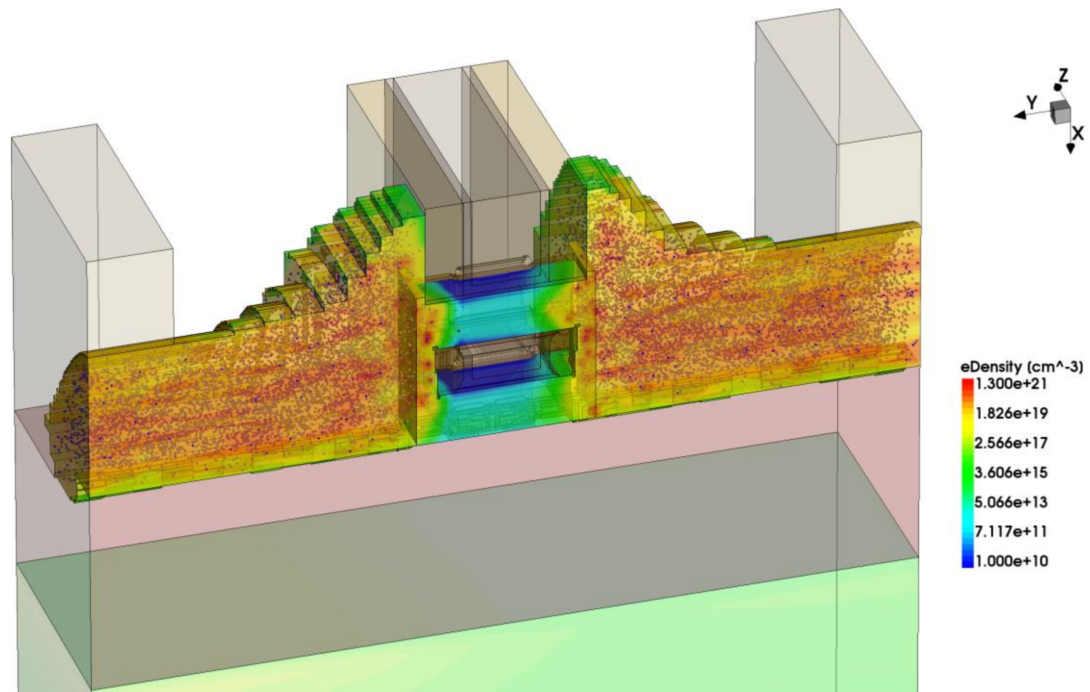


Figure 6: Benchmark nanosheet device simulated in Garand with random discrete dopants.

For the 5nm technology being considered here, it is expected that metal gate granularity will no longer be a significant source of SV, as gate-last processing will lead to a mostly amorphous gate metal. The sources of SV considered here are random discrete dopants (RDD) and line edge roughness (LER). RDD are generated statistically using a rejection technique based on the local nominal (continuous) doping concentration at each silicon lattice site. As such it depends entirely on the continuous doping profile obtained from the process simulation, with no other parameters to consider. Line edge roughness is characterised by a rms amplitude and a correlation length. For such small technology the variation due to line edge roughness will manifest almost purely as gate length variation, with little variation across the width of the device, so here a large correlation length is used. The overall gate length variation should also be well controlled, with a total (3σ) variation of approximately 1.1nm. Therefore, the rms amplitude (1σ) for the independent random lines used on either side of the gate is 0.25nm.

The dominant source of SV in these devices will be RDD. An example of RDD within the benchmark nanosheet structure is shown in Figure 6, illustrating the local variations in carrier density due to the discrete dopants.

The TCAD statistical ensemble size used in this case is 500. This has been increased from the 200 devices used in Deliverable D5.4, in order to provide more accurate statistics. The 500 different I_D-V_G characteristics obtained for the nominal devices are shown in Figure 7.

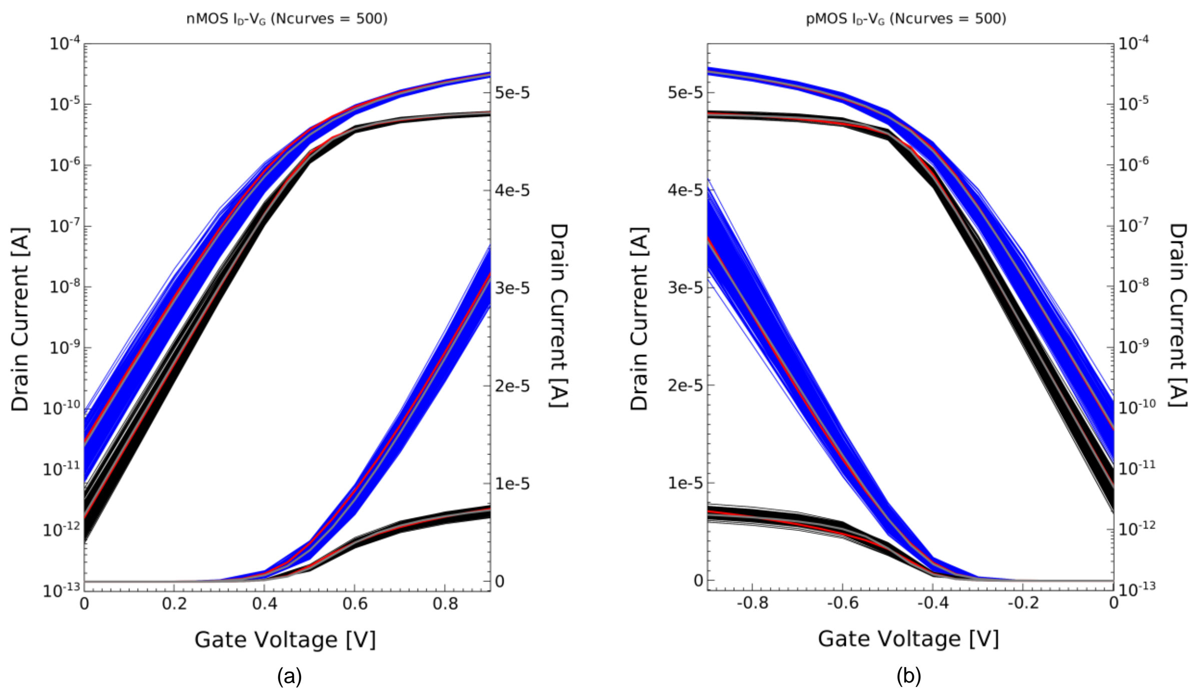


Figure 7: Id-Vg characteristics for the (a) nMOS and (b) pMOS devices at the nominal point in the DoE, with a statistical ensemble of 500 devices. Black curves @ Vd=0.05V and blue curves @ Vd=0.9V

7 LETI NSP model for nanosheet devices

7.1 Overview of the Leti NSP model

The LETI NSP model is a surface-potential-based model dedicated to advanced 3D CMOS device architectures. The model was developed with special emphasis on supporting vertically-stacked nanowire/nanosheet Gate-All-Around (GAA) CMOS technologies, and fits naturally with the stacked nanowire architecture that is investigated in this project.

LETI NSP is constructed in a hierarchical way with two levels of parameter sets: a global-mode parameter set, and a local-mode parameter set. The actual model evaluation is based on the local parameter values. In global mode, the local parameter value will be calculated through the scaling rules, using both the global model card and the device geometry information; in local mode, the local parameter value is directly obtained from the local model card, and there is no need to provide device geometry information such as gate length.

In the TCAD-to-SPICE flow, instead of using the global mode to describe devices with different geometries, the Response Surface Model (RSM) approach is applied. RSM can not only capture the device geometry-dependent effects, but also the impact of non-geometry parameters, such as implantation energy, annealing condition, lithography defocus, etc., on device electrical characteristics. To use the RSM approach, only the local mode is required for SPICE modelling of individual device.

7.2 Stacked-nanowire related parameters

In the LETI NSP compact model, the selection of the device architecture is determined by the SWGEO model parameter:

SWGEO	Device Architecture
0	Vertically-stacked nanowire/nanosheet gate-all-around MOSFET
1	FinFET MOSFET
2	Vertical nanowire/nanosheet gate-all-around MOSFET

Table 2: Options for the SWEGO parameter

For the benchmark vertically-stacked nanowire MOSFET used in this deliverable, SWGEO of 0 is used in the model card.

The stacked nanowire / nanosheet architecture targeted by the LETI NSP model is illustrated in Figure 8. The parameters used to describe the nanowire / nanosheet architecture are presented in Figure 8 as well. Special attention needs to be paid to parameter *W*. Normally an instance parameter, *W* is the device width, and similar to gate length parameter *L*, in the local mode it will not have an impact on device characteristics. However, in nanowire / nanosheet devices, instance parameter *W* in NSP no longer relates to the traditional device width concept, it is the width of the nanowire / nanosheet. Consequently, unlike the FinFET counterpart, using a different *W* in the SPICE netlist with a local model card will generate different results. The propagation of *W* in the flow is closely monitored to ensure consistency between model extraction and circuit simulation.

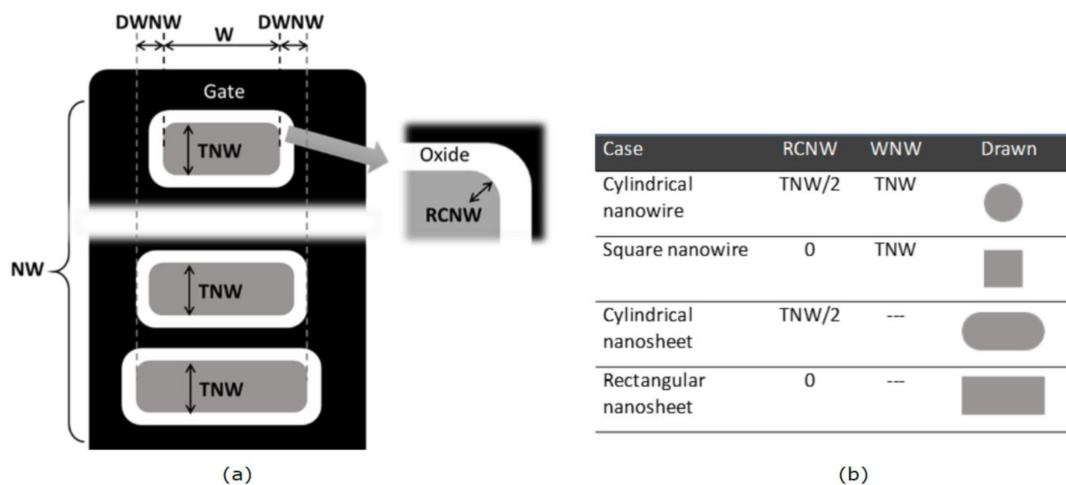


Figure 8: a) Cross-section and (b) typical cases of the stacked nanowire/nanosheet MOSFETs

As a summary, in the setup of the LETI NSP model card for a vertically stacked nanowire device, some parameters are set specifically according to the nanowire architecture.

7.3 Parameter extraction strategy

In the TCAD-to-SPICE flow, as illustrated in Figure 9, the SPICE modelling is divided into three stages: uniform device extraction stage, the response surface model extraction stage, and, finally, the statistical model extraction stage. The aim of the uniform device extraction stage is to provide the base SPICE model for the target device; the aim of the response surface model extraction stage is to provide SPICE models that can cover device global process variation; the aim of the statistical model extraction stage is to provide SPICE models that can cover device local statistical variability.

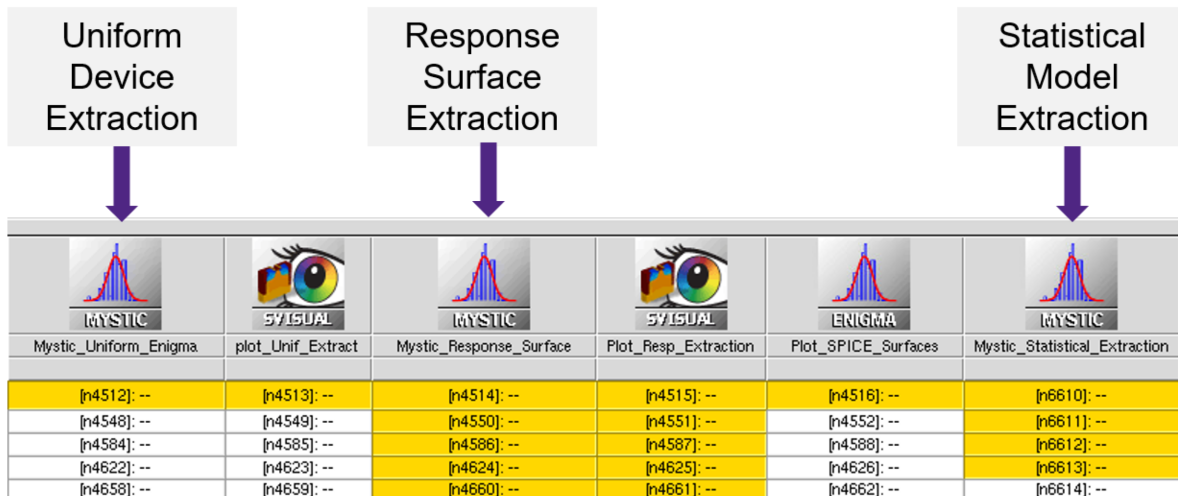


Figure 9: SPICE model extraction stages in the TCAD-to-SPICE flow

A comprehensive uniform I-V extraction strategy is developed which consists of two sub stages: Low drain stage and high drain stage. With carefully selected parameters and designated steps, short channel effects and low/high field transport properties are properly captured by the model. Using the SPICE models obtained from the uniform extraction stage as the base models, a comprehensive strategy is developed to capture the impact of the global variation of key process parameters on device characteristics, by re-extracting a carefully selected subset of the SPICE model parameters (the response-surface parameters) for each point in the DoE grid. These parameters can then be used to construct the response-surface models to generate parameter values covering the whole TCAD DoE space, including points in the process space that are not aligned with DoE grid points. Thus, SPICE models can be obtained for any process points (off-grid or on-grid) within the DoE space. Similarly, a statistical parameter extraction strategy is developed by re-extracting a carefully selected subset of the SPICE model parameters that capture the statistical local variations at a DoE point.

8 Device compact model extraction results

8.1 Mystic Extraction Results

8.1.1 Uniform Extraction

Firstly, full, nominal device models for the SUPERAID7 benchmark nanowire devices need to be extracted. This is only done for the nominal device, i.e. the centre point in the DoE. For the nominal models, the simulated results from Sentaurus Device are uploaded as target data, and the uniform extraction strategy has been implemented with the compact model extraction tool Mystic and integrated into the TCAD-to-SPICE flow within Sentaurus Workbench. The parameter extraction results for both nMOS and pMOS are summarised in Figure 10 and Figure 11, comparing the extracted model with the original TCAD data.

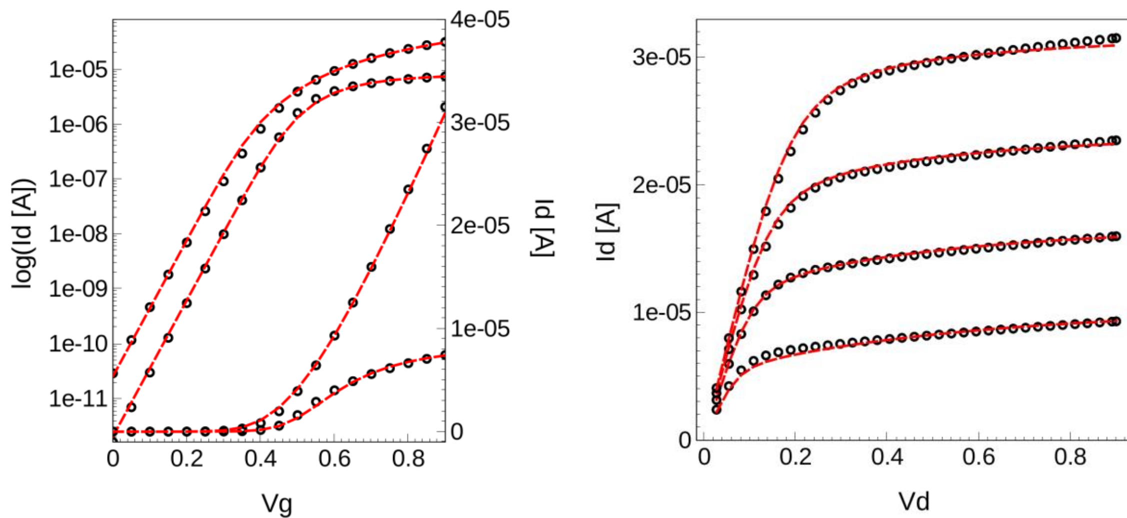


Figure 10: nMOS nominal model extracted by Mystic for SUPERAID77 benchmark nanowire devices. (a) I_D-V_G at Vd=0.05V & 0.9V, and (b) I_D-V_D at Vg=0.6V,0.7V,0.8V & 0.9V

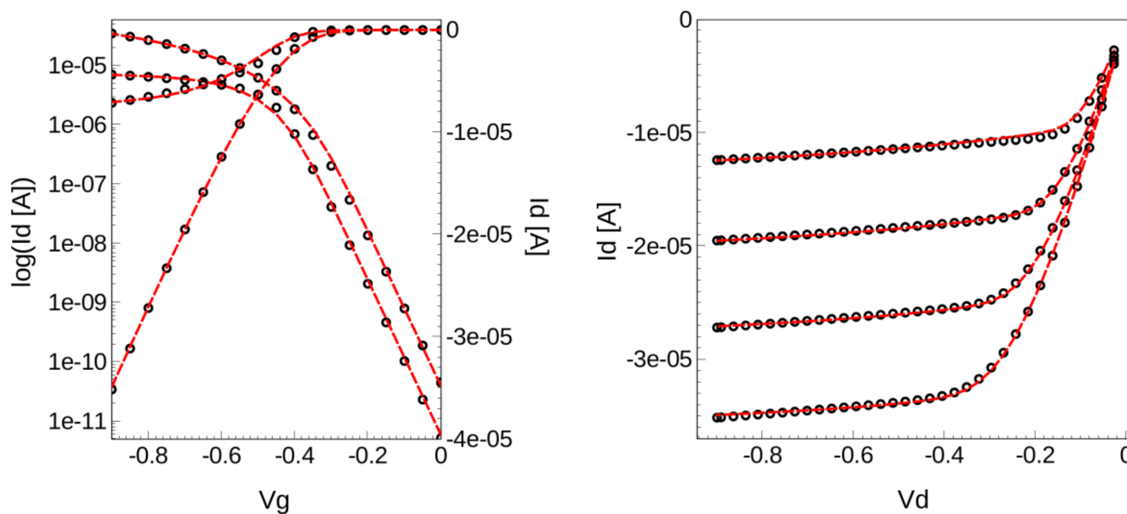
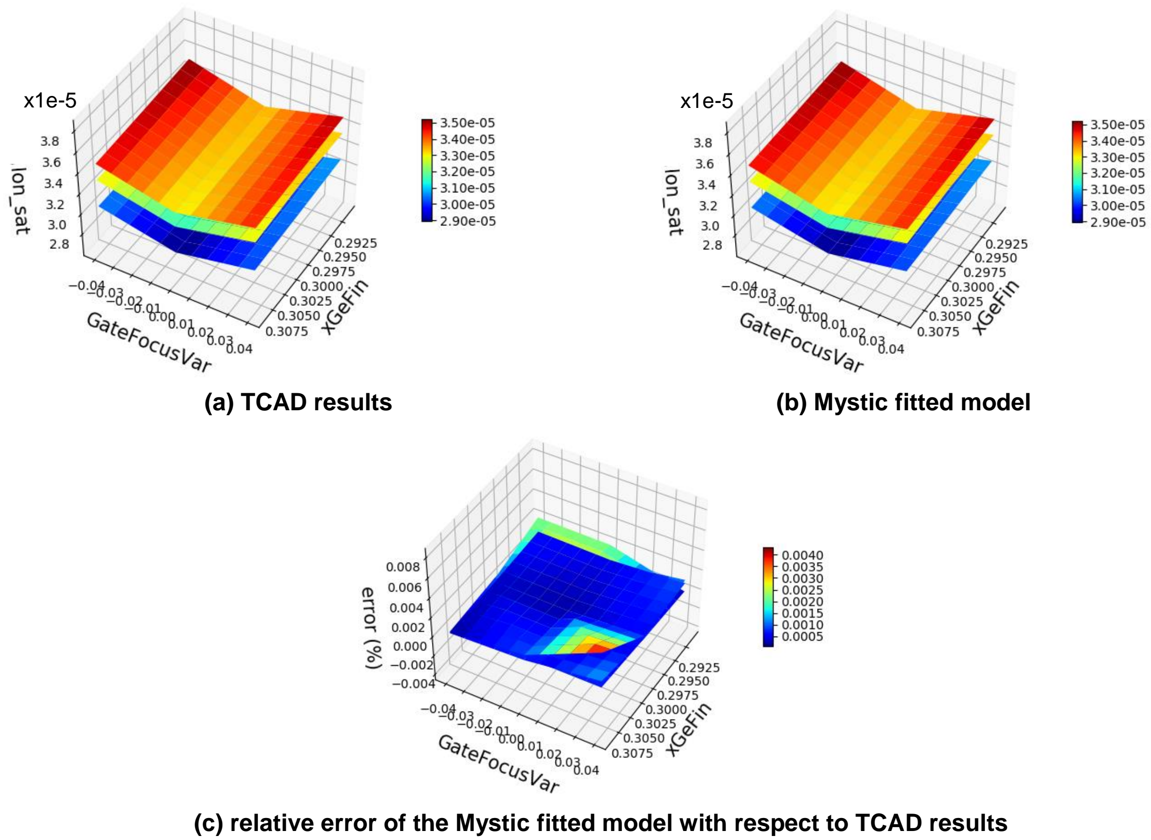


Figure 11: pMOS nominal model extracted by Mystic for SUPERAID77 benchmark nanowire devices. (a) I_D-V_G at Vd=-0.05V & -0.9V, and (b) I_D-V_D at Vg=-0.6V, -0.7V, -0.8V & -0.9V

8.1.2 Response Surface Extraction

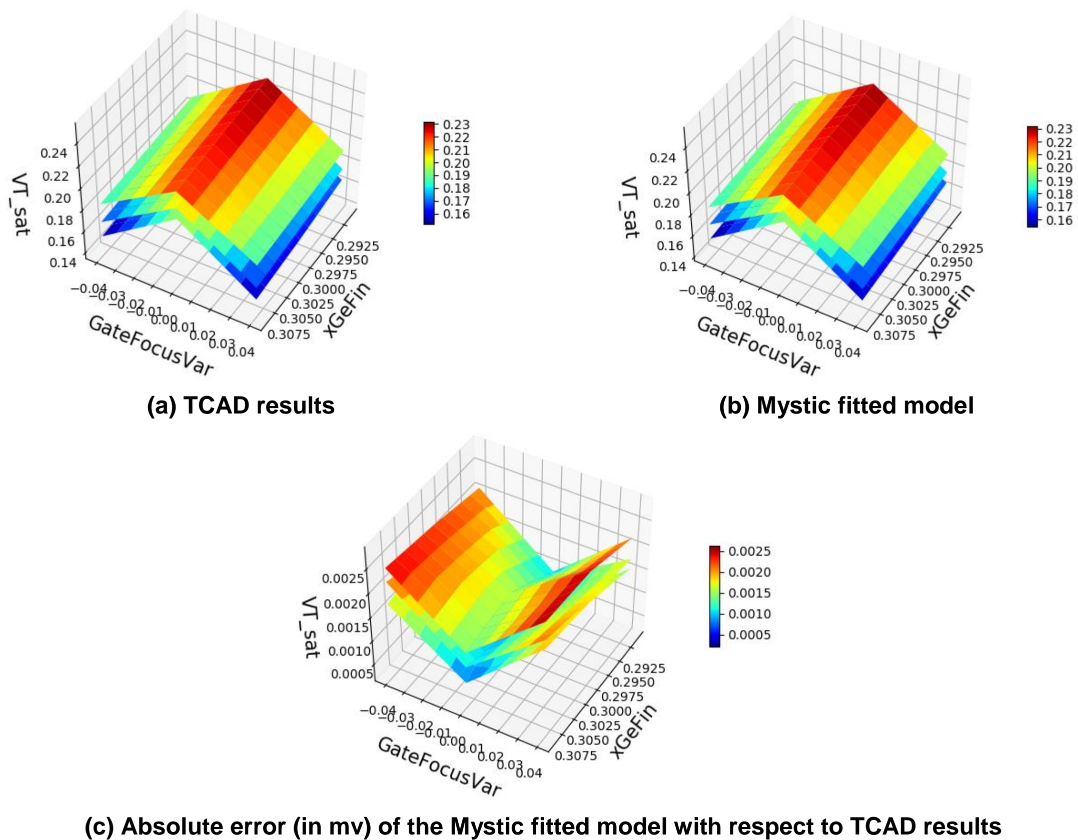
Then, the extracted nominal model is used as the base model. The response surface model extraction strategy has been implemented to cover the global process variation. The nMOS results are shown in Figure 12 & Figure 13. Here the “V”-shaped response, particularly for gate litho defocus, that was observed in the TCAD results (see Section 6.1) is clear in the response surface. Mystic-fitted models capture the variation of key figures of merit very well, with maximum 0.0035% error of Ion_sat for nMOS, and maximum 0.03% error for pMOS. The error of threshold voltage is defined as the absolute difference between TCAD and SPICE modelling. For nMOS, the maximum Vth_sat fitting error is less than 3.5mV, and for pMOS, is less than 0.8mV.



(a) TCAD results **(b) Mystic fitted model**

(c) relative error of the Mystic fitted model with respect to TCAD results

Figure 12: Response surface for nMOS Ion_Sat covering the process variation DoE (different surfaces correspond to the three different DoE values of Fin SADP deposition factor)



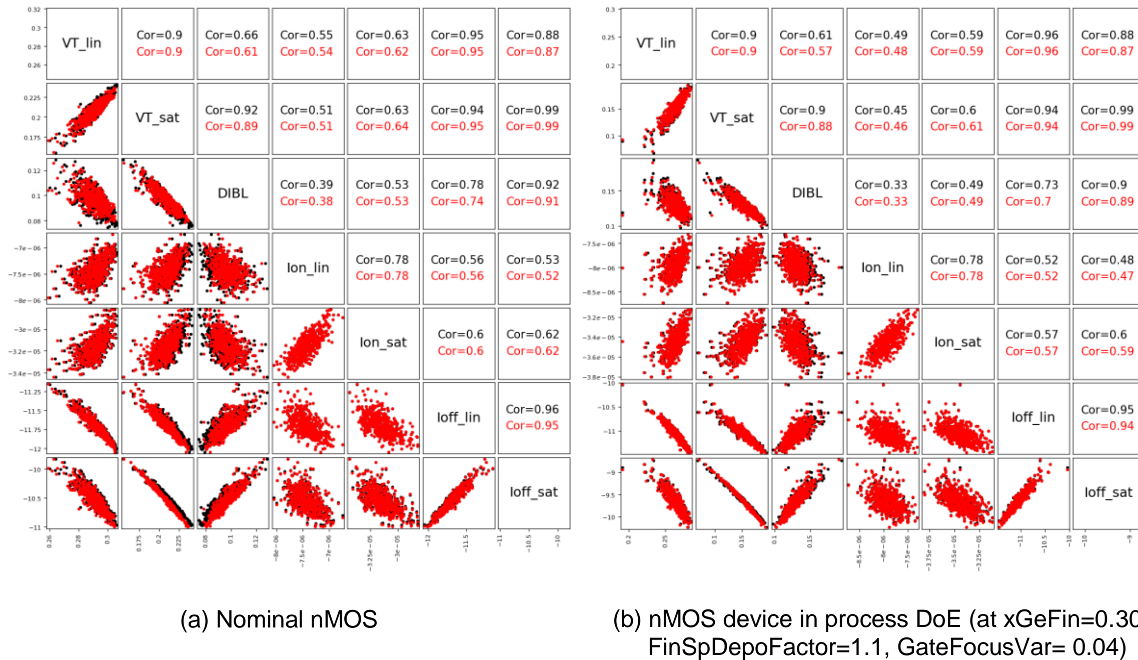
(a) TCAD results **(b) Mystic fitted model**

(c) Absolute error (in mv) of the Mystic fitted model with respect to TCAD results

Figure 13: Response surface for nMOS Vt_Sat covering the process variation DoE (different surfaces correspond to the three different DoE values of Fin SADP deposition factor)

8.1.3 Statistical Extraction

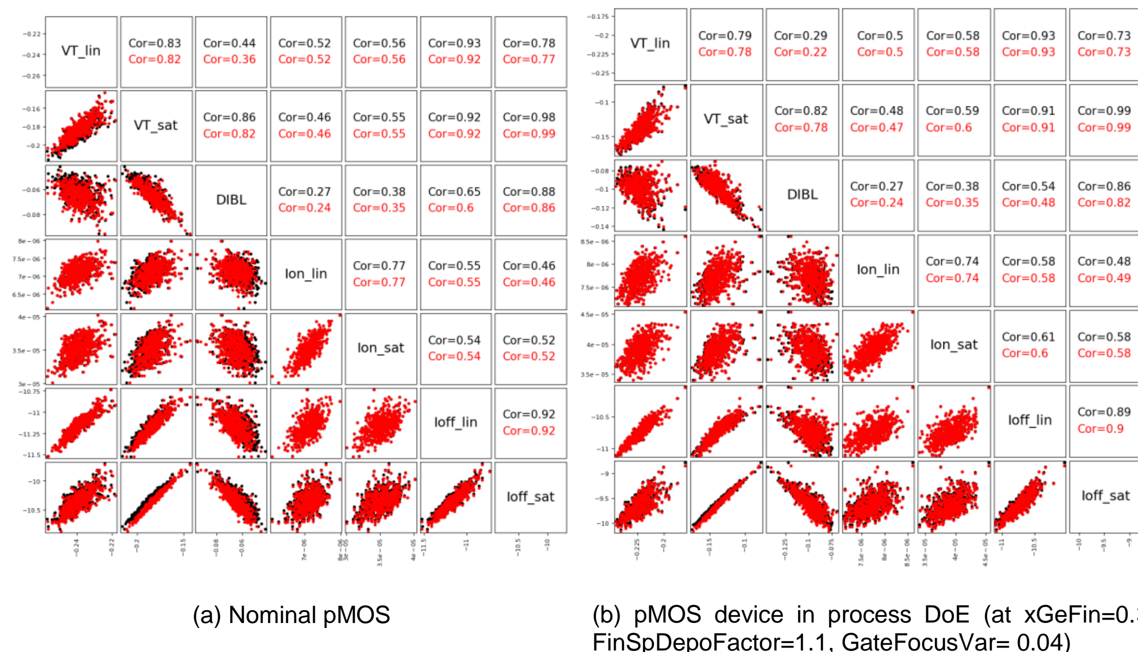
The statistical parameter extractions have been carried out for the SUPERAID7 benchmark nanowire devices. One major advantage of our statistical extraction strategy is the accurate capture of the distribution and correlation of key device figures of merit (FoM). As demonstrated in Figure 14 and Figure 15 for both nMOS and pMOS, the correlations of device FoM are fully captured by the statistical compact modelling approach.



(a) Nominal nMOS

(b) nMOS device in process DoE (at xGeFin=0.309, FinSpDepoFactor=1.1, GateFocusVar= 0.04)

Figure 14: Statistical model fitting results for nMOS nanowire devices (Black: TCAD results; red: compact model results)



(a) Nominal pMOS

(b) pMOS device in process DoE (at xGeFin=0.309, FinSpDepoFactor=1.1, GateFocusVar= 0.04)

Figure 15: Statistical model fitting results for pMOS nanowire devices (Black: TCAD results; red: compact model results)

8.2 RandomSpice Model Library

After successful extraction of compact models by Mystic, these models can be used to build a model library for RandomSpice using ModelGen technology. The advantage of ModelGen is that an (almost) infinite number of different device compact models can be generated that will all fit the same distributions and correlations in the FoM, matching the original TCAD results. This facilitates circuit simulations where usually a huge number of statistical circuit instances are needed. The RandomSpice model library can regenerate the process variation as predicted by TCAD simulations. As shown in Figure 16, the variation across the DoE space of key figures of merit are well recovered.

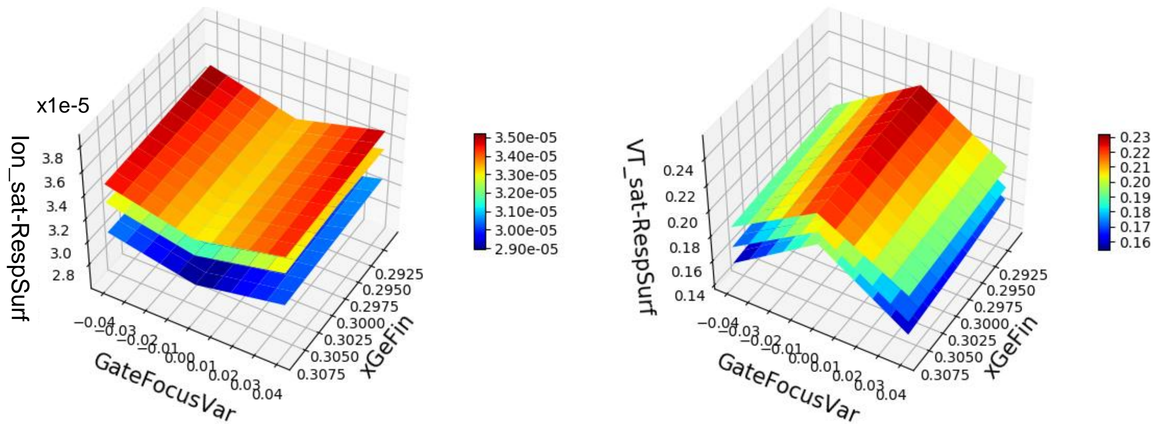
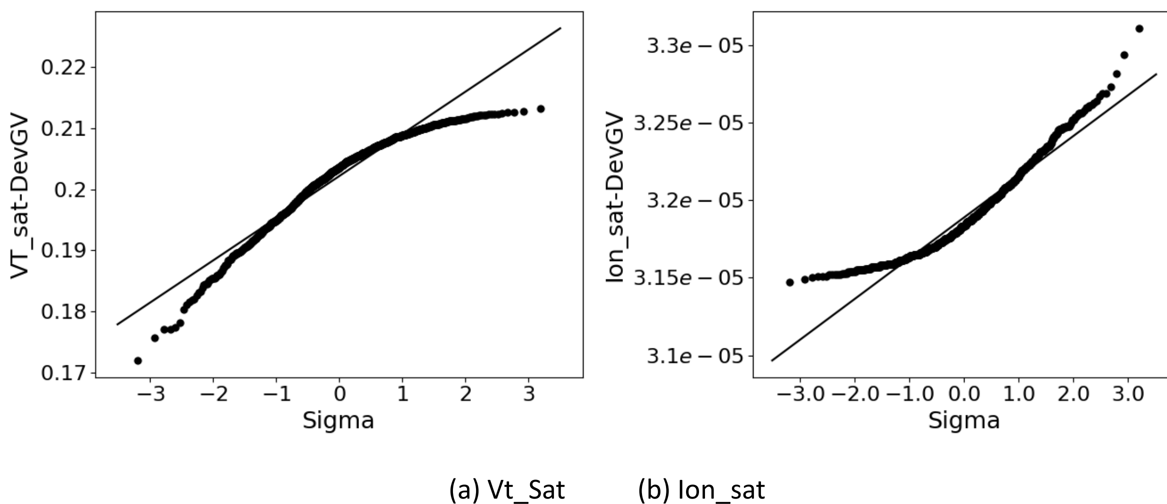


Figure 16: Regenerated response surface by RandomSpice covering DoE of nMOS nanowire devices. Similar to Figure 13, different surfaces correspond to the three different DoE values of Fin SADP deposition factor



(a) Vt_Sat (b) Ion_sat

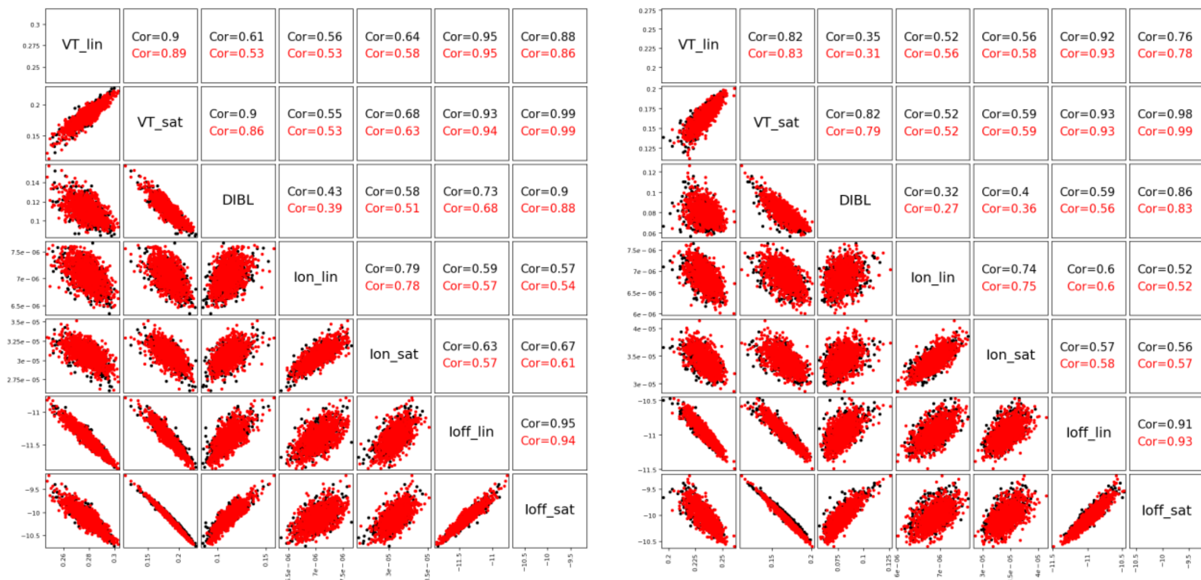
Figure 17: Regenerated response surface by RandomSpice covering DoE of nMOS nanowire devices when a Gaussian distribution for gate defocus factor is assumed

Assuming the gate defocus factor variable follows a Gaussian distribution with mean value of 0.0 and standard deviation of 0.01 µm, the impacts of global process variation on the distributions of key device FoM are illustrated in Figure 17, highlighting the skewed distributions introduced by the "V"-shaped response of the defocus variation. Considering the Vt_sat distribution, the highest Vt_sat occurs at the mean gate focus factor (peak of the Gaussian distribution), therefore there will be a large number of devices with close-to-maximum Vt_sat. At the same time, the minimum Vt_sat occurs at both +ve and -ve tails of the distribution in gate focus factor and therefore has significantly lower probability of

occurring. This is illustrated by a flattening of the distribution in Figure 17(a) towards higher Vt_sat, and a steepening towards lower values. This represents a skew in the distribution towards higher Vt_sat values. Ion_sat in Figure 17(b) conversely skews towards a lower current. An important effect is that the assumed symmetric (Gaussian) distribution of the gate defocus factor leads to a highly asymmetric distribution of the electrical data studied.

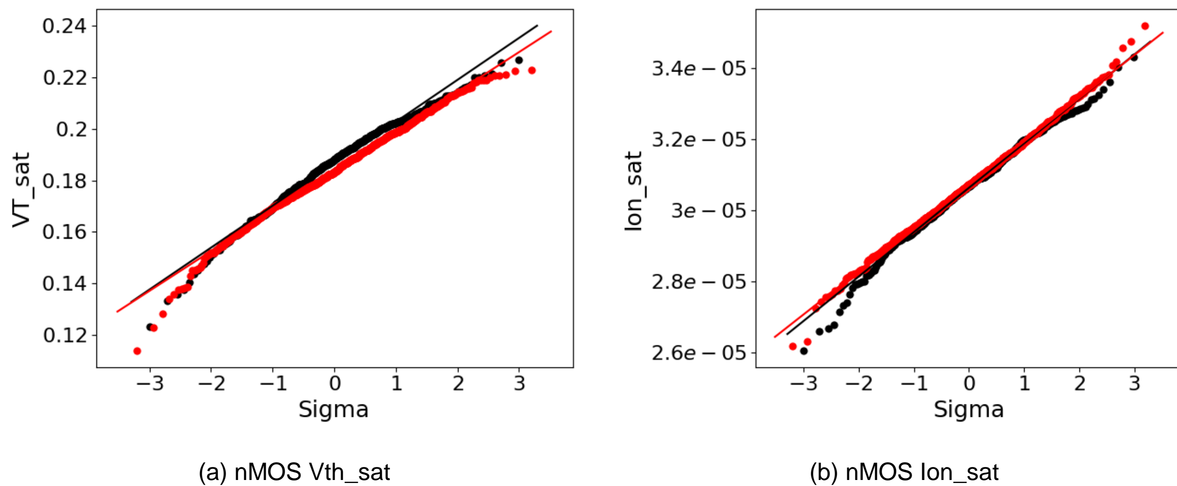
In this study, the TCAD statistical ensemble size is 500. Using the RandomSpice model library, a practically unlimited number of statistical device can be generated in statistical circuit simulation with preserved statistical information obtained from TCAD simulation within the same DoE space. Not only the statistical information of the on-grid points can be reproduced by the RandomSpice model library, but also off-grid points can be generated using the statistical distribution interpolation capabilities of ModelGEN. Thus, the RandomSpice model library can generate statistical information for any process points (off-grid or on-grid) within the DoE space.

Figure 18 to Figure 20 demonstrate that the RandomSpice library can regenerate statistical variation at the intermediate grid points. In this case, after the construction of the RandomSpice model library, statistical TCAD simulations can be carried out for arbitrary coordinates in the process DoE that do not correspond to those points where models have been extracted. In order to validate this, TCAD simulations were carried out, but Mystic extraction was *not* performed, for a statistical ensemble of 500 devices with local variation at an arbitrary point with xGeFin=0.3, FinSpDepoFactor=0.9, GateFocusVar=-0.04 (validation coordinate) in the process variation space. Then for comparison, 1000 HSPICE simulations were performed using RandomSpice to generate an ensemble of devices at that DoE location. As shown in Figure 18 to Figure 20, using the capabilities of RandomSpice it is possible to accurately generate arbitrary numbers of SPICE models that closely replicate the device behaviour, including correlation and statistical distributions of FoMs, predicted using TCAD.



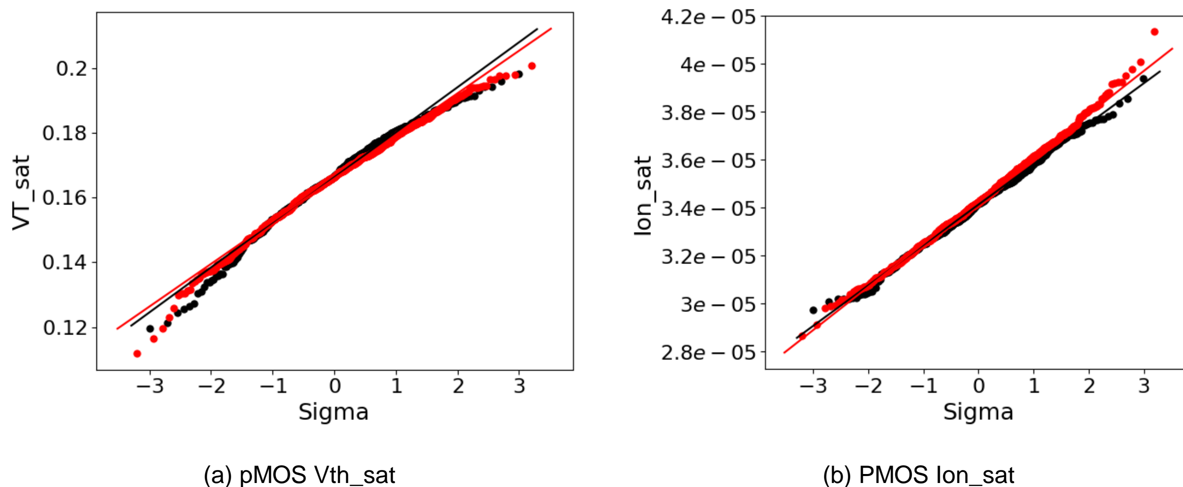
(a) nMOS device at the validation point. (b) pMOS device at the validation point.

Figure 18: 1000 HSPICE simulations using generated statistical compact models by RandomSpice, compared with 500 TCAD statistical simulations (Black: TCAD results; red: RandomSpice results)



(a) nMOS Vth_sat (b) nMOS Ion_sat

Figure 19: nMOS FoM distribution comparisons between 1000 HSPICE simulations using generated statistical compact models from RandomSpice, and 500 TCAD statistical simulation (Black: TCAD results; red: RandomSpice results)



(a) pMOS Vth_sat (b) PMOS Ion_sat

Figure 20: pMOS FoM distribution comparisons between 1000 HSPICE simulations using generated statistical compact models from RandomSpice, and 500 TCAD statistical simulation (Black: TCAD results; red: RandomSpice results)

9 5nm back-end structure

In this section we describe the generation methodology for transistor layout and the back end of line (BEOL) interconnect to be used as a circuit level demonstrator, and the tools and approaches used to extract the parasitic RC components associated with the interconnect wires.

9.1 Interconnect structure generation

To obtain a realistic 5nm back-end structure we have used the state-of-the-art process emulator Sentaurus Process Explorer [5]. This Synopsys tool allows the rapid synthesis of circuit scale structures given a layout file (e.g. GDSII format) and a process recipe. Figure 21 shows a schematic of the tool flow from the layout import/visualization, to the process recipe definitions and the actual process emulation execution (*Route*). The tool also allows the exploration of several process splits by means of a user-friendly Design of Experiment GUI.

Figure 22 shows an example of process flow development through the Process Explorer GUI. A succession of modules and steps define the flow. These steps are selected by the user from a library of predefined process steps of the tool (e.g. deposition or etch.), whose parameters can be modified by the user (e.g. deposition time). Once the flow definition is completed and has been tested, the flow recipe is stored in a database and can then be used with compatible layouts to generate physical structures. During flow creation, cell inputs and outputs can be defined by annotating special layers that denote contact connections such as Vdd or Vss (Figure 23). This is important when the structure is used for extracting RC netlists featuring all the necessary annotations to run through a SPICE simulation, as shown in the next section.

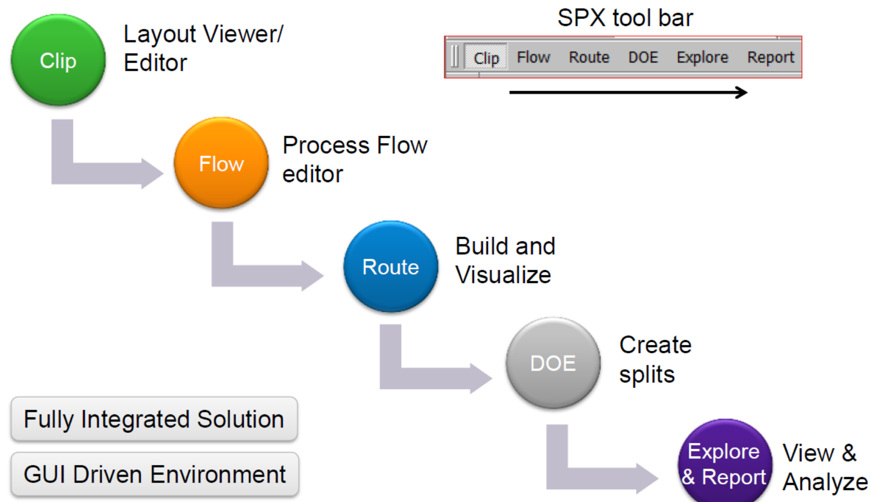


Figure 21: Sentaurus Process Explorer emulation flow.

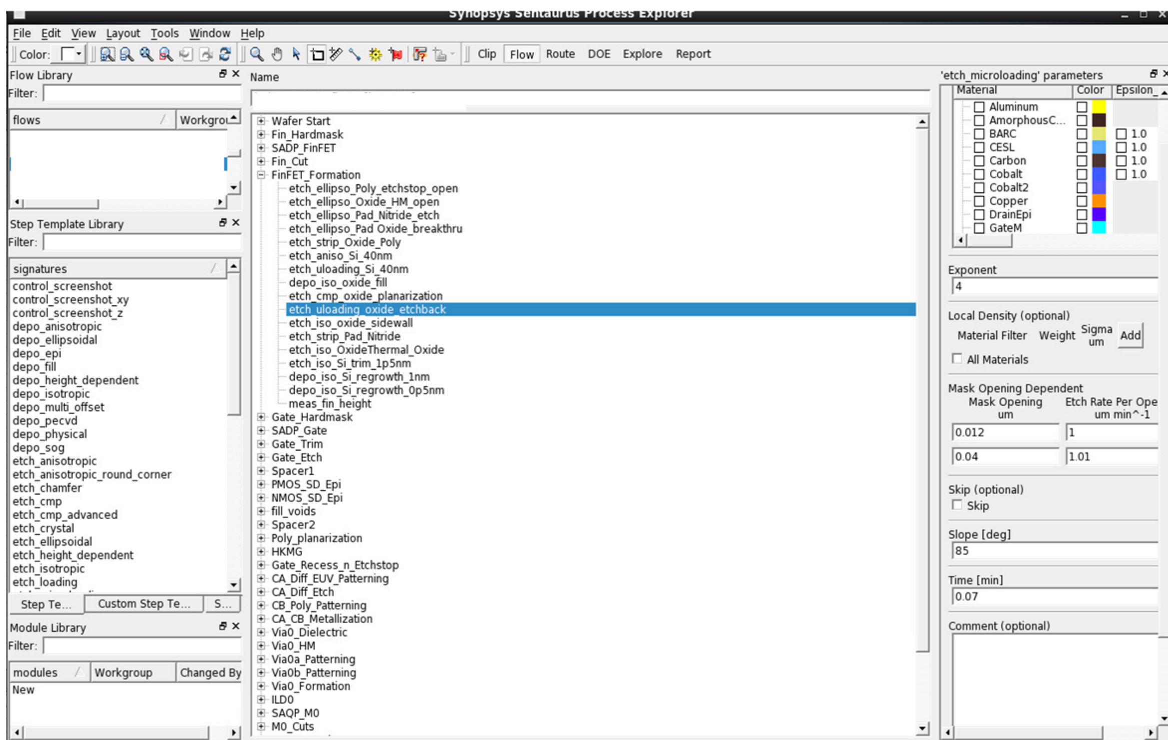


Figure 22: Example of Flow development through the Process Explorer GUI.

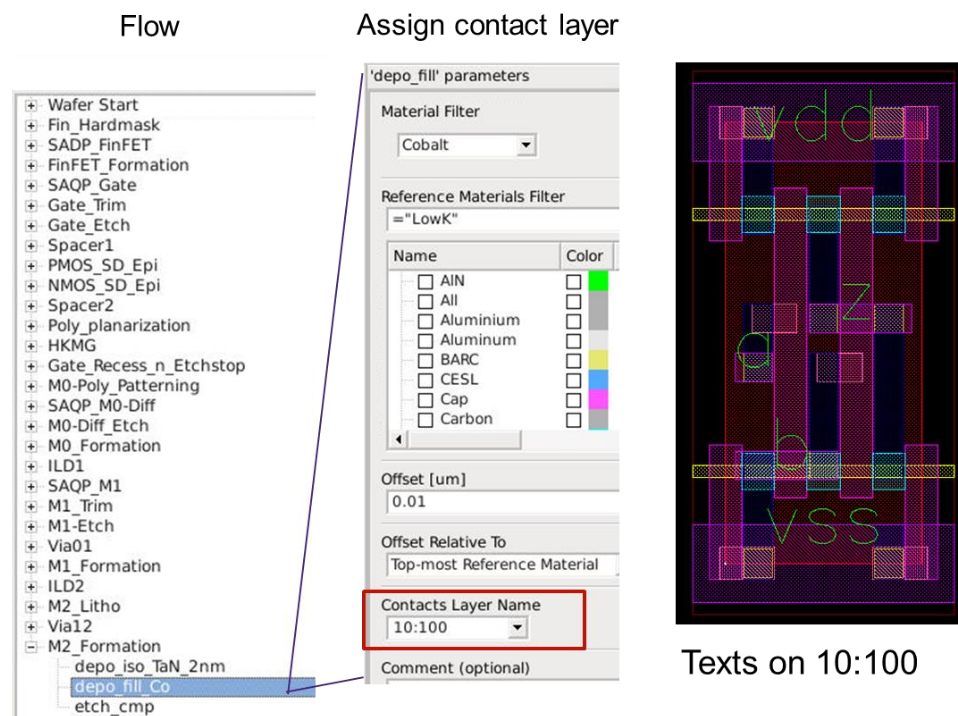
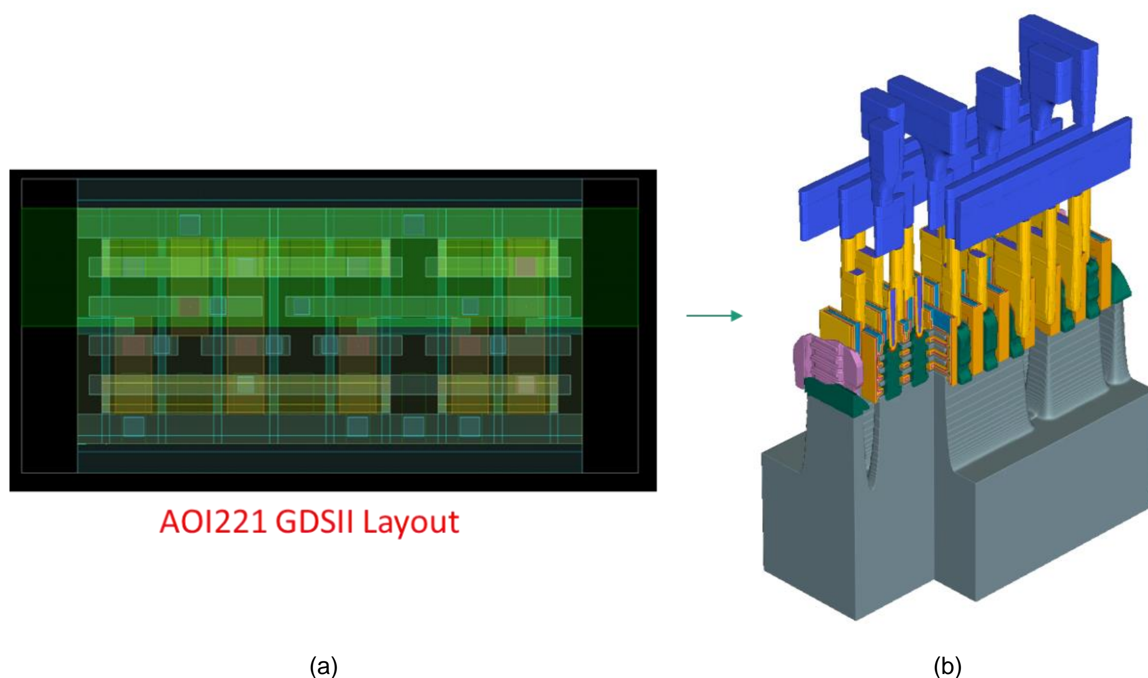


Figure 23:Process Explorer Structure and Layout Annotation

Figure 24 shows the GDSII Layout and the final 3D structure obtained from Process Explorer for our demonstrator AND-OR Invertor (AOI) standard cell, implemented using a representative 5nm technology which is used as a test case for the analysis presented in this deliverable.



(a) (b)

Figure 24: AOI221 standard cell for the 5nm technological node. (a) GDSII Layout and (b) 3D emulated process structure (right)

9.2 Compact models for interconnects

Once a 3D structure has been generated using Process Explorer, this can be used to extract the RC equivalent parasitic elements for the BEOL, which in combination with front-end compact models can be used to construct a complete SPICE netlist for circuit simulation of the AOI standard cell.

Raphael [8] is the industry-standard, 2D and 3D resistance, capacitance and inductance extraction tool. As a reference field solver, Raphael provides accurate parasitic models. trusted by major foundries. Interconnect parasitics generated by Raphael are included as part of their design reference guide.

Raphael allows users to:

- Analyse complex on-chip interconnect structures and the influence of process variation
- Create a database of parasitics for both foundries and designers to study the effect of design rule change
- Generate accurate capacitance rules for layout parameter extraction (LPE) tools
- Visualise output characteristics such as the potential distribution inside complex 3D shapes with Sentaurus Visual tool.

The core of the 3D solver is based on a Laplace solution of the electrostatic potential throughout the 3D structure. Figure 25 and Figure 26 show an example of the extracted equivalent circuit models for the parasitic resistances and capacitances in the AOI cell.

```
* Linked RC netlist:
* SPICE Models for Resistance (Ohm)
R_0_1      BM0X1UBV0X1              BM0X1UCM0X1                 2.4585e+00
R_2_3      TaN1X2UTiN2X8            TaN2X6UTiN2X10              1.1246e+04
R_4_5      TaN1X1UTungsten2X4       TaN1X1UTungsten2X5          4.1619e+01
R_6_7      TiAlN2X26UTiN2X39        TaN1X10UTiAlN2X27           1.2942e+04
R_8_9      TiAlN2X6UTiN2X7          TaN2X7UTiN2X11              2.3888e+04
R_10_3     TaN1X1UTiN2X9            TaN2X6UTiN2X10              1.8462e+04
R_11_12    TaN2X1UTiN2X3            TaN2X1UTiAlN2X1             2.4137e-01
R_13_14    p2g                      TaN1X4UTiN2X12              1.0069e+02
R_15_16    TaN2X6UTiAlN2X6          TaN1X2UTiN2X7               3.8696e+01
R_17_18    TaN1X2UTiAlN2X6          TaN2X7UTiAlN2X7             1.0089e+04
R_3_19     TaN2X6UTiN2X10           TiN2X10UTiNitrideX3         0.0000e+00
R_5_20     TaN1X1UTungsten2X5       TaN1X1UTaN2X5               9.1843e+02
R_5_21     TaN1X1UTungsten2X5       TaN1X1UTaN2X6               9.4563e+00
R_22_23    TaN1X4UTungsten2X8       TaN1X4UTungsten2X9          1.4106e+02
R_17_2     TaN1X2UTiAlN2X6          TaN1X2UTiN2X8               2.8724e+03
R_24_25    TaN1X3UTaN2X8            TaN2X9UTiN2X15              3.8043e+04
R_26_27    TaN1X10UTiAlN2X26        TiAlN2X27UTiN2X40           9.4894e+03
R_28_29    BM1X3UCM1X3              BM0X7UCM0X7                 5.0721e+01
R_30_31    TaN2X14UTiAlN2X14        TaN1X7UTiN2X24              9.1121e+00
R_16_32    TaN1X2UTiN2X7            TaN1X2UTiN2X10              6.2793e+01
R_33_25    TiN2X12UTiNitrideX6      TaN2X9UTiN2X15              1.6828e+02
R_34_35    TaN1X8UTiAlN2X15         TaN2X15UTiAlN2X15           0.0000e+00
R_36_37    TiAlN2X12UTiNitrideX9    TiNitrideX9UTungsten2X11    1.2659e+01
R_38_39    TaN2X15UTiN2X25          TaN1X7UTungsten2X14         1.0278e+01
R_40_41    BM0X10UCV0X17            BM0X10UBV0X17               0.0000e+00
R_42_43    TaN1X7UTiAlN2X14         TaN1X7UTaN2X14              0.0000e+00
R_44_45    TaN1X4UTaN2X10           TiN2X16UTungsten2X9         9.1333e+00
R_46_47    TiN2X26UTungsten2X15     TaN1X8UTungsten2X15         0.0000e+00
```

Figure 25: A snapshot showing a subset of the Spice models for Resistance as extracted by Raphael for the AOI221 cell.

```
* SPICE Models for Capacitance (F)
C_189_3      BM0X2UCV0X4              TaN2X6UTiN2X10            9.0341e-24
C_213_133    n4s                      n2g                       1.6310e-21
C_17_308     TaN1X2UTiAlN2X6          BM0X7UCV0X8               1.5918e-22
C_256_335    TiN2X20UTiNitrideX9      TaN2X23UTiN2X37           2.5173e-27
C_97_148     BV0X17UTiNitrideX19      TaN2X9UTiAlN2X9           4.8754e-26
C_211_99     BM0X4UCV0X3              TaN1X3UTiAlN2X9           1.5773e-22
C_29_291     BM0X7UCM0X7              TaN2X21UTiN2X35           3.9217e-28
C_278_130    BM0X8UCV0X16             BM0X3UCM0X3               8.5400e-21
C_114_46     TiN2X21UTungsten2X12     TiN2X26UTungsten2X15      1.1398e-23
C_213_56     n4s                      BV0X8UTiNitrideX9         1.2183e-19
C_101_341    TaN1X10UTaN2X27          TiN2X48UTungsten2X27      7.4799e-23
C_315_82     TaN2X22UTiAlN2X22        TiN2X11UTungsten2X6       2.4747e-27
C_206_56     SiGeBX7UTiNitrideX8      BV0X8UTiNitrideX9         8.9961e-21
C_185_238    BV0X19UCV0X19            TaN1X7UTiN2X25            4.4111e-26
C_119_255    TaN1X10UTiN2X40          n4g                       9.9739e-23
C_120_255    TaN1X10UTiN2X39          n4g                       1.5739e-22
C_246_22     TiAlN2X15UTiNitrideX12   TaN1X4UTungsten2X8        1.4502e-22
C_318_346    TaN2X20UTiAlN2X20        TiN2X29UTungsten2X16      4.3640e-24
C_262_346    TaN2X19UTiAlN2X19        TiN2X29UTungsten2X16      6.2598e-24
C_189_344    BM0X2UCV0X4              TiN2X3UTungsten2X1        7.5640e-24
C_168_359    TaN1X7UTaN2X15           SiGeBX1UTiNitrideX2       8.4968e-22
C_146_90     BV0X17UCV0X17            TaN1X8UTiN2X22            7.5331e-26
C_288_164    n3s                      TiNitrideX6UTungsten2X8   1.1783e-20
C_240_133    p1d                      n2g                       7.9638e-22
C_288_56     n3s                      BV0X8UTiNitrideX9         8.7365e-20
C_240_213    p1d                      n4s                       7.7031e-21
C_264_222    TaN1X1UTiN2X10           BV0X1UCV0X1               1.8014e-22
C_30_347     TaN2X14UTiAlN2X14        BV0X2UCV0X2               2.0778e-25
C_254_203    TaN2X6UTiNitrideX3       TiAlN2X13UTiN2X18         2.1566e-25
C_119_63     TaN1X10UTiN2X40          BM0X9UCM0X9               3.1626e-25
C_120_63     TaN1X10UTiN2X39          BM0X9UCM0X9               5.5835e-25
C_23_34      TaN1X4UTungsten2X9       TaN1X8UTiAlN2X15          1.8601e-22
C_23_61      TaN1X4UTungsten2X9       TaN1X8UTiAlN2X16          4.2266e-23
C_168_97     TaN1X7UTaN2X15           BV0X17UTiNitrideX19       2.3070e-25
C_14_326     TaN1X4UTiN2X12           n1d                       5.8497e-21
C_70_5       TaN1X4UTaN2X9            TaN1X1UTungsten2X5        7.8789e-23
```

Figure 26:A snapshot showing a subset of the Spice models for Capacitance as extracted by Raphael for the AOI221 cell.

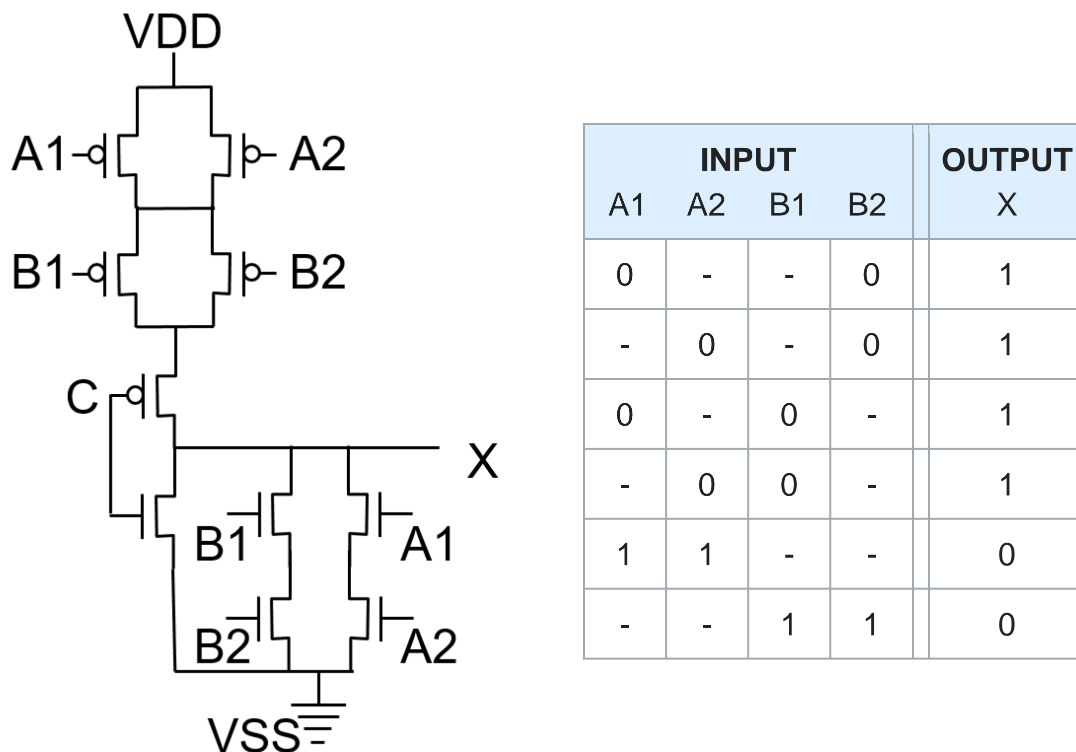
```
.subckt N2_aoi221_nanoslab A1 A2 B1 B2 C X VDD VSS VBP VBN
MP1 p1d p1g p1s VBP pmos l=0.01u w=0.028u m=1 nfin=1
MP2 p2d p2g p2s VBP pmos l=0.01u w=0.028u m=1 nfin=1
MP3 p3d p3g p3s VBP pmos l=0.01u w=0.028u m=1 nfin=1
MP4 p4d p4g p4s VBP pmos l=0.01u w=0.028u m=1 nfin=1
MP5 p5d p5g p5s VBP pmos l=0.01u w=0.028u m=1 nfin=1
MN1 n1d n1g n1s VBN nmos l=0.01u w=0.028u m=1 nfin=1
MN2 n2d n2g n2s VBN nmos l=0.01u w=0.028u m=1 nfin=1
MN3 n3d n3g n3s VBN nmos l=0.01u w=0.028u m=1 nfin=1
MN4 n4d n4g n4s VBN nmos l=0.01u w=0.028u m=1 nfin=1
MN5 n5d n5g n5s VBN nmos l=0.01u w=0.028u m=1 nfin=1
.include RCX_meas_RC.rc4Matrix.spi
.ends N2_aoi221_nanoslab
```

Figure 27: Sub-circuit for HSPICE simulation of the AOI221 cell including annotated netlist and extracted RC parasitics file.

Finally, front-end device models (as described in Section 8) and back-end RC parasitic models are grouped together to construct a SPICE netlist that enables the simulation of the AOI circuit performance though the Synopsys circuit simulator HSPICE [9]. Figure 27 shows an example illustrating how the parasitic elements and device models are combined using sub-circuit definitions and the inclusion of Raphael-produced netlists to produce a single SPICE netlist. This creates a seamless link between front-end and back-end flows which enables the simultaneous evaluation of the impact on circuit performance of both interconnects and devices.

10 Benchmark circuit simulations

As a demonstration for the whole methodology, circuit simulations are performed by RandomSpice on the AOI demonstrator cell, employing the compact model for the nanowire FETs combined with the back-end RC parasitic models. The AOI is implemented by CMOS circuitry as shown in Figure 28. The delay time between the output signal and the input signal is an important metric for an AOI, which mirrors characterisation arcs that would be used as part of standard cell library characterisation flows. To describe these delay times, we use a specific terminology for example the label *a1f-2-xr*, denotes the time taken between input A1 falling to the output X rising. To simplify the truth table of the AOI, we assume the 'C' input is tied to '0'. We then measure the input output delays using HSPICE simulations of the AOI cell operation.



INPUT				OUTPUT
A1	A2	B1	B2	X
0	-	-	0	1
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
1	1	-	-	0
-	-	1	1	0

Figure 28: CMOS implementation and truth table for the 2-2 And-Or-Invertor circuit. The dash in the truth table indicates that it does not matter what that input is.

Figure 29 shows the variation of several delay metrics over the process DoE. The response of the delays mirrors the V_T response of the device itself, which is to be expected.

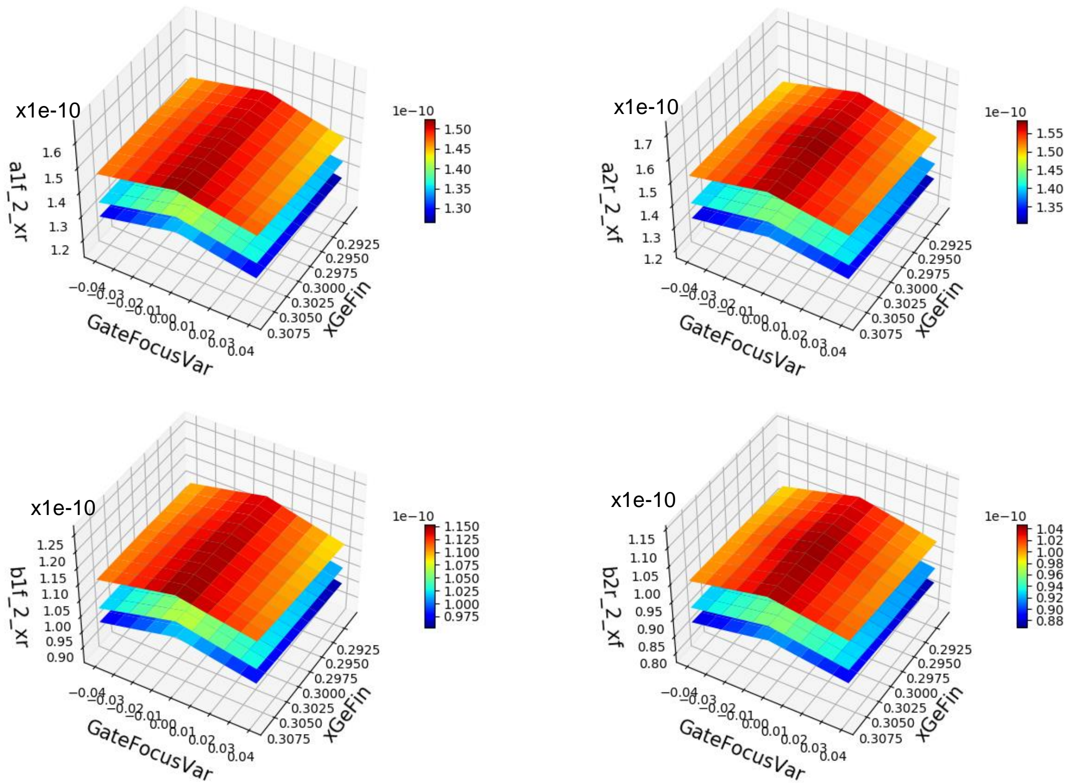


Figure 29: Measured delay time from HSPICE simulation results of the AOI221 cell including Mystic extracted models for device DoE and the extracted backend RC parasitics. (a1, a2, b1 and b2 are the 4 inputs ports, while x is the output port. 'r' refers to rising signal, 'f' refers to falling signal)

Using the RandomSpice model library generated from TCAD data, statistical circuit performance can be modelled using Monte Carlo circuit simulation, to investigate the impact of both statistical and global variations and the correlations between them at the circuit level. The results of MC simulation of the demonstrator AOI circuit are shown in Figure 30, where GV denotes that only global (i.e. process) variation is included, LV denotes that only local (i.e. statistical) variation is included, GV+LV means the combination of both variations are present. Here we assume each of the three process variation parameters follow a Gaussian distribution.

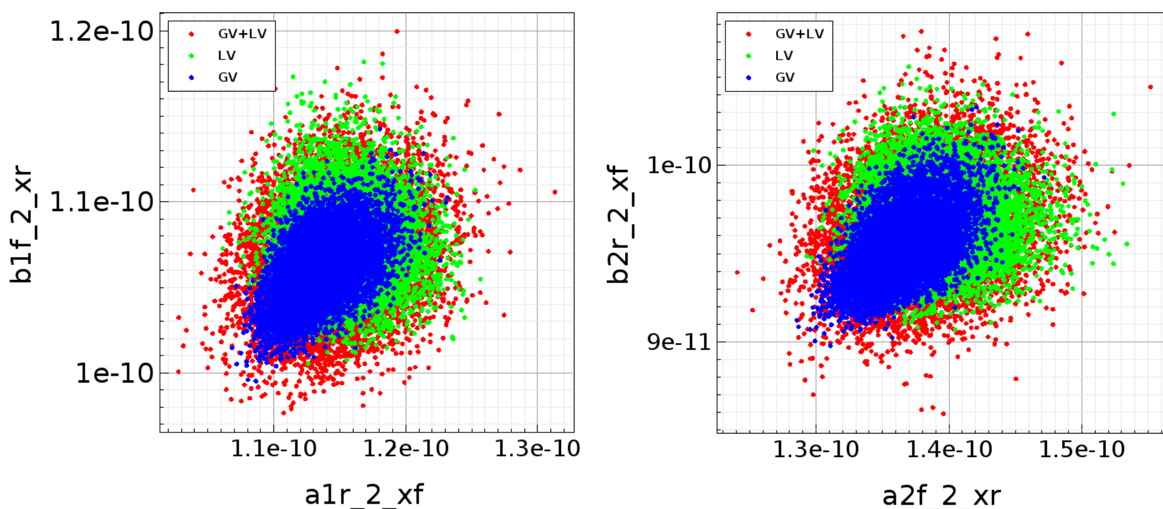
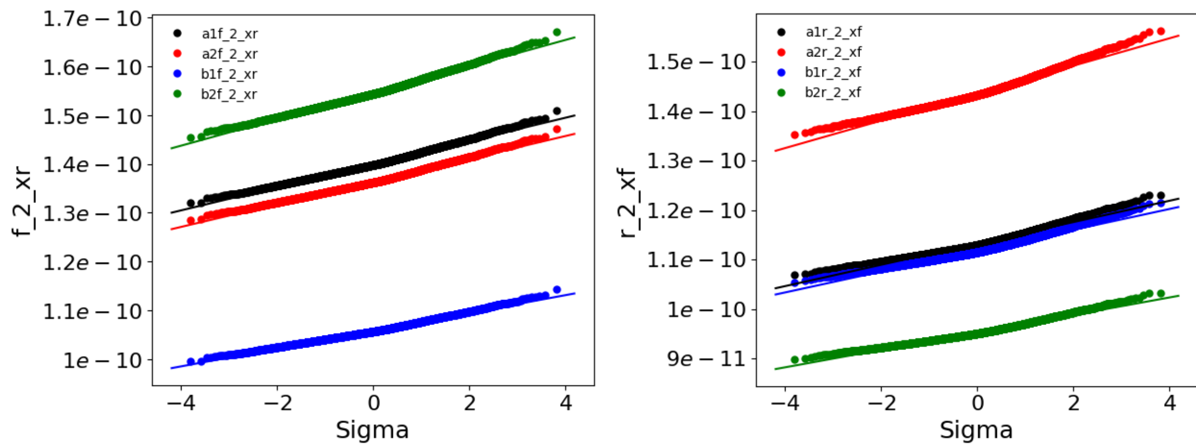
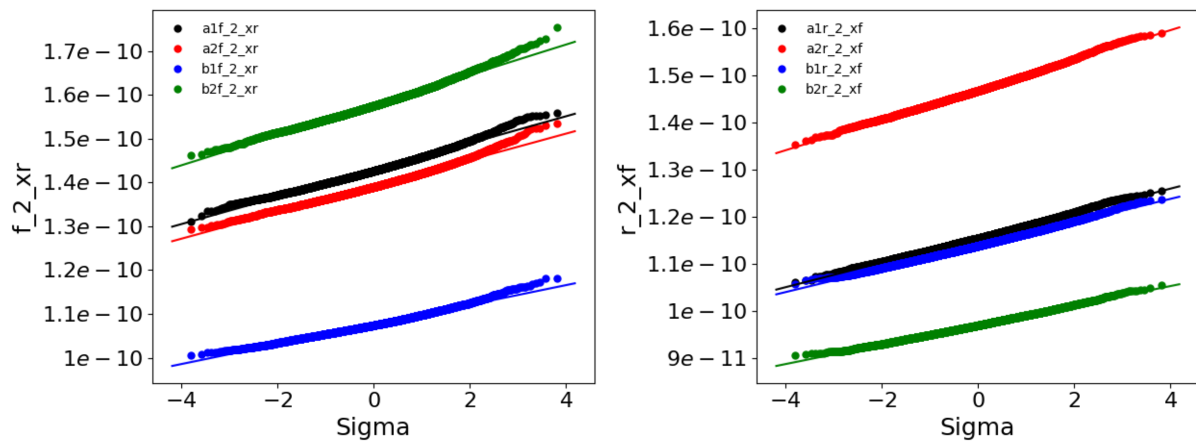


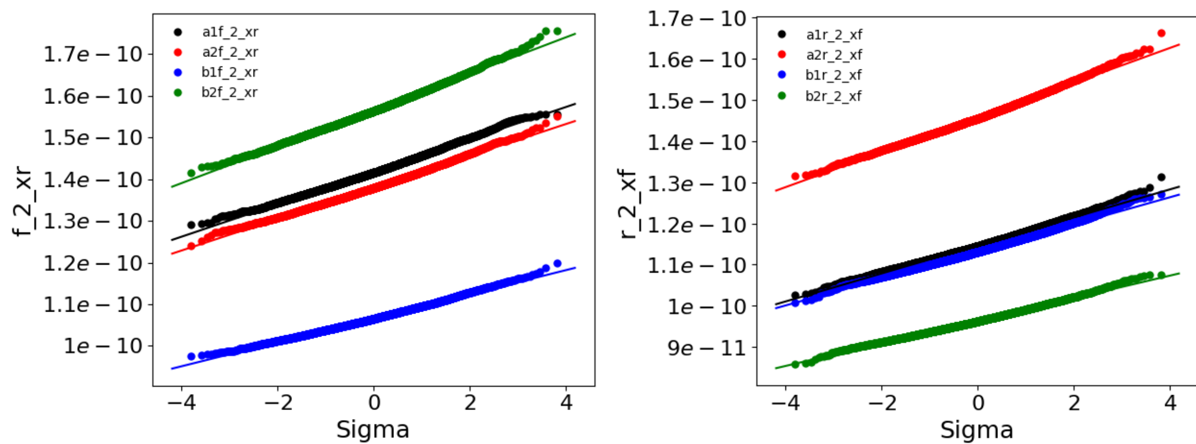
Figure 30: Example AOI signal timing simulation results produced using RandomSpice



(a) Distribution of delay time in the presence of global process variation (GV)



(b) Distribution of delay time in the presence of local statistical variation (LV)



(c) Distribution of delay time in the presence of both global and local variation (GV+LV)

Figure 31: Distributions of AOI propagation delays .

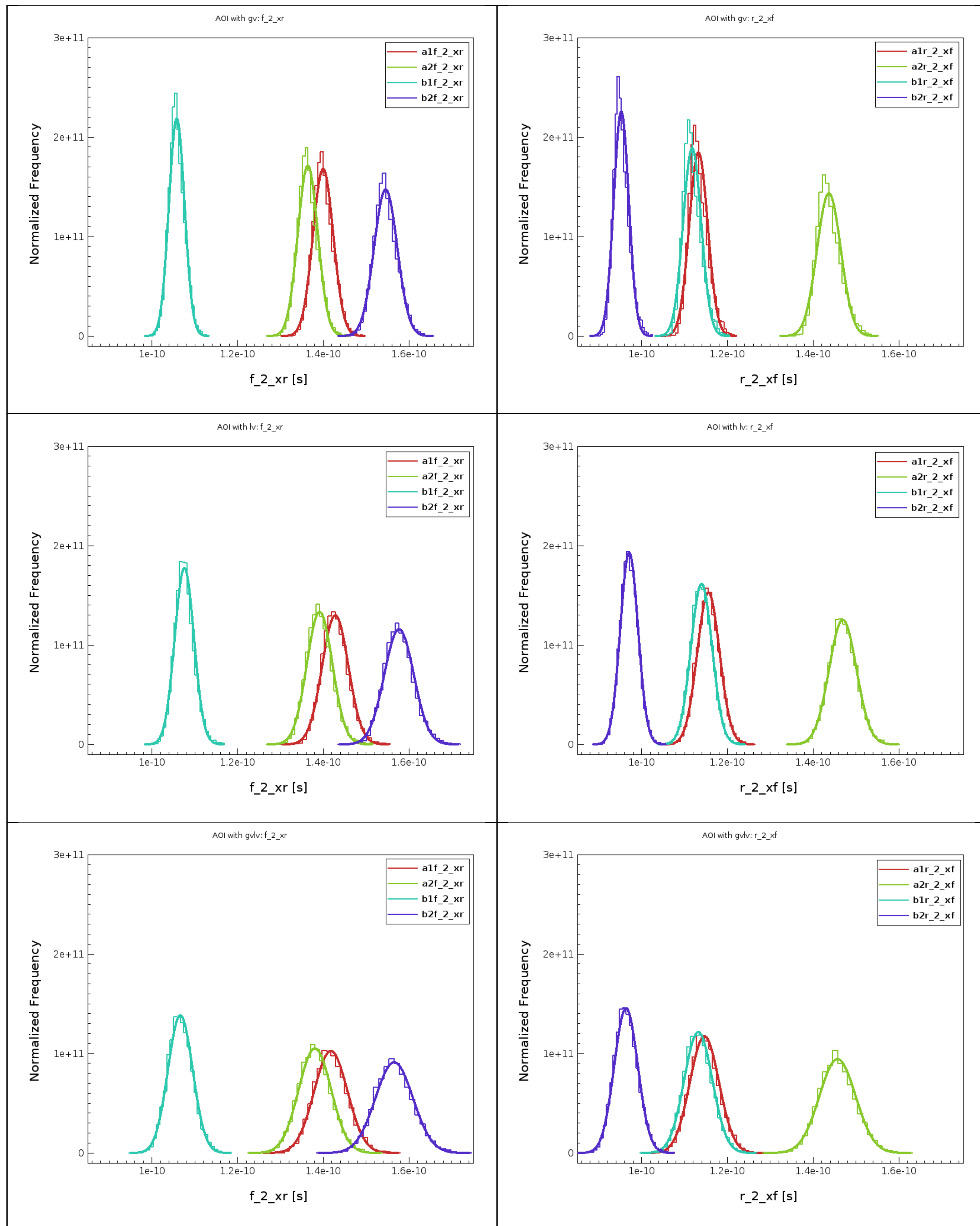


Figure 32: Signal timing histograms with fitted Gaussian distributions for AOI propagation delays in the presence of global process variation (top), local statistical variation (middle) and combined GV and LV (bottom).

By analysing the q-q plots of all delays (Figure 31), the fastest input triggering an output rise is from input B1, while the slowest input triggering an output rise is from input B2. For a falling output, the shortest delay is from input B2 and the longest is from A2.

Analysing the obtained delay histograms in Figure 32 leads to the conclusion that, when all of the worst-case transitions are taken into consideration that it is possible that the critical path which determines the maximum performance of the circuit may change when variability

is taken into account. When the impact of GV and LV are considered separately signal *b2f_2_xr* is consistently the worst-case transition, however, when we combine GV and LV there is a significant probability (~5%) that *a1f_2_xr* could be the worst-case transition, as evidenced by the overlapping distributions shown in Figure 32. As a result, it is critical to consider the combined impact of GV and LV when developing cell characterisation flows which feed into synthesis and static timing analysis (STA) for advanced technologies.

As a further demonstration of the capabilities provided by this SPICE modelling methodology, we can study the performance of Ring Oscillators (ROs) implemented by wiring the AOI so as to mimic digital logic delay chains. The performance of the ROs depends greatly on the way the ports of the AOI are connected. Two extreme cases can be set up by considering the best-case and worst-case critical paths. The wiring of the AOI based RO for each stage of these cases is illustrated in Figure 33.

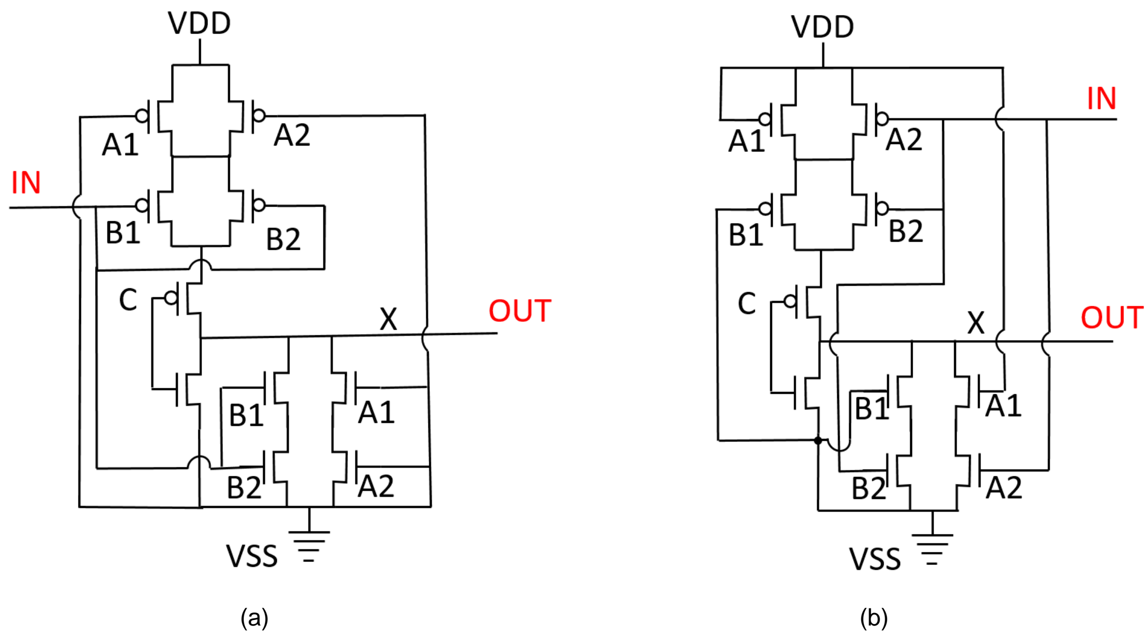


Figure 33: Schematics of the wiring of AOI for each stage of two extreme case ROs: (a) best-case (RO1) and (b) worst-case (RO2)

Two 11-stage ROs were simulated, and the impact of statistical variations, as well as the global variations from the process parameters, are shown in Figure 34. The results show that the equivalent “slow” and “fast” paths through an equal number of identical cells can be significantly different.

As GV dominates the behaviour of an RO circuit, we can use the DTCO framework to analyse the relative importance of the GV components modelled. Figure 35 demonstrates how the variations of different process parameters impact the performance of the RO implemented by AOI. As shown, *FinSpDepoFactor* variation mainly impacts the RO frequency, while the variation of *GateFocusVar* mainly impacts on the RO leakage. *xGeFin* variation has quite a small impact on RO performance, however, it contributes to the decorrelation between frequency and leakage. These results also show how the DTCO framework developed in the SUPERAID7 project can be used to identify the relative impact of both GV and LV, and can help to direct process improvement efforts to the aspects of variation where the biggest gains can be achieved, thus closing the feedback loop on design-technology co-optimisation.

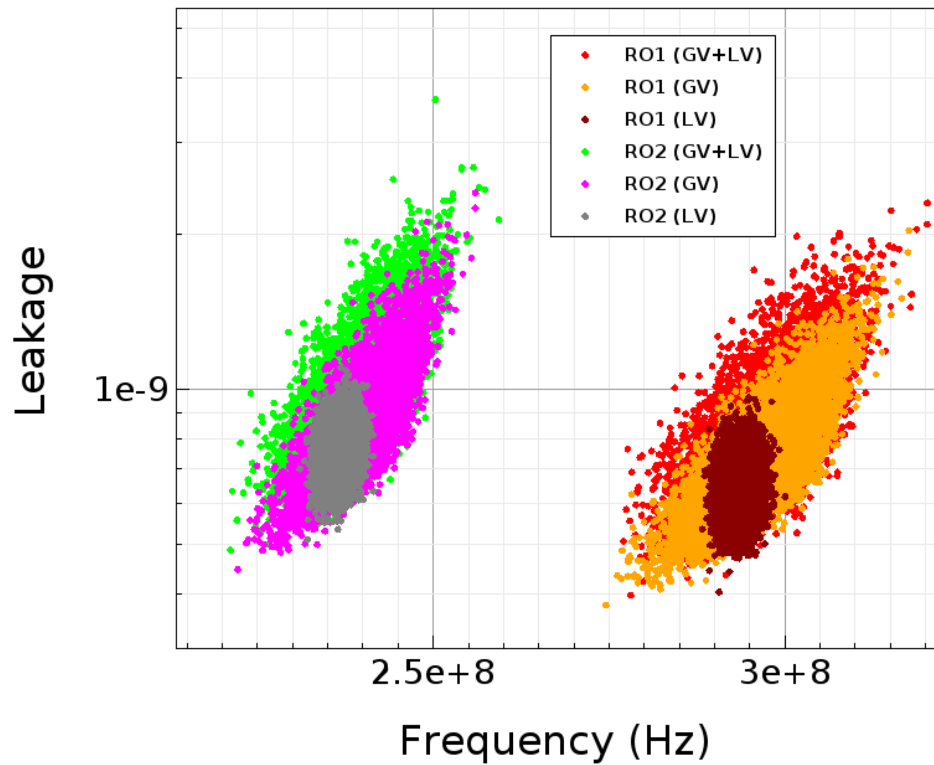


Figure 34: Leakage of two extreme case ROs, implemented by AOI. RO1 is the best-case version and RO2 is the worst case.

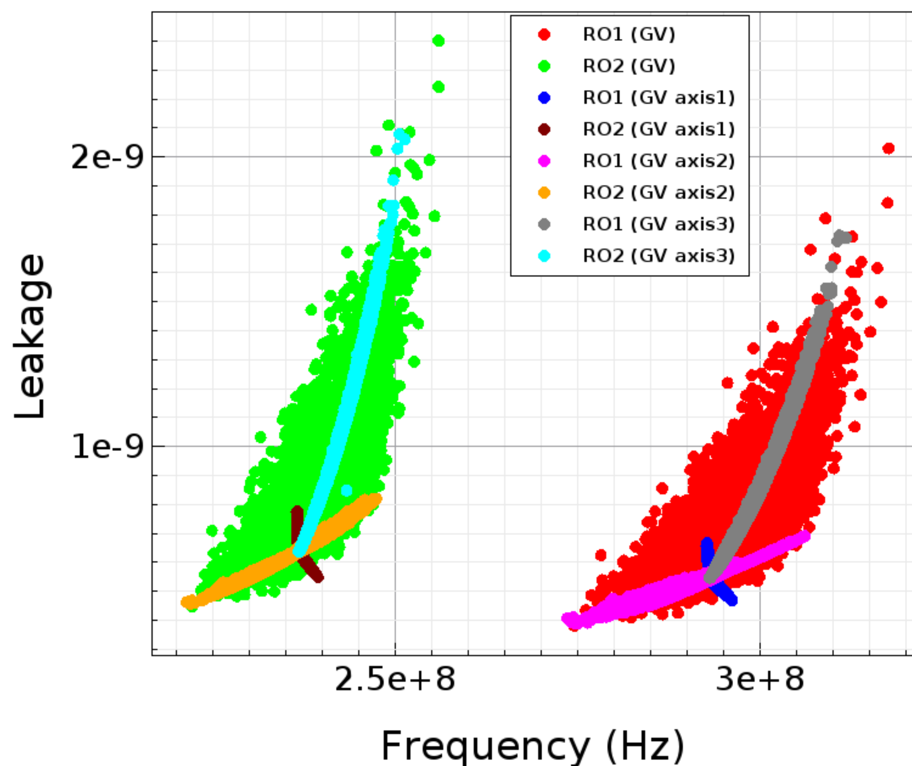


Figure 35: Variations introduced by different process parameters for the leakage of two extreme case ROs (GV axis1: xGeFin; GV axis2: FinSpDepoFactor; GV axis3: GateFocusVar) . RO1 is the best-case version and RO2 is the worst case.

11 Conclusions

Within SUPERAID7, a hierarchical software system has been developed to trace the impact of systematic and stochastic process variations from their sources, through device and interconnect performance to circuit behaviour. For this software system, both established commercial TCAD tools and specific simulation programs from project partners have been extended and combined to enable the investigation of highly three-dimensional nanoscale transistors and interconnects, and especially of their variations. The extended compact model extraction approach, and the new compact models developed, allow the study of the impact of variations on relevant circuits, as demonstrated in this deliverable for an AND-OR-Invertor cell and a Ring Oscillator.

The further use and prospects of the results obtained consist of three important elements: Most prominent, the extended overall compact model extraction and circuit simulation tools are being made available for application in leading-edge industry, as part of the TCAD-to-SPICE DTCO flow of the SUPERAID7 partner Synopsys. Second, the tools are being used by the partners themselves, especially by CEA/Leti and Fraunhofer IISB, for the further development and optimization of technologies, devices and circuits within their own research activities and within cooperative projects. Third, whereas the overall concept is versatile and can be applied to a large variety of technologies, devices and systems, dedicated application areas require the extension of existing models and software tools, and the development of new ones, for specific processes and new device architectures. Beyond that, the overall approach is not only important for advanced More Moore devices, like the nanowires investigated in the SUPERAID7 project, but for a wide range of device architectures, ranging from (analogue) More-than-More devices with somewhat-relaxed feature sizes to emerging Unconventional Nanoelectronics, where information is not stored as charges.

12 List of Abbreviations

3D: Three-Dimensional

A: Amps (unit measure for electrical currents)

AOI: AND-OR Invertor

F: Farads (unit measure for electrostatic capacitance)

FoM: Figure of merit

nm: nanometres (unit measure for length)

DoE: Design of Experiments

DD: Drift-Diffusion

DTCO: Design-Technology Co-Optimization

TCAD: Technology Computer Aided Design

DTCO: Design-Technology Co-Optimisation

RO: Ring Oscillator

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