This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688101.

ICT Project No 688101

SUPERAID7

Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

D6.2: Hierarchical Set of Presentation Foils and Leaflets for Use by SUPERAID7 Partners and Eventually by the EC Services – to be Updated until the End of the Project

	Name	Organisation	Date
Edited	Eberhard Bär	Fraunhofer IISB	May 16, 2018

Contents

Abstract

This deliverable comprises a project flyer and work package presentation slides for public use. The flyer is intended to be used in printed form. The slides can be used for presentations as well as for a printed handout.

1. Introduction

For disseminating the results of the project different channels are used, including the webpage, publications, and presentations at conferences or other events. In addition, a consolidated set of presentation foils and a project flyer have been prepared to support all project partners in advertising their own and the overall results of SUPERAID7. Furthermore, the material can be used by the EC services for displaying the objectives and results of the project.

2. Project Flyer

Our experience from various PR actions has shown that besides distributing material in electronic form, printed material is also well appreciated. For example, at events with face-to-face contacts it is appropriate to distribute printed material.

The goal of the project flyer, which is intended to be used mainly in printed form, is to draw attention to the project, its topics, and its results. For further information, the reader of the flyer should refer to the electronic sources such as those available at www.superaid7.eu. A 2-page flyer has therefore been considered appropriate and has been set up using appealing and eye-catching figures with results from the project.

The flyer is shown in the appendix of this deliverable.

The work package slides described in the next chapter have been designed in a way that they can also be used in printed form (with 2 slides printed per DIN A4 page) and in this way complement the printed project flyer.

3. Presentation Slides

For more detailed information about the project, work package slides for the technical work packages (WP2, WP3, WP4, WP5) and for WP1 (overview of the project) have been prepared. The slides are intended to be used to present the approach and results of the project to external parties, such as groups from academia or industry which might be interested in using the software developed within SUPERAID7. The slides can also be used in printed form, in particular together with the printed project flyer described in the previous section.

The slides will be updated continuously until the end of the project to allow the inclusion of the latest project results.

The slides are shown in the appendix of this deliverable.

Appendix

SUPERAID7 flyer

Presentation slides for

WP1: Project Management/Overview of the Project

WP2: Specifications and Benchmarks

WP3: Variation-aware Equipment and Process Simulation

WP4: Variation-aware Device and Interconnect Simulation

WP5: Software Integration and Variation-aware Compact Models

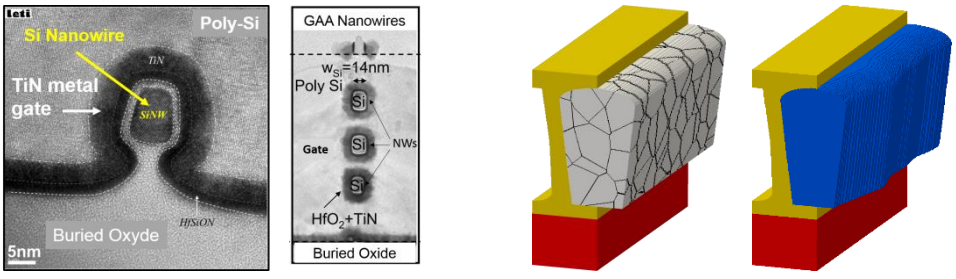
SUPERAID7 – STABILITY UNDER PROCESS VARIABILITY FOR ADVANCED INTERCONNECTS AND DEVICES BEYOND 7 NM NODE

Introduction

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled More Moore, process variability is getting ever more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Modelling and simulation (TCAD) offers the unique possibility to investigate the impact of process variations and trace their effects on subsequent process steps and on devices and circuits.

Within SUPERAID7 we:

- **establish a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits, down to the 7 nm node and below, including interconnects**
- **improve physical models and extend compact models**
- **study advanced device architectures such as tri-gate/Ω-gate nanowire transistors or stacked nanowires, including alternative channel materials**



(a) (b) (c) (d)

Examples for device architectures studied in the SUPERAID7 benchmarks
(a) Ω-gate nanowire transistor
(b) Stacked gate-all-around nanowires

Example for stochastic process variations which can introduce resistance variations in short range interconnects
(c) Copper granularity
(d) Line-edge roughness

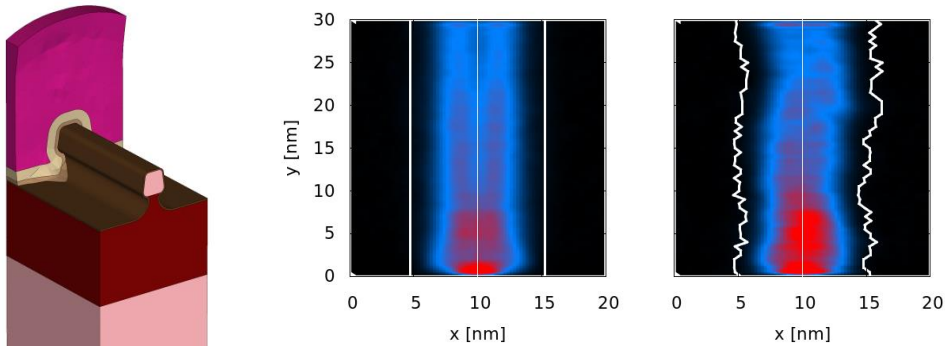
Work packages

The work package **"Specifications and Benchmarks"** is dedicated to the key features of the simulation system from the point of view of exploitation beyond the project. Specifications are defined for the 7 nm tri-gate and 5 nm stacked-nanowire technologies to be simulated. Morphological data and associated measured electrical characteristics for these devices are described in order to perform process and device simulations, and comparisons between experimental data and simulations are carried out.

In the work package **“Variation-aware Equipment and Process Simulation”** the work is focused on the integration of the topography modules from Fraunhofer IISB and TU Wien (lithography, etching, deposition) and on the development of physical models for topography steps. The latter is based on an analysis of the current capabilities of the modules and the resulting requirements for adaptations with respect to the SUPERAID7 benchmarks but also with respect to the needs of the simulation end-user community as a whole.

Within the work package **“Variation-aware Device and Interconnect Simulation”** a set of confined scattering models and a ballistic version of a non-equilibrium Green's function simulator have been developed. Ab-initio quantum simulations of surface roughness with realistic More-Moore device parameters obtained from CEA-Leti have been successfully completed. A prototype fast field solver has been developed that can be used to extract resistances and capacitances for advanced interconnect structures. This includes the capability to model global and statistical local variability due to line edge roughness and metal granularity.

The work package **“Software Integration and Variation-aware Compact Models”** focuses on the integration of the software modules for process, device, and interconnect simulation. Furthermore, compact models are developed, such as the predictive and physical compact model LETI-NSP for gate-all-around stacked nanowire/nanosheet MOSFETs.



(a) (b) (c)

(a) 3D process simulation of gate stack etching which is part of the sequence for the fabrication of the Ω-gate nanowire transistor shown in Figure (a) on the first page

Simulated electron density (red: high, blue: low) in ideal (b) and rough (c) wires: quantum repulsion keeps the density away from the boundaries

First results from SUPERAID7 have already been commercialized, including the integrated TCAD to SPICE DTCO (design technology co-optimization) flow made commercially available by Synopsys. Furthermore, the LETI-NSP compact model is being proposed for international standardization via the Compact Model Coalition (CMC) to allow the inclusion of LETI-NSP in all major ECAD (electronic computer-aided design) tools.

Partners

Fraunhofer IISB (Coordinator)
with Chair of Electron Devices, University of Erlangen-Nuremberg as Linked Third Party

Gold Standard Simulations, now part of Synopsys

CEA-Leti

University of Glasgow

TU Wien

Contact and further information

Dr. Jürgen Lorenz, Fraunhofer IISB (Project Manager)

www.superaid7.eu

This project has received funding from the European Union’s Horizon 2020 research and innovation program under grant agreement No. 688101.

SUPERAID7

Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

Project Manager: Jürgen Lorenz, Fraunhofer IISB

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www.superaid7.eu

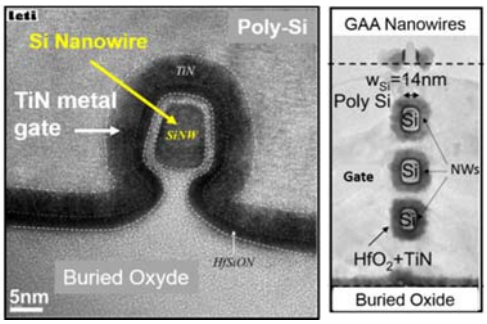
Contents

SUPERAID7
Objectives (1)

- Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled More Moore, process variability is getting ever more critical.
- Effects from various sources of process variations, both systematic and statistical, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits.
- Modelling and simulation (TCAD) offers the unique possibility to
  - investigate the impact of process variations,
  - trace their effects on subsequent process steps and on devices and circuits.
- Physical models developed for nominal processes also hold in case of variations => for the treatment of variations only extensions of the software are needed to allow one to handle large sets of simulations.

SUPERAID7
Objectives (2)

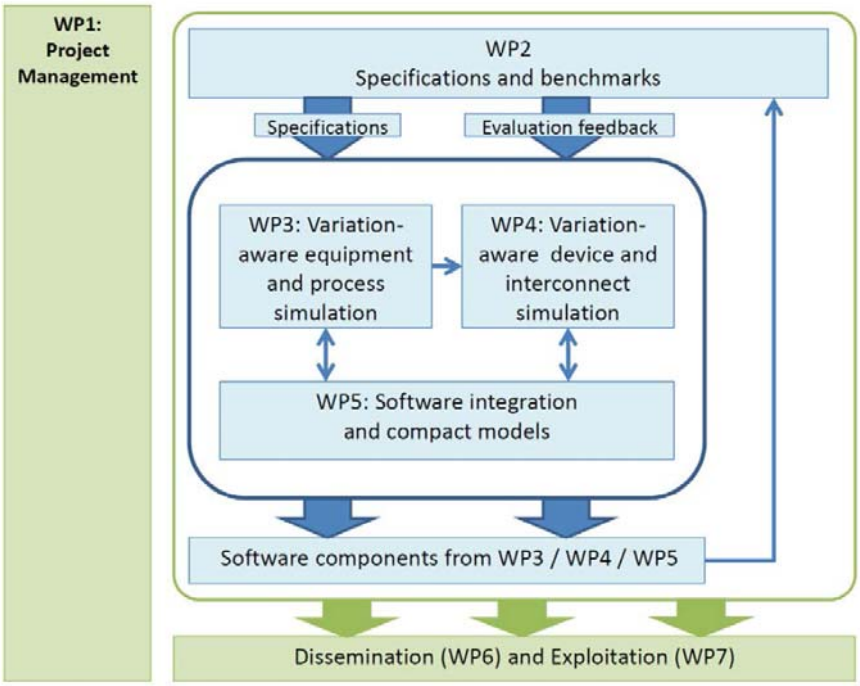
- Within SUPERAID7 we
  - establish a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits, down to the 7 nm node and below, including interconnects,
  - improve physical models and extend compact models,
  - study advanced device architectures such as TriGate/ΩGate FETs or stacked nanowires, including alternative channel materials.



SUPERAID7
Project Data and Partners

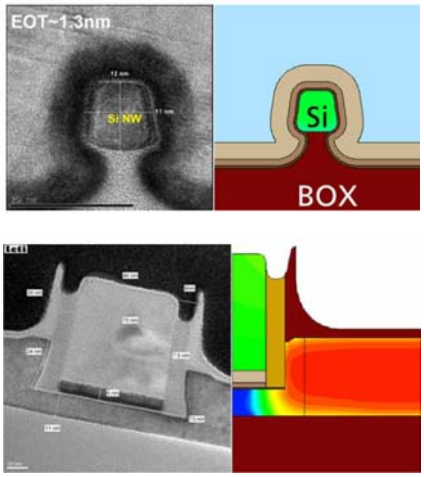
- Project period: 01/2016 – 12/2018
- EC funding: 3,377,527.50 EUR from Horizon Call ICT-25-2015 “Generic micro- and nano-electronic technologies“
- Partners
  - Fraunhofer IISB (Coordinator)
    with Chair of Electron Devices, University of Erlangen-Nuremberg
    as Linked Third Party
  - Gold Standard Simulations, now part of Synopsys
  - CEA-Leti
  - University of Glasgow
  - TU Wien

SUPERAID7
Project Structure



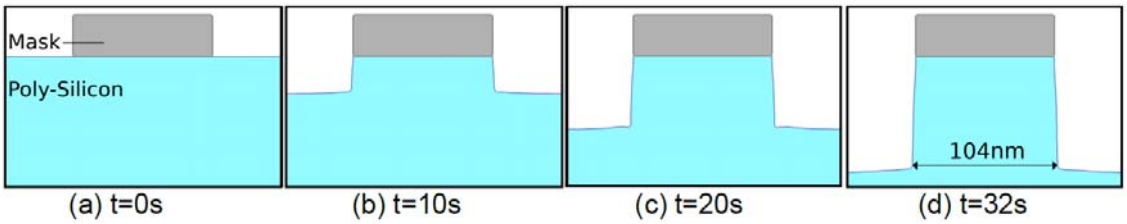
Examples from the Project, WP2
Comparison of Experiment and Simulation

- Specifications of software and benchmarks 1 and 2 finalized
- Relevant morphological and electrical data for benchmark 1 collected from background work
- Benchmark simulations carried out, using as far as possible software from the project
- Example: Comparison of experiment and simulation after
  - gate stack deposition (top)
  - hard mask removal (bottom)

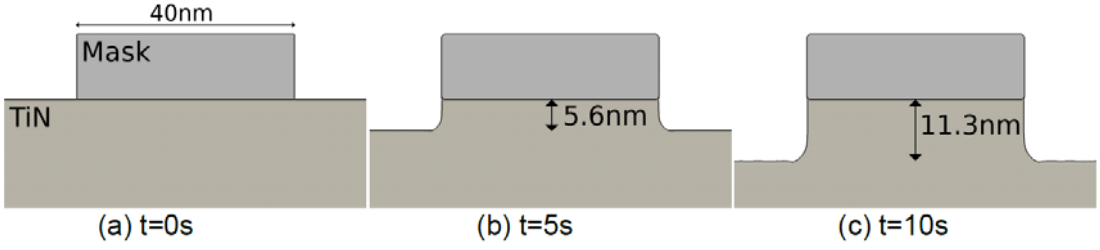


Examples from the Project, WP3
Simulation of Gate Stack Patterning (Poly-Silicon, TiN)

- Simulation of poly-silicon etching in a SF_6/CH_2F_2 plasma with a bias power set to 75 W and a SF_6 to CH_2F_2 ratio of 0.45:



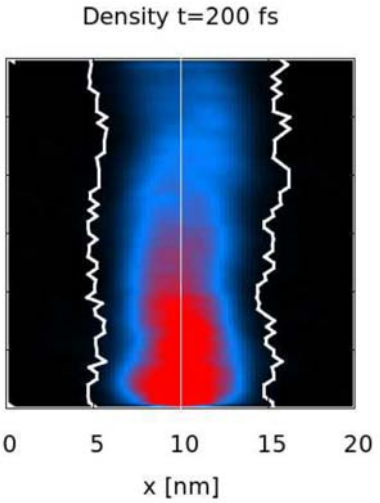
- Simulation of titanium nitride etching in a Cl_2/CH_4 plasma:



Examples from the Project, WP4

Quantum Wire Surface Roughness Variability

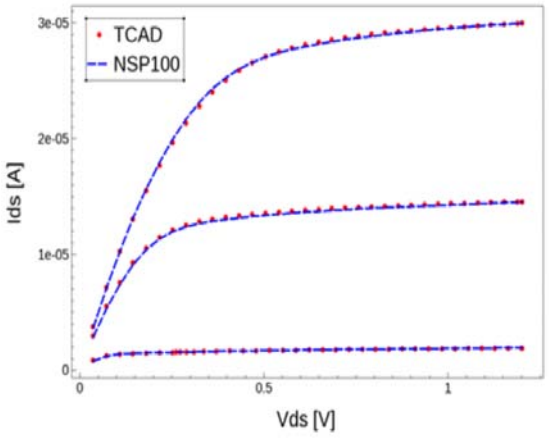
- Analysis of lithography induced variability in wire cross-section on electron transport via ab-initio Wigner simulations
  - Quantum simulations provide physical insight into the electron evolution process affected by the surface roughness
  - Interplay between quantum repulsion and penetration (tunneling) into the boundaries
  - Validate the assumptions of the 1D multi-subband surface roughness scattering model



Examples from the Project, WP5

New SPICE model LETI-NSP

- WP5: Integration between various internal tools for process, device and interconnect simulation; development of compact models
- New SPICE compact model LETI-NSP has been developed
- Compact model extraction demonstrated on 7 nm FinFET, with process simulation conducted by Fraunhofer and linked to experimental data from LETI
- The figure shows Ids-Vds characteristics from TCAD simulations compared to the LETI-NSP compact model (NSP 100)



Conclusions and Outlook

- Variability (systematic and statistical) is one of the most critical issues for further scaling of advanced CMOS devices.
- Hierarchical simulation from equipment to circuit level can and must contribute to technology/device development and yield optimization.
- SUPERAID7 provides key contributions to variability-aware design technology co-optimization (DTCO).
- First results from SUPERAID7 have already been commercialized, including the integrated TCAD to SPICE DTCO (design technology co-optimization) flow made commercially available by Synopsys.
- The LETI-NSP compact model is being proposed for international standardization via the Compact Model Coalition (CMC) to allow the inclusion of LETI-NSP in all major ECAD (electronic computer-aided design) tools.

Acknowledgement

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SUPERAID7

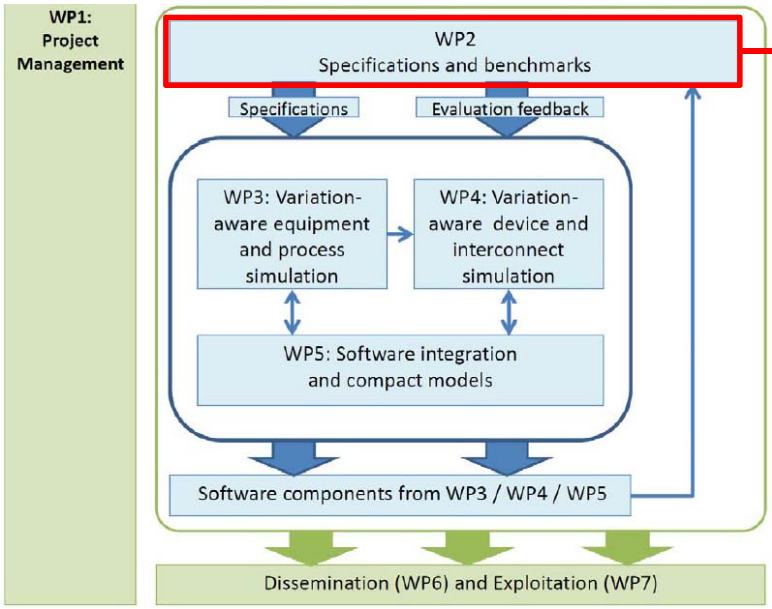
Work Package on Specifications and Benchmarks (WP2)

Work package coordinator: Sylvain Barraud, CEA-LETI

sylvain.barraud@cea.fr

Contents

Link to Other Work-Packages



WP2

- Provide input data to WP3/WP4/WP5
- Feedback to other WPs after the comparison between experiment and simulation

WP2 Partners

leti ceatech

GSS

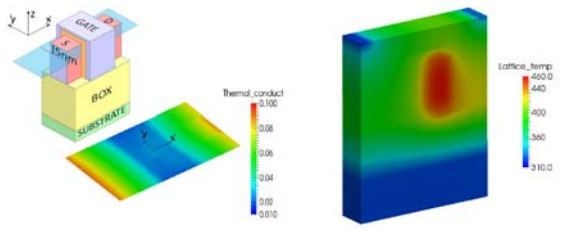
Fraunhofer IISB

Objectives

- Software and Device **Specifications**
  - To specify the requirements to be met by process/device/interconnect simulation to address **7-5 nm technological nodes**
  - Two generations of process architectures and related process flows will be considered (**Trigate** for 7 nm node and **Stacked-Nanowires** for 5 nm node).
  - To provide morphological and electrical results to WP3 and WP4 for the validation of process/device simulation
- **Benchmark** the Software System Developed in SUPERAID7
  - Comparison between experiment and simulation
  - Impact of systematic and statistical process variation

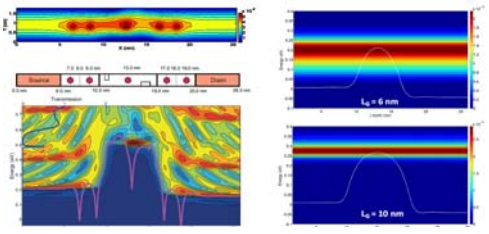
Key Physical Models Needed for Advanced Devices

Self-heating, random discrete dopants (RDD), line edge roughness (LER) and metal gate granularity (MGG) are significant concerns in terms of device scaling and circuit yield.



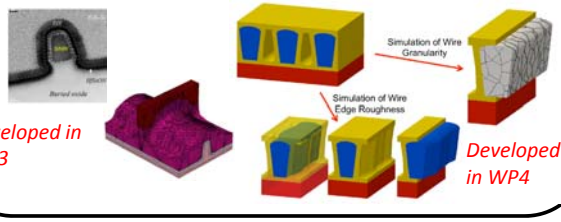
Developed in WP4

Advanced MOSFET architectures (Trigate/stacked-NWs) required quantum transport models to account for quantization effects and S/D tunneling current.
- Tight-binding approach (band structure calculation)
- Wigner/NEGF transport



Developed in WP4

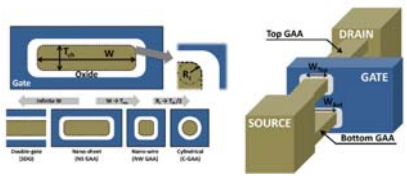
Advanced simulation of interconnect and device structures
- RC extraction in the presence of statistical variability (line edge roughness, metal granularity, …)
- Influence of real topography on device behavior
→ Interfaces of WP3 tools to GSS device simulation



Developed in WP3

Developed in WP4

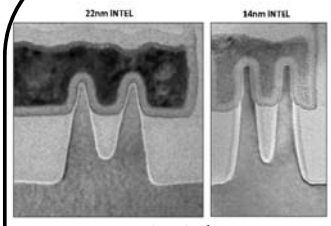
Compact model for advanced devices (stacked-NWs): quantum confinement, arbitrary NW shape, mobility model,…



Developed in WP5

Key Device Characteristics – 1st Generation of Devices

Trigate FETs

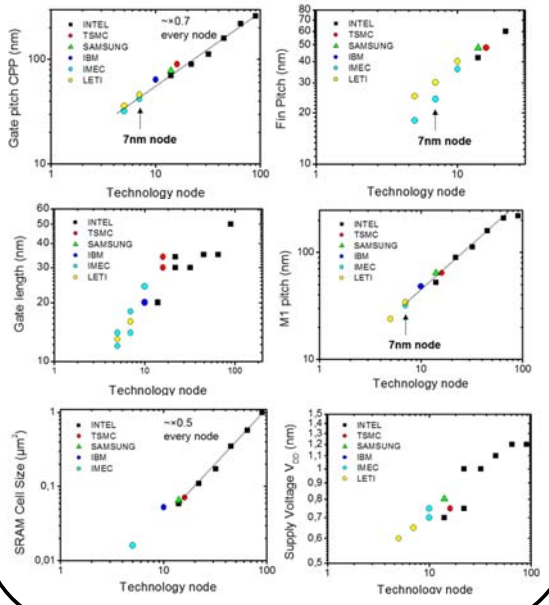


Fin pitch

- Fin pitch
- Gate length
- Metal pitch
- Gate pitch
- Supply voltage
- SRAM cell size
- EOT

• Fin pitch can basically minimize the cell capacitance and/or maximize the drive current (FP<40nm and a Fin width~7nm are expected)
• Unmerged Fins can increase access resistance and decrease drive current. But, a loss in drive current due to smaller Fin pitch can be recovered with a reduction of capacitance
• A Contacted Poly Pitch of around 46nm is expected at 7nm node (additional challenges on the gate length, spacer size and contact size).

Evolution of key design rules down to 7nm node



A database has been built from publications of INTEL, TSMC, SAMSUNG and IBM
For sub-10nm, the data come from LETI and IMEC (simulation results)

Specifications of Device and Process Assumptions

1st generation of device (Trigate) for 7 nm node

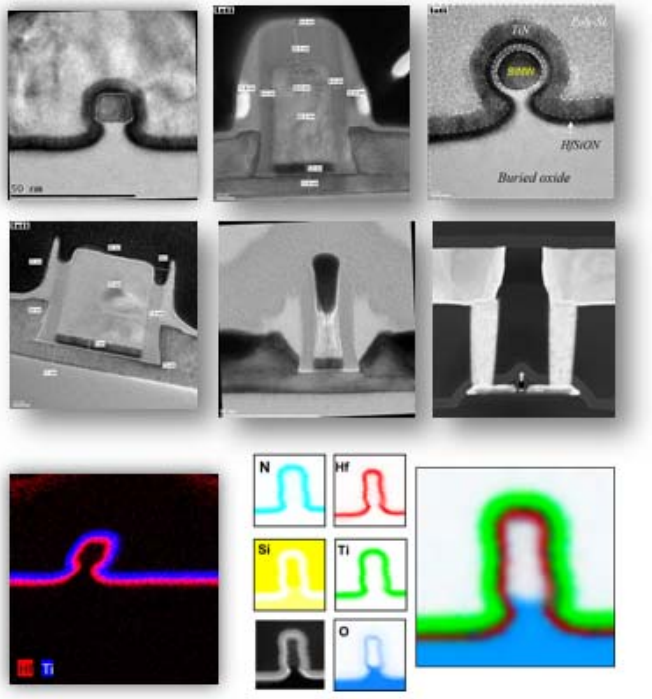
- Replacement-Metal-Gate (RMG)
- Fin runs along one [110] direction
- In-situ doped thin merged epi for both nFET and pFET.

Key items	Definition (unit, um)	Comments
Substrate	Bulk standard	Top/bottom (100) and sidewall (110) – Transport along the [110] direction
Fin patterning	EUV (or multiple patterning)	
Fin pitch	30nm	Single-Fin for SRAM
Fin width	7nm	
Fin height	42nm	
CPP	46nm	
L_G nominal	16nm	
Spacer	6nm	
Epitaxy	Merged	Si:P / SiGe:B
Gate stack	RMG	Encapsulated by dielectric for SAC
MEOL	SAC	
Lithography	193i or EUV	

→ Specifications of device and process assumptions have been delivered to WP3 and WP4 for the process and device simulation

Trigate Process Flow

- SOI substrates (BOX 145nm)
- Active patterning: Mesa
- Gate stack (**HK/MG**) and patterning
- Spacer 1
- Raised source/drain
- Extension N/P implant and anneal
- Spacer 2
- HDD implant N/P and anneal
- CESL/Contact & Back-End

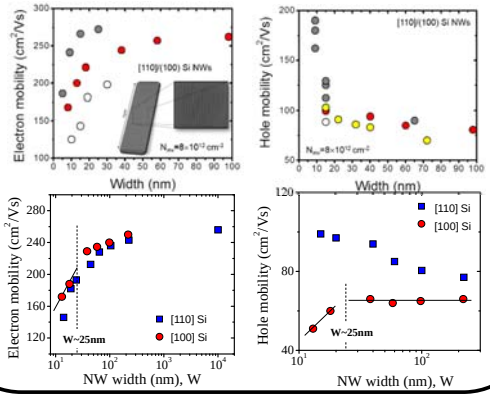


→ Data provided to WP3

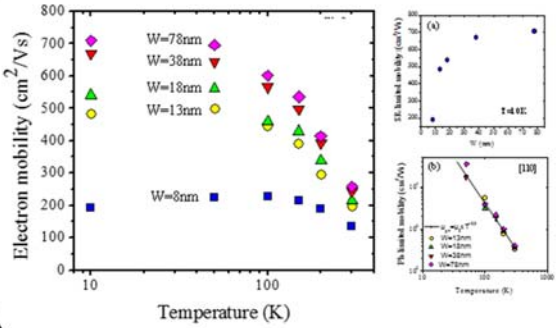
SUPERAID 7

Long-channel Mobility in Trigate MOSFET Architectures

Room-temperature characterization



Low-temperature characterization



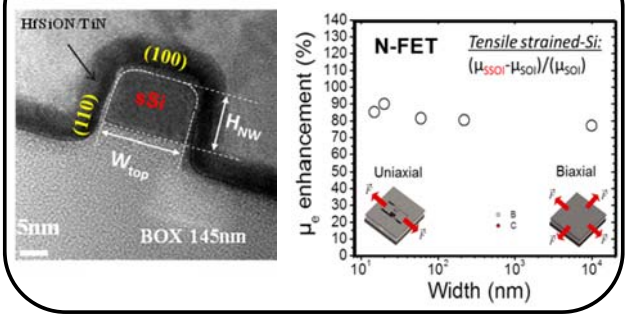
- Electron and hole mobility *vs* inversion charge are extracted for different nanowire widths.
  - Sidewall conduction and quantum confinement effects
- Carrier mobility was measured for different transport orientations ([110] and [100] nanowire FETs)
  - Evidence of sidewall conduction of quantum confinement effects
- Low-temperature measurements were performed to investigate the scattering mechanisms
  - Phonon and surface-roughness limited mobility down to 10 K
- **Advanced simulation tools developed in WP4 can be validated on experimental data**

→ Data provided to WP4

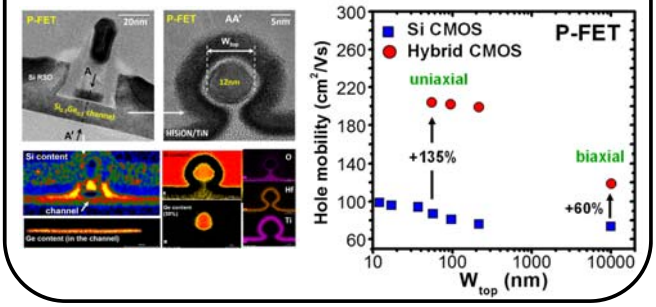
SUPERAID 7

Long-channel Mobility in Trigate MOSFET Architectures

Tensile strain for N-FET



Compressive strain for P-FET

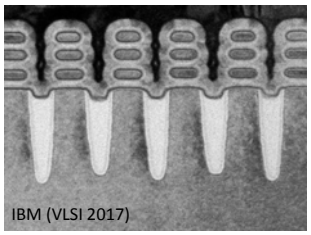


- Carrier mobility measured in tensile strained-SOI nanowires
  - Effect of nanowire width (10nm<W<10µm)
- Hole mobility measured in compressive SiGe nanowires
- Short-channel performance have been studied

→ **Data provided to WP4**

Key Device Characteristics: 2nd Generation of Device

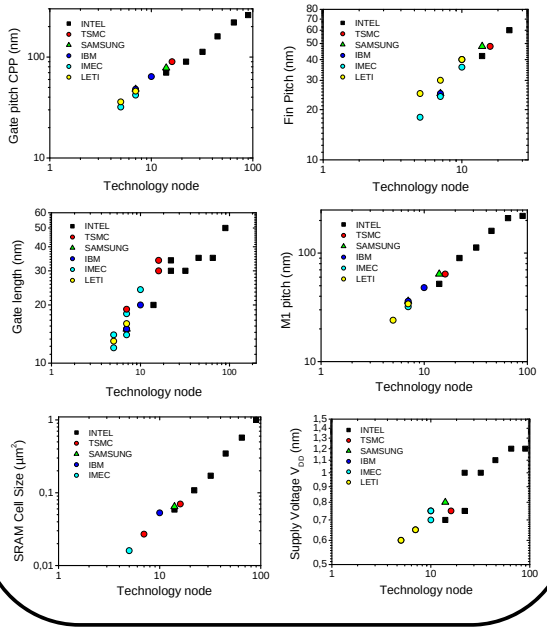
GAA stacked-NW FETs



- The Fin pitch
- The gate length
- The metal pitch
- The gate pitch
- The supply voltage
- The SRAM cell size
- The EOT

• Fin pitch can basically minimize the cell capacitance and/or maximize the drive current
• Unmerged Fins can increase access resistance and decrease drive current. But, a loss in drive current due to smaller Fin pitch can be recovered with a reduction of capacitance
• A Contacted Poly Pitch of around 36nm is expected at 5nm node (additional challenges on the gate length, spacer size and contact size).

Evolution of key design rules down to 5nm node



A database has been built from publications of INTEL, TSMC, SAMSUNG and IBM [refs in D2.4]
For sub-7nm, the data come from LETI and IMEC (simulation results)

Specifications of Device and Process Assumptions

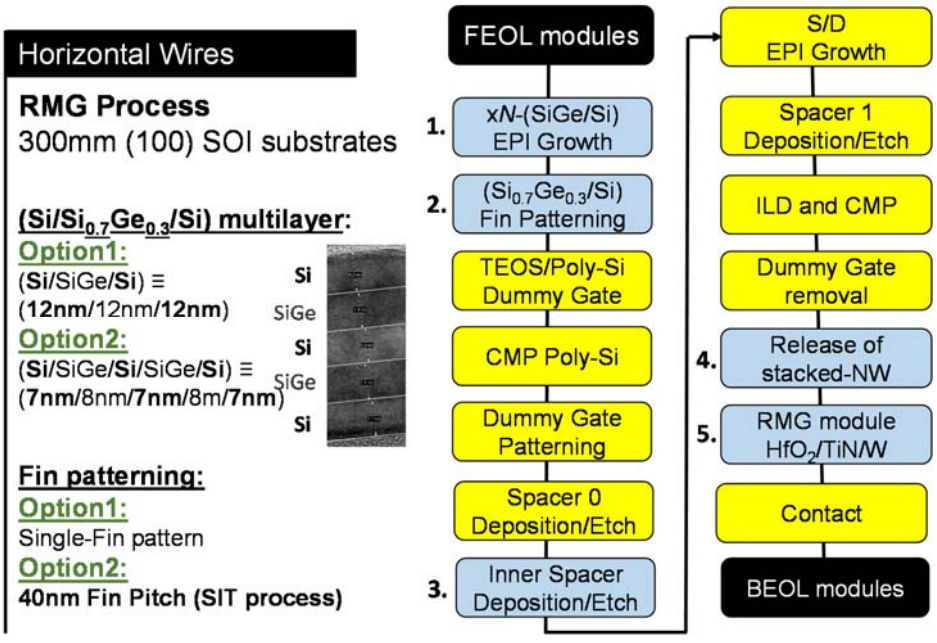
2nd generation of device (GAA stacked-Nanowires) for 5nm node

- Replacement-Metal-Gate (RMG)
- (SiGe/Si) Fins run along one [110] direction
- In-situ doped merged epi for both nFET and pFET.

Key items	Definition (unit, um)	Comments
Substrate	Bulk standard	Top/bottom (100) and sidewall (110) – Transport along the [110] direction
Fin patterning	Multiple patterning or EUV	
Fin pitch	20nm	Single-Fin for SRAM
Fin width	Depend on nanowires/nanosheets	
Fin height	Total thickness similar to trigate	
CPP	36nm	
L_G nominal	13nm	
Spacer	4nm	
Epitaxy	Merged	Si:P / SiGe:B
Gate stack	RMG	Encapsulated by dielectric for SAC
MEOL	SAC	
Lithography	193i or/and EUV (depend on critical levels)	

→ Specifications of device and process assumptions have been delivered to WP3 and WP4 for the process and device simulation (details given in D2.4)

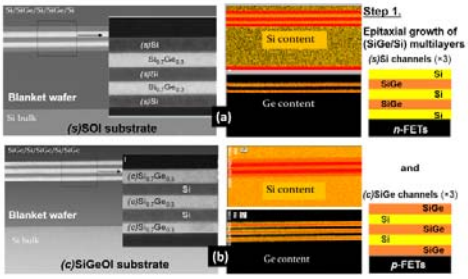
Stacked-Nanowires Process Flow (LETI)



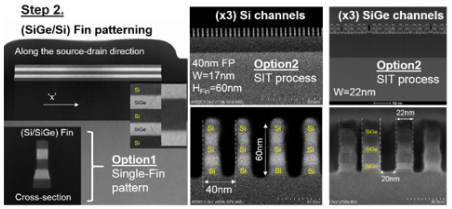
Inner spacers and SiGe:B raised-S/D are used. The Ge concentration in the SiGe layers is around 30%. The steps numbered '**1**' to '**5**' are specific technical requirements for stacked wires FETs (as compared to FinFET devices)

→ Data provided to WP3

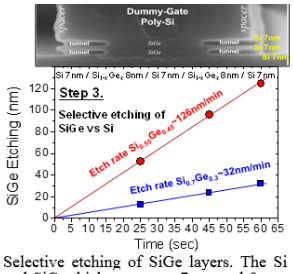
Morphological Data Extracted at Different Process Steps



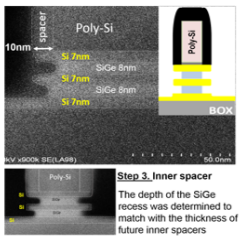
TEM images and EDX spectroscopy maps of (Si/SiGe) superlattices with **(a)** ×3 levels of tensile strained Si layers (for *n*-FETs) and **(b)** ×3 levels of compressive strained SiGe layers (for *p*-FETs) stacked upon one another.



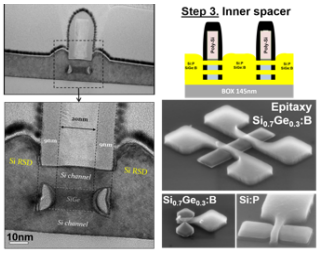
Cross-sectional TEM images after etching of (Si/SiGe) fins in the longitudinal and transverse directions of futures Si (or SiGe) wires). Two types of fins patterning were used: **(Left)** single-Fin process and **(Right)** dense arrays of fins with a SIT process. Our SIT-based patterning technique yields 40 nm-pitch fins which are 60 nm high and 20 nm wide for both Si and SiGe channels.



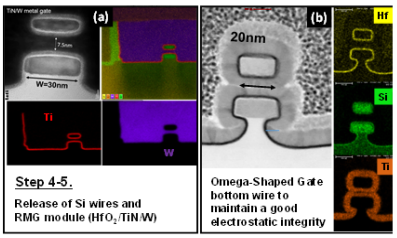
Selective etching of SiGe layers. The Si and SiGe thicknesses are 7 nm and 8 nm, respectively. **(Top)** Cross-sectional SEM image showing the etch depth profile realized before the integration of inner spacers. **(Bottom)** SiGe etch depth *versus* time for 30% and 45% of Ge.



Cross-sectional SEM images of stacked-NWs FETs prior to SiN inner spacers integration. The Si and SiGe thicknesses are 7 nm and 8 nm, respectively. The etching of SiGe layers stops at the same 'x' position than the spacer/poly-Si dummy gate interface.



(Left) Cross-sectional TEM images of stacked-NWs FET after the integration of inner spacers. The Si and SiGe thicknesses are 12 nm. **(Right)** 3D SEM images of stacked-NWs FETs after the source-drain epitaxy ($Si_{0.7}Ge_{0.3}$:B for *p*-FETs and Si:P for *n*-FETs). Inner spacers are well-aligned and correctly dimensioned.

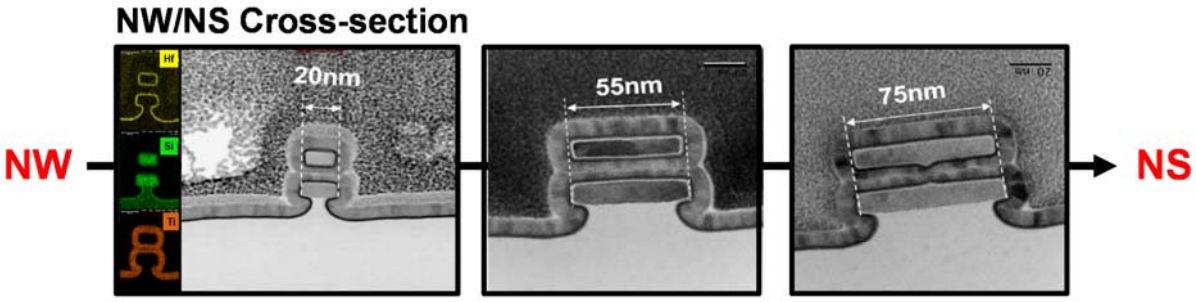


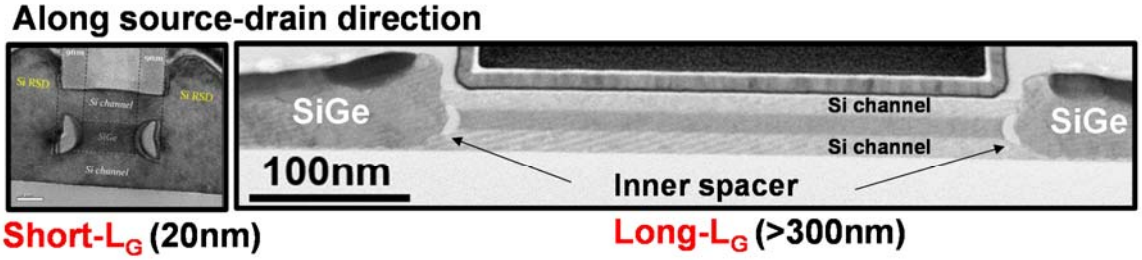
(a) Cross-sectional TEM images and EDX maps of stacked wires FETs (HfO_2, TiN and W gate stack). Wire widths above 20 nm are used to improve the effective width W_{eff} and then enhance the drive current. An Ω-Gate Si channel is used for the bottom wire **(b)** to maintain a good electrostatic integrity. The deposition of high-k dielectrics (HfO_2) and metals (TiN/W) is conformal.

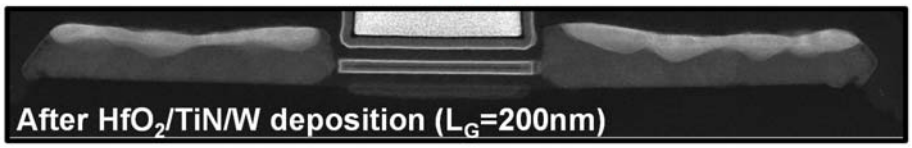
→ Data provided to WP3

SUPERAID 7

Morphological Data Extracted at Different Process Steps





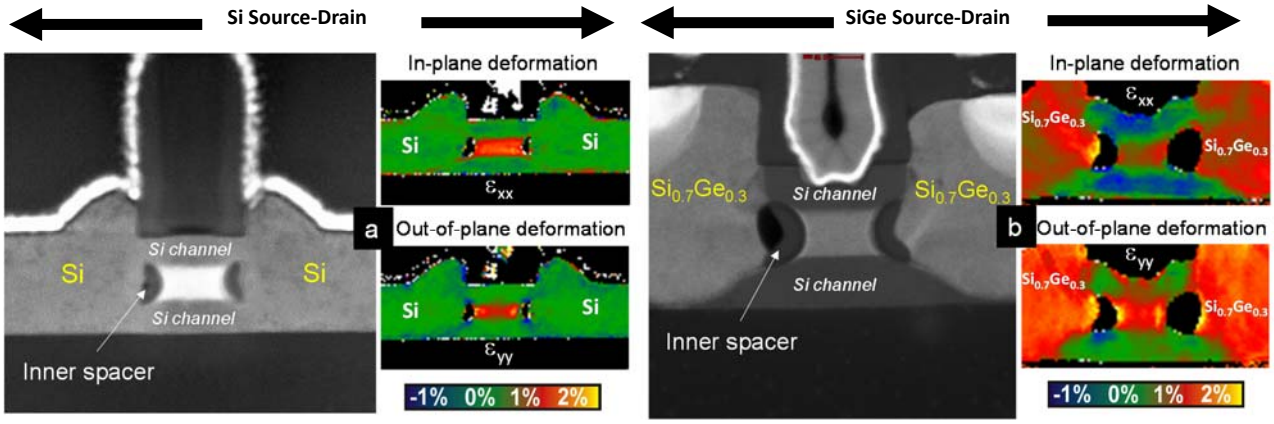


→ Data provided to WP3

SUPERAID 7

Strain Characterization at Different Process Steps

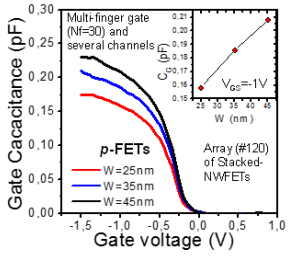
Strain maps at different process-step: (Si/SiGe) multi-layers, Fin patterning, S/D epitaxy, …



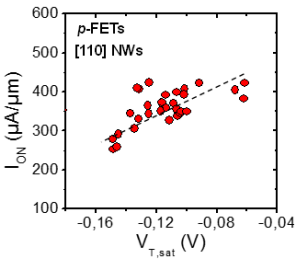
HAADF STEM images of stacked-NWs *p*-FETs and deformation maps acquired by PED in the (e_{xx}) and (e_{yy}) directions. A spatial resolution of about 1.5 nm is achieved. Strain is measured **after Si (a)** and **$Si_{0.7}Ge_{0.3}$:B (b) S/D epitaxy**. For Si S/D, no strain is generated into Si *p*-channels. However, recessed and epitaxially regrown $Si_{0.7}Ge_{0.3}$:B S/D junctions clearly inject a significant amount of compressive strain in top and bottom Si *p*-channels. A compressive strain close to [0.5-1%] (in blue color) is clearly visible.

→ Data provided to WP3

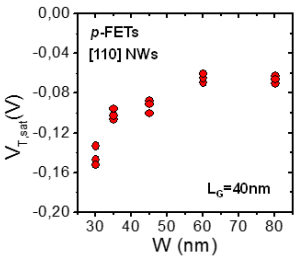
Electrical Characteristics Measurements



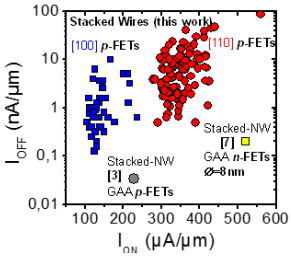
Gate capacitance *vs* V_{GS} for stacked-NWs *p*-FETs with W=25-45nm. Here, L_G=500nm.



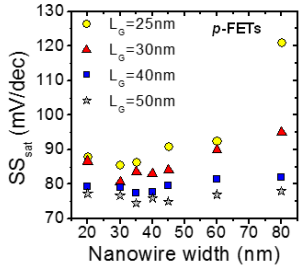
I_{ON} *vs* $V_{T,sat}$ for stacked-NWs *p*-FETs with W=25-35nm at V_{DD}=0.9V. 25nm<L_G<70nm.



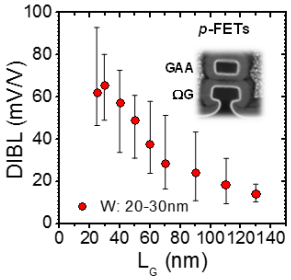
$V_{T,sat}$ *vs* W for stacked-NWs *p*-FETs with L_G=40nm at V_{DD}=0.9V.



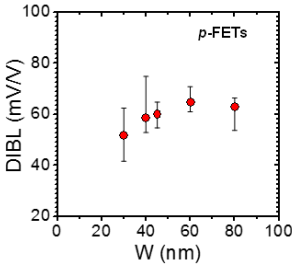
I_{ON}/I_{OFF} plot of [100] and [110] stacked-NWs *p*-FETs with W=20nm-30nm at V_{DD}=0.9V.



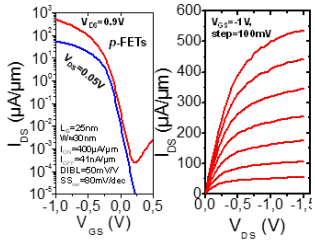
Subthreshold slope *vs* wire width (W) for stacked-NWs *p*-FETs with 25nm≤L_G≤50nm.



Median DIBL *vs* gate length (L_G) for stacked-NWs *p*-FETs with W=20nm-30nm.



Median DIBL *vs* nanowire width (W) for stacked-NWs *p*-FETs with L_G=40nm.



I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of stacked-NWs *p*-FETs with L_G=25nm. Here, W~30nm.

→ Data provided to WP4

Conclusions and Outlook

- **Software and device specifications are fully defined for both generations of devices** (Trigate and GAA Stacked-Nanowire/Nanosheet FETs).
- **Process-flow data and electrical device characteristics have been delivered to WP3 and WP4** for the validation of process and device simulations.

- **Outlook**
  - Comparison between simulations and experiments for 2nd generation of devices (GAA Stacked-Nanowire FETs – 5 nm node)

SUPERAID7

Work Package on Variation-aware Equipment and Process Simulation

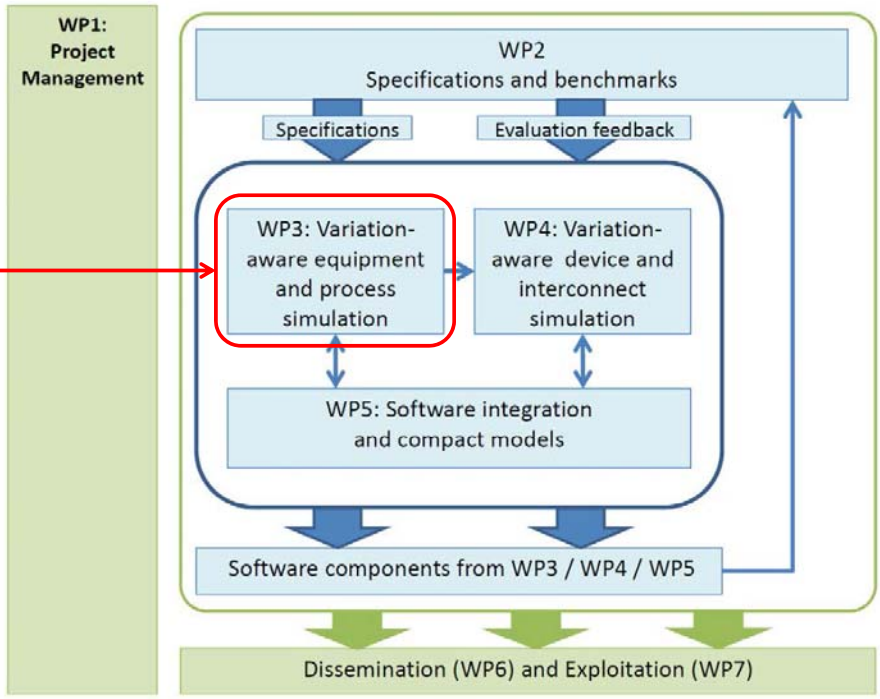
Work package coordinator: Eberhard Baer, Fraunhofer IISB

eberhard.baer@iisb.fraunhofer.de

Contents

Work Package on Variation-aware Equipment and Process Simulation in the Context of the Project

WP3



Variation-aware Equipment and Process Simulation

Partners

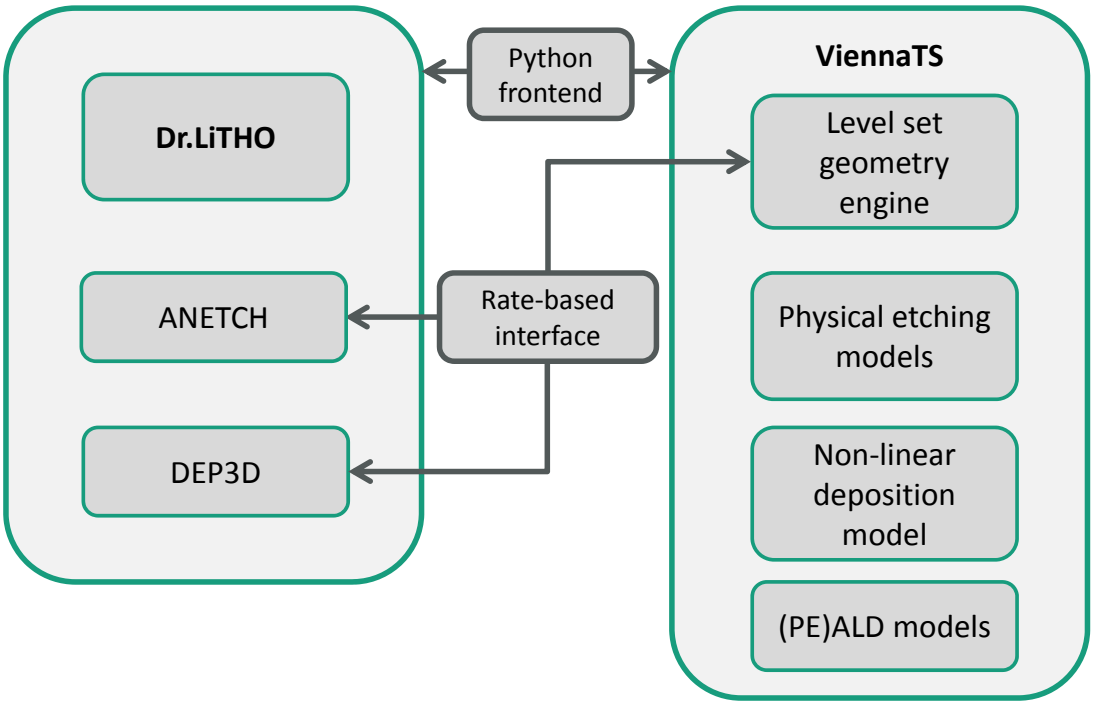
Fraunhofer IISB

TU WIEN

Variation-aware Equipment and Process Simulation
Objectives

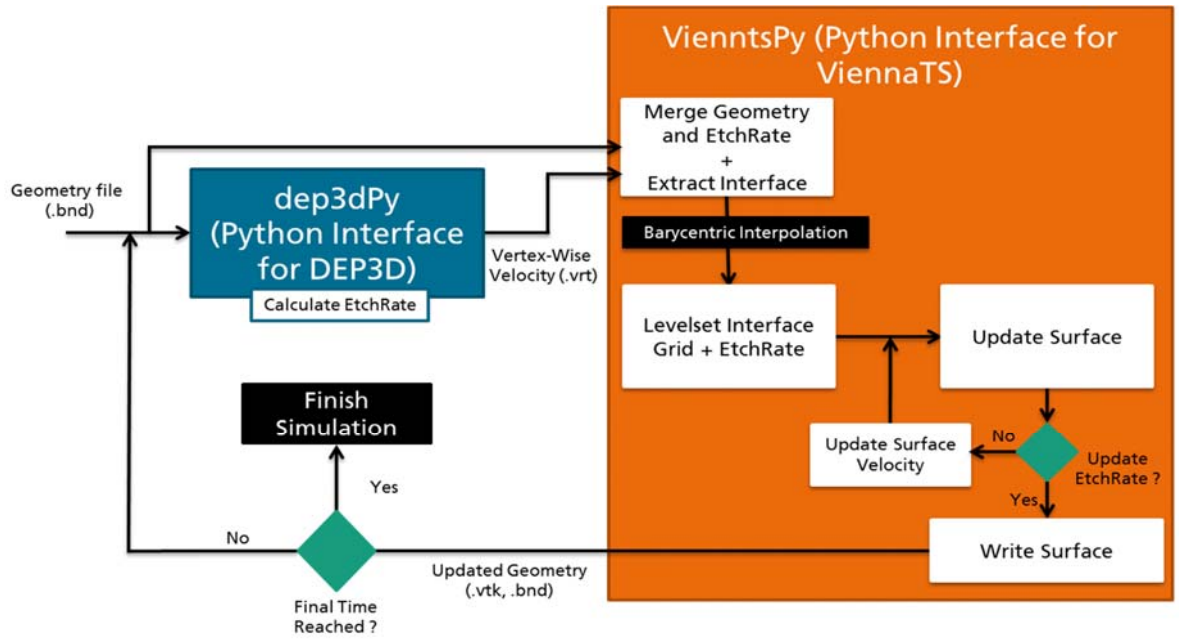
- Tight integration of the etching and deposition modules (DEP3D, ANETCH of Fraunhofer and ViennaTS of TU Wien) with background work on lithography simulation (using Dr.LiTHO of Fraunhofer) providing a unified frontend for topography simulation
- Development of physical models for etching and deposition processes relevant for device and interconnect fabrication
- Interfacing of feature-scale simulation with external equipment simulation modules
- Integration of the topography modules with further process steps and device and interconnect simulation
- Model calibration, verification, and benchmark support

Software Integration
Topography Simulation Modules and their Interaction



Software Integration

Example: Integration of DEP3D from IISB with ViennaTS

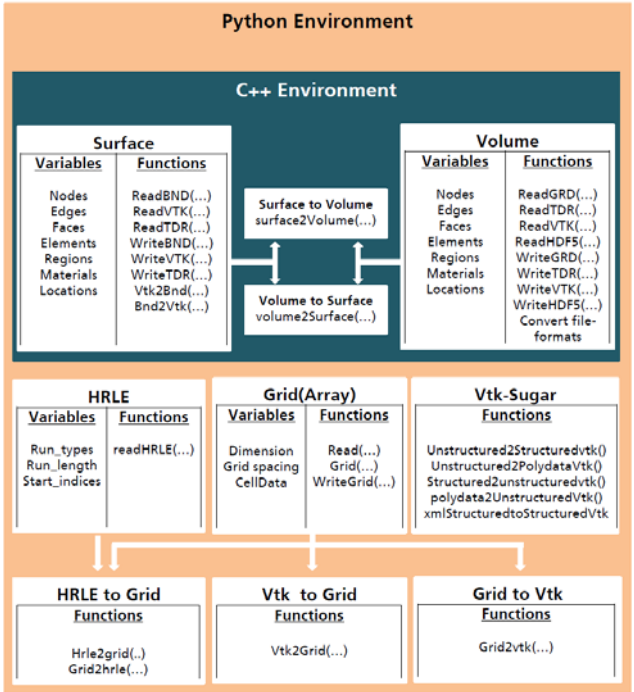


Software Integration

Example: Geometry Engine Python Package

Package supports:

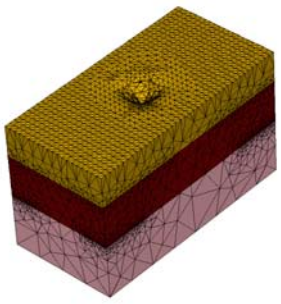
- Different geometry representations (surface and volume) of arbitrary 3D structures (without bulk data such as doping)
- Different formats, including SNPS TDR and open formats such as VTK
- Conversion between formats
- Different operations, such as extraction of surface mesh from volume mesh



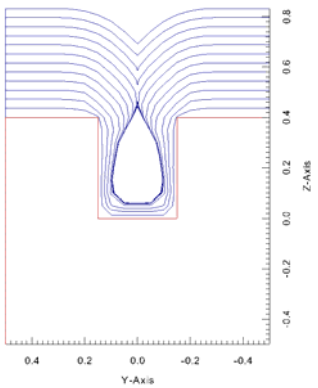
Simulation Models
Deposition and Etching Models

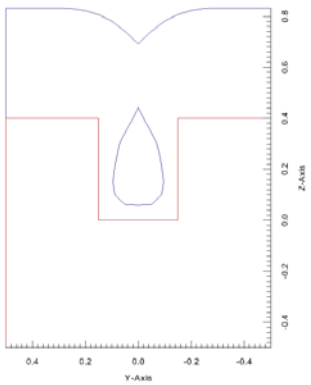
- Deposition models are available for
  - general non-linear multiple-species deposition, model is able to reproduce a plenum of processes driven by a multiple species by adjusting a few parameters
  - sputter deposition, chemical vapor deposition (CVD), ionized metal plasma deposition, plasma-enhanced CVD, and superconformal deposition
  - transient simulation of atomic layer deposition (ALD) and plasma-enhanced ALD (PEALD)
- Etching models are available for etching of different materials
  - such as (poly)silicon, silicon oxide, TiN, HfO_2
  - with different chemistries, such as Cl_2, HBr, SF_6, CH_2F_2, C_xH_y, CF_x, BCl_3

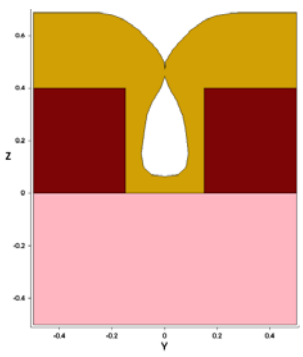
Simulation Examples
Low-temperature Oxide Deposition with Void Formation



- Simulation of low-temperature oxide (LTO) deposition with the LPCVD (low-pressure chemical vapor deposition) model of DEP3D using a sticking coefficient $s_c = 0.2$



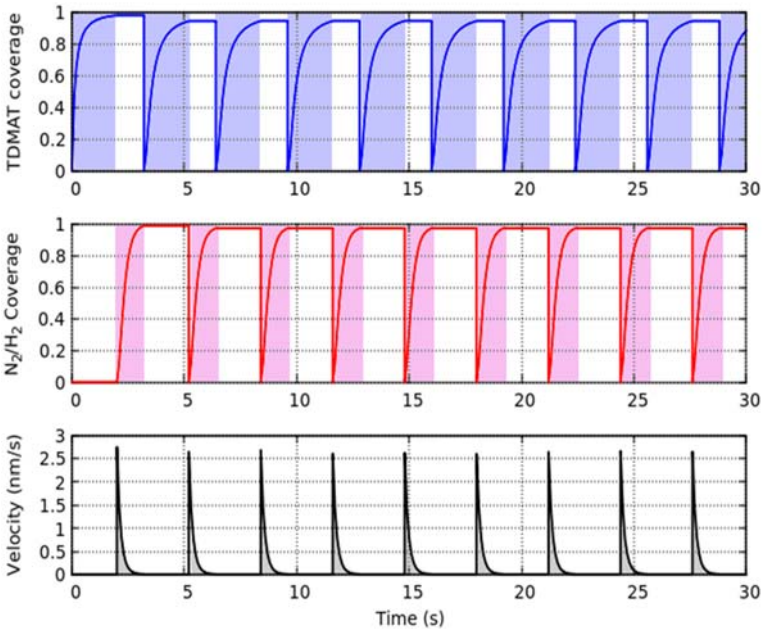




Simulation Examples

Plasma-enhanced Atomic Layer Deposition (PEALD)

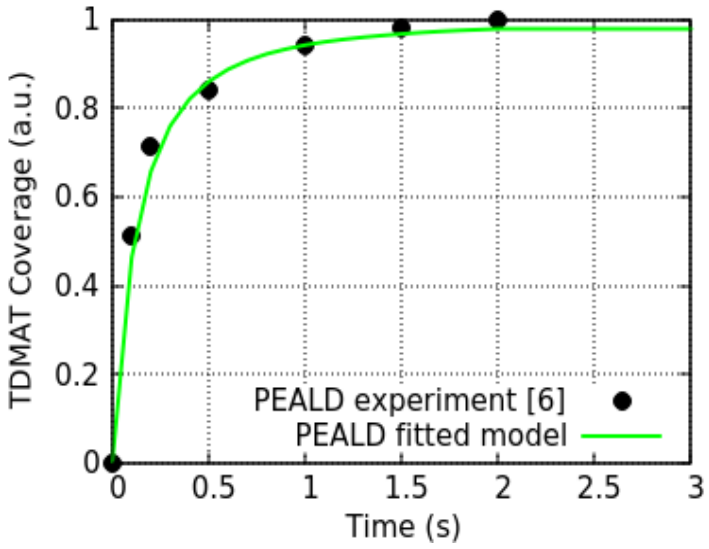
- TiN PEALD using TDMAT and N_2/H_2 plasma is modeled based on an adaptation of a model for conventional ALD.
- The film growth (deposition of a single layer of TiN) takes place only during the H_2-N_2 plasma step.



Simulation Examples

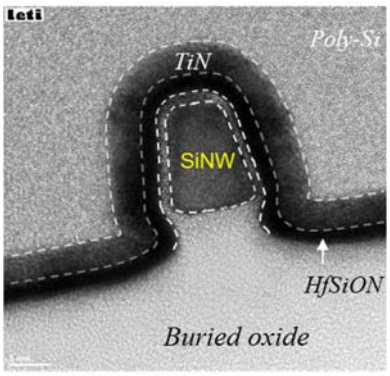
Plasma-enhanced Atomic Layer Deposition (PEALD)

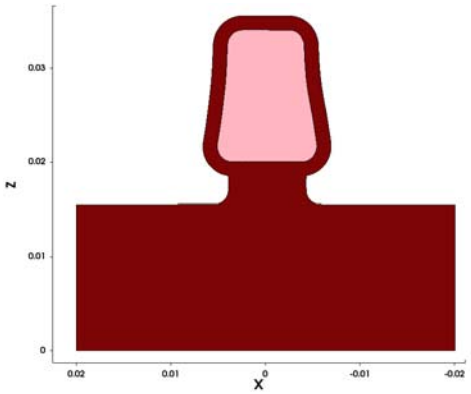
- We used the experimental data from literature to find the best fitting values for the model parameters.
- Adjusting the fitting parameters results in a PEALD model, which fits well with the measurements.



Simulation Examples
Simulation of Fin Etching

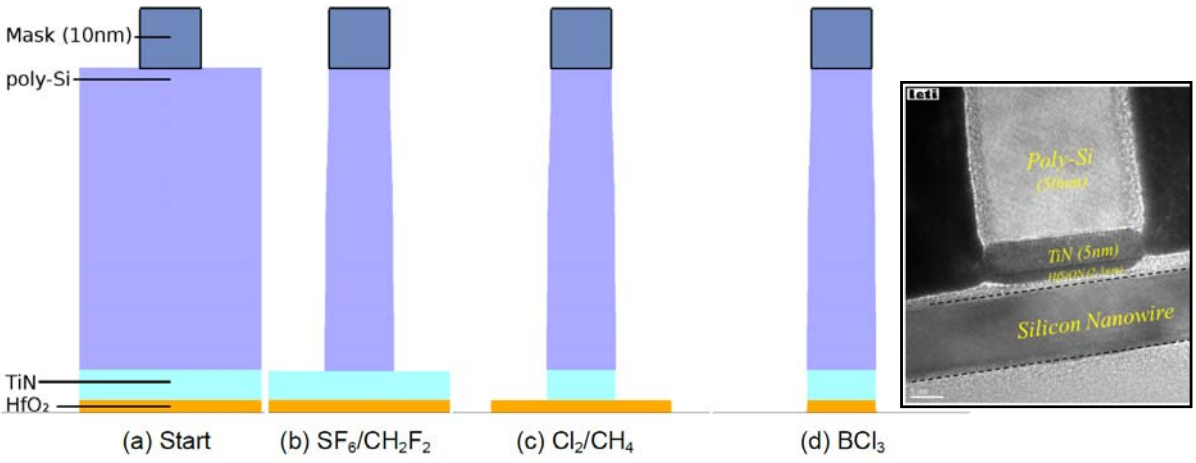
- Fin etching is carried out using a dry etching process with HBr, Cl_2, and oxygen chemistry.
- Using the corresponding model in ANETCH, the profiles can be reproduced using typical values for the fluxes of ions and neutrals and model parameters from literature.
- Further extension of the model will include the link to equipment simulation for obtaining boundary conditions for fluxes of ions and neutrals.





Simulation Examples
Simulation of Gate Stack Patterning

- Result of the simulation sequence used to etch through the gate stack of HfO_2 (1.9 nm), TiN (5 nm), and poly-Si (50 nm) using a 10 nm mask:



Conclusions and Outlook

- The topography modules allow the integrated simulation of lithography, etching, and deposition.
  - The software provides integration routines for the Fraunhofer and TU Wien tools, based on a Python frontend and a rate-based interface between ANETCH, DEP3D and the ViennaTS level set module.
  - The integration is extended by a Geometry Engine Python Package which provides additional functions.
- The data exchange with electrical simulation of devices and interconnects is possible via file exchange.
- The modules provide a large variety of physical models and capabilities for structure emulation.
  - They have been applied to the SUPERAID7 benchmarks cases.
  - This will be extended, particularly including equipment simulation, and using further experimental data, e.g., from the Industrial and Scientific Advisory Board.

SUPERAID7

Work Package on Variation-Aware Device and Interconnect Simulation

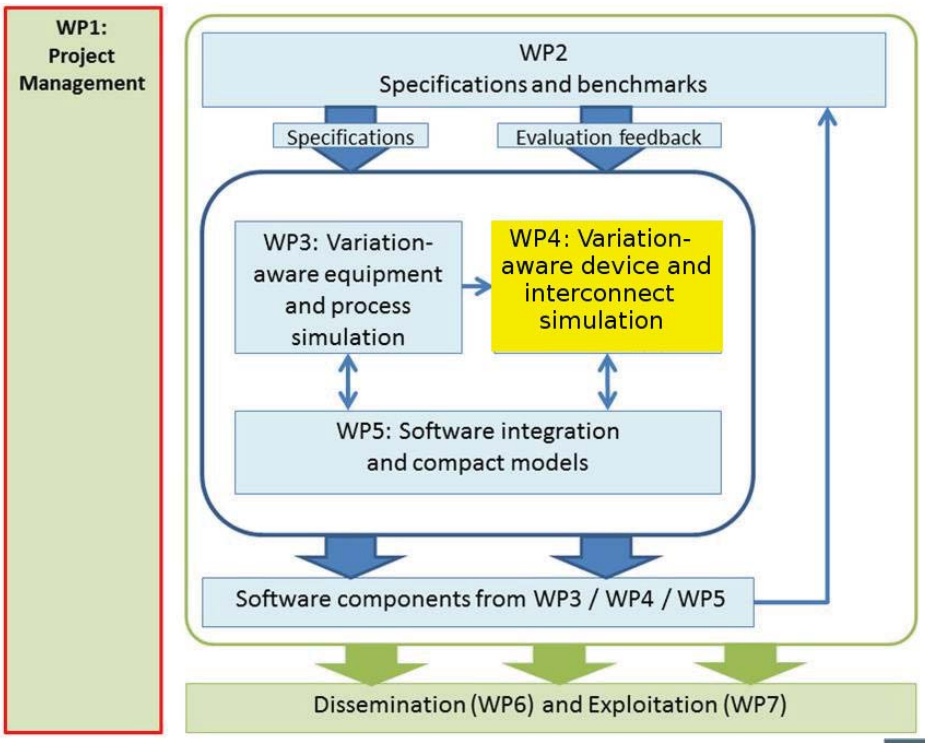
Work package coordinator: Mihail Nedjalkov, TU Wien
mixi@iue.tuwien.ac.at

SUPERAID 7

Content

SUPERAID 7

Work Package on Variation-Aware Device and Interconnect Simulation in Context



SUPERAID 7

Variation-Aware Device and Interconnect Simulation: Partners

IμE

GSS (now part of SYNOPSYS)

University of Glasgow

leti ceatech

SUPERAID 7

Variation-Aware Device and Interconnect Simulation: Objectives

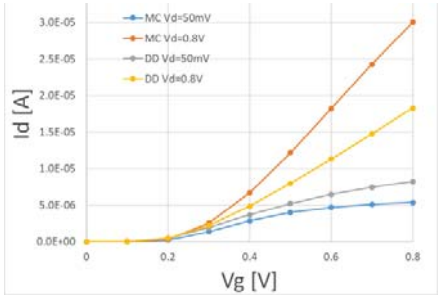
- To enable *device and advanced interconnect simulation tools* of GU/GSS to deal with realistic geometries including variability and process-induced variation.
- To develop and to implement *refined physical models* which are needed for the simulation of advanced devices like FinFET's and Nanowire transistors, especially when effects of *confinement*, quantum behavior and charge broadening come into play.
- To develop interconnect models which properly account for *grain boundary and surface roughness effects* on electron transport.

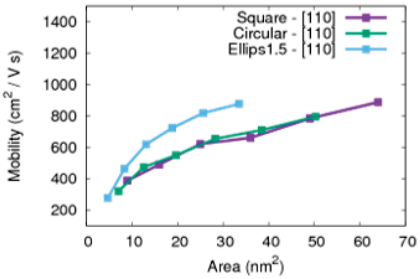
Confined Carrier Transport Models
Complete set MultiSub Scattering Models

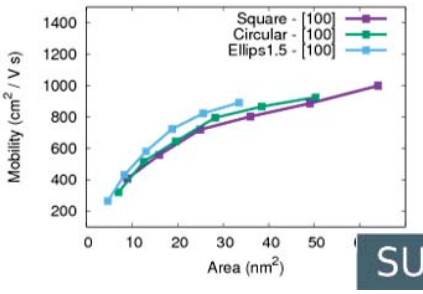
- Systematic Derivation of quantum aware scattering mechanisms which take into account the energy quantization and lack of momentum conservation due to electron confinement in Si, SiGe, Ge and III-V materials nanowires
- Most relevant processes of electron interaction with acoustic and deformation potential optical phonons, polar optical phonons, surface roughness, ionized impurities and alloy materials are taken into account
- Theoretical and numerical verification
- A self-contained document with a systematic derivation of the theory starting from first principles
- Dissemination

Confined Carrier Transport Models
1D MultiSub MC Simulator

- Multi-subband Monte Carlo simulator for confined channels investigated
- Incorporated the quantum aware scattering models developed as part of Superaid7 project
- Importance of capturing quantum confinement effects studied and highlighted *See reduced channel mobility as geometric confinement increased*
- Necessary to model quantum confinement effects for development of future FET technologies

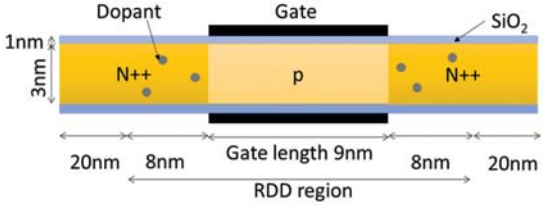


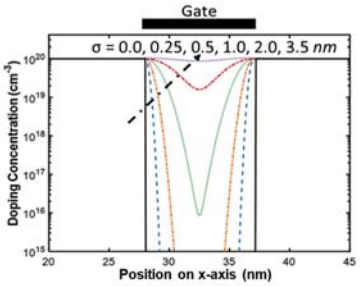


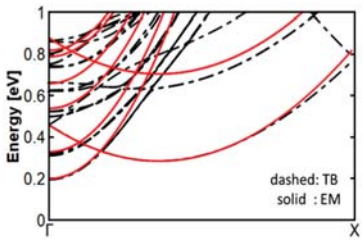


SUPERAID 7

Confined Carrier Transport Models
Atomistic model of the NWFET with RDF



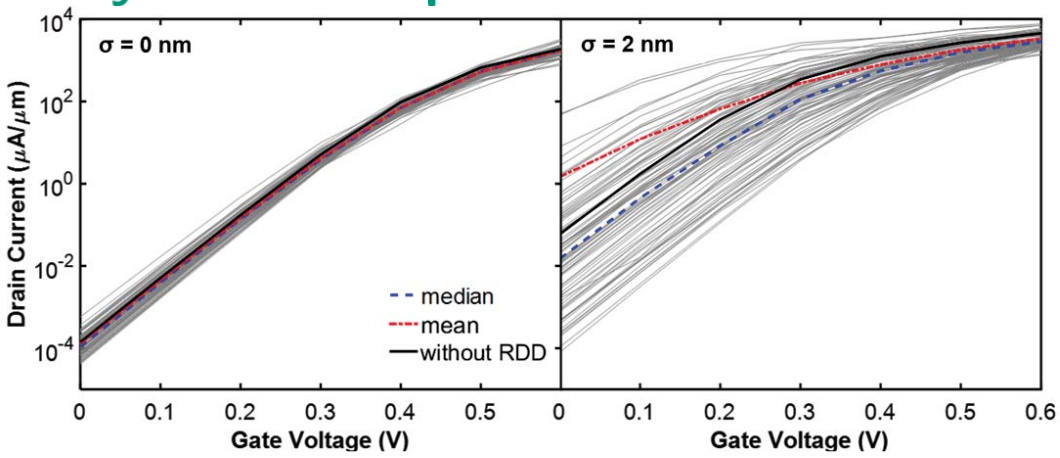




- Effect of random discrete dopant (RDD) penetration under the gate measured by σ , which is the standard deviation of the diffusion into the channel from the source-channel and drain-channel interfaces
- Calibrated effective masses using T.B: $ml = 0.954$ and $mt = 0.271$ instead of 0.891 and 0.201 for bulk Si

SUPERAID 7

Confined Carrier Transport Models
Variability from Coupled Mode NEGF

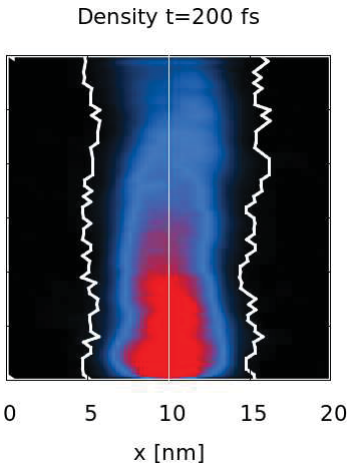


- I-V curves for 2 different values of σ. For each σ, an ensemble of 100 samples was considered
- The higher is σ, the higher is the variability
- The variability of many important figures of merit: I_{Off}, I_{On}, V_{th}, Subthreshold Slope, can be extracted from these $I-V$ curves

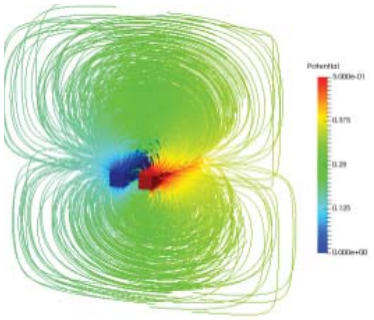
Confined Carrier Transport Models
Quantum Wire Surface Roughness Variability

Analysis of lithography induced variability in wire cross-section on electron transport via ab-initio Wigner simulations

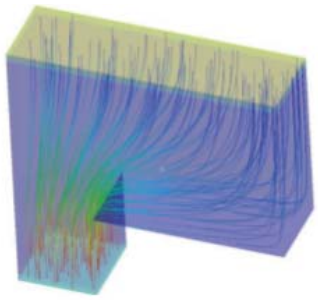
- Quantum simulations provide physical insight into the electron evolution process affected by the surface roughenss
- Interplay between quantum repulsion and penetration (tunneling) into the boundaries
- Validate the assumptions of the 1D MultiSub Surface Roughness scattering model



Process&Variability-Aware IC Simulations
Variability-Aware Interconnect Simulator

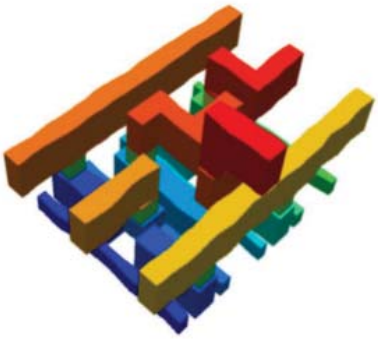


Calculated field lines

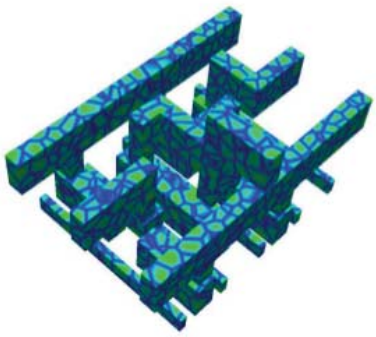


Current flow in interconnect line

- Field solver and conduction model used to obtain resistance in each wire and cross-capacitances



Line Edge Roughness (LER)



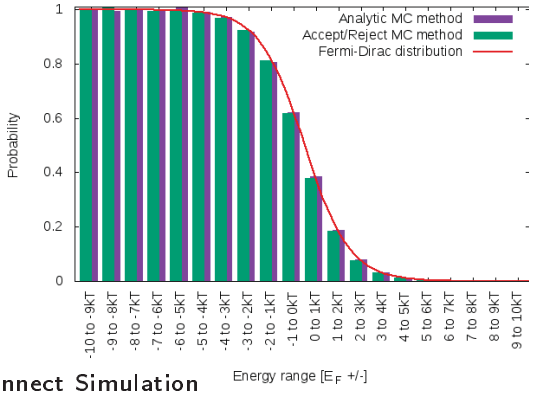
Metal Line Granularity (MLG)

- LER and MLG can be introduced into structure
- Process variation in line height and separation are also modelled

SUPERAID 7

Process&Variability-Aware IC Simulations
Monte Carlo Interconnect Simulator

- Cu electron statistics corresponds to the Fermi-Dirac (F-D) distribution
- An analytic Monte Carlo (MC) is used to sample the F-D distribution
- Three primary scattering events are considered:
  - Electron-electron - using a conductivity baseline and classical definition
  - Surface roughness - perturbation is given by a variation in the potential as a function of the longitudinal boundary axis
  - Grain boundary - columnar grains are assumed and each electron's location is tracked with respect to the two neighboring boundaries

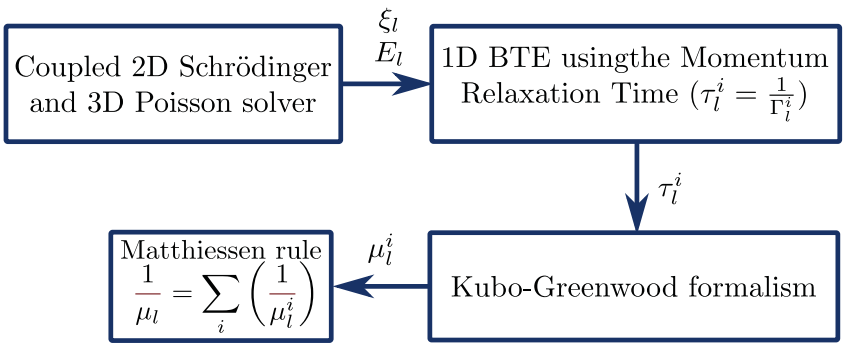


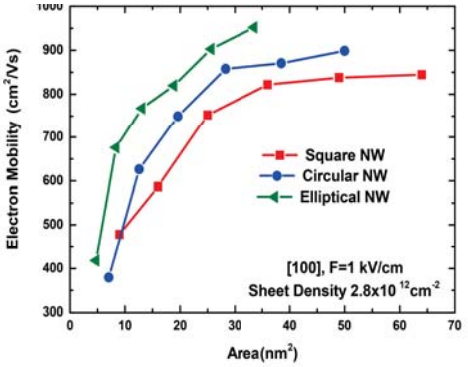
SUPERAID 7

Quantum Mobility Models and Effects

Quantum-aware mobility models based on MultiSub scattering models and Kubo-Greenwood theory

- Long-channel simulations $\Rightarrow$ reliable mobility in devices with strong confinement effects
- The mobility (μ_l^i) associated with each scattering mechanism is calculated using its rate ($\Gamma^i(l, k_z)$) by applying the Kubo-Greenwood formula
- Matthiessen's rule calculates the total mobility (μ_l)

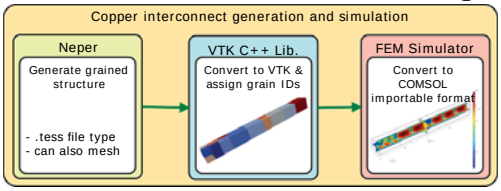


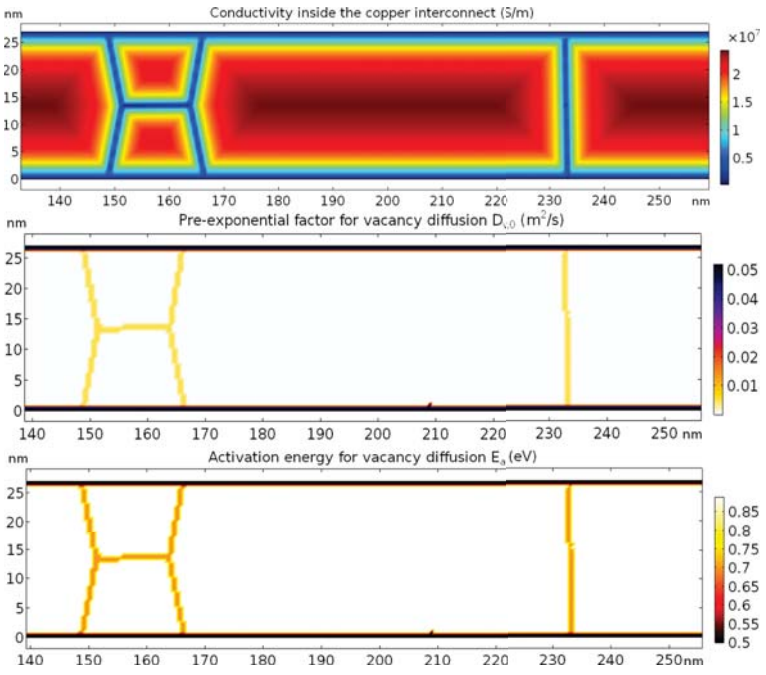


Reliability in Advanced Interconnects (IC's)

To analyze electromigration phenomena in copper nano-IC's, a proper treatment of grain boundaries (GB) and material interfaces (MI) is essential

- Several tools are used to generate a grained Cu structure and to import it into a finite element simulation tool
- GB and MI are treated as spatial parameters including conductivity/resistivity, vacancy diffusion pre-exponential factor, and activation energy





Conclusions

- The impact of confinement on carrier transport is approached by different frameworks for analysis
  - Derivation of a complete set of 1DMS scattring models
  - 1DMSMC: Capturing quantum confinements effects within the transport solution is imperative for predicting future FET performance
  - Statistical simulations using mode-space NEGF and effective masses calibrated using atomistic band structure calculations (Tight-Binding)
- Interconnect structures including process and statistical variability can be simulated, with resistances and capacitances extracted for use in circuit simulation. A MC model for electron scattering in copper has been developed
- The Kubo-Greenwood theory based on the MultiSub scattering models has been implemented for the calculation of the mobility in Si NWTs
- An efficient method to model microstructure dependent electromigration in copper nano-interconnects has been developed

SUPERAID7

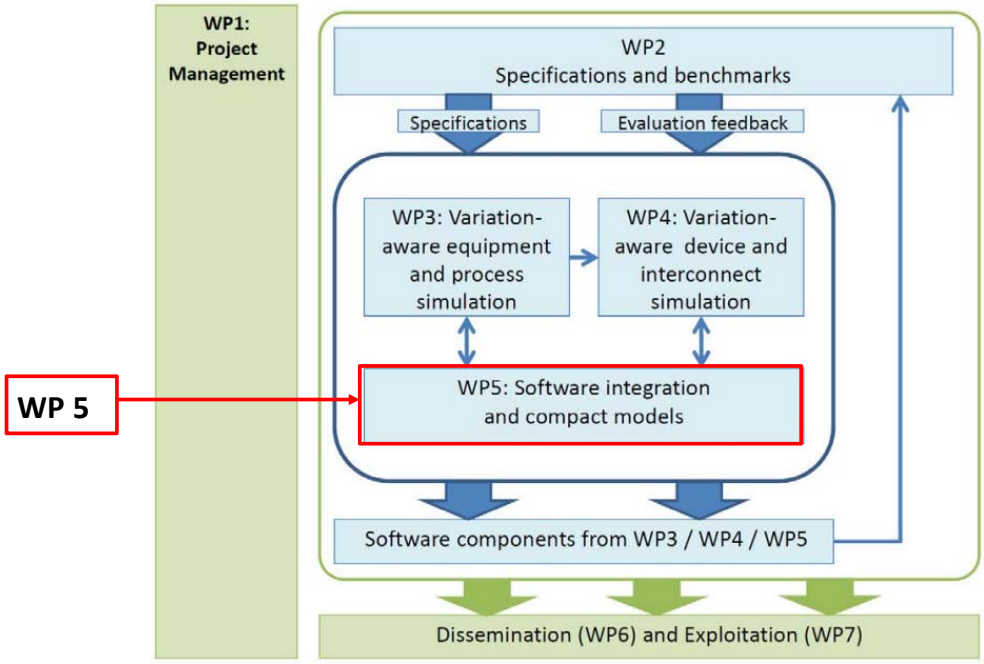
Work Package on Software Integration and Variation-Aware Compact Models

Work package coordinator: Asen Asenov, University of Glasgow

asen.asenov@glasgow.ac.uk

Contents

Work Package on Software Integration and Variation-Aware Compact Models in the Context of the Project



Software Integration and Variation-Aware Compact Models

Partners

Fraunhofer IISB

SYNOPSYS®

leti ceatech

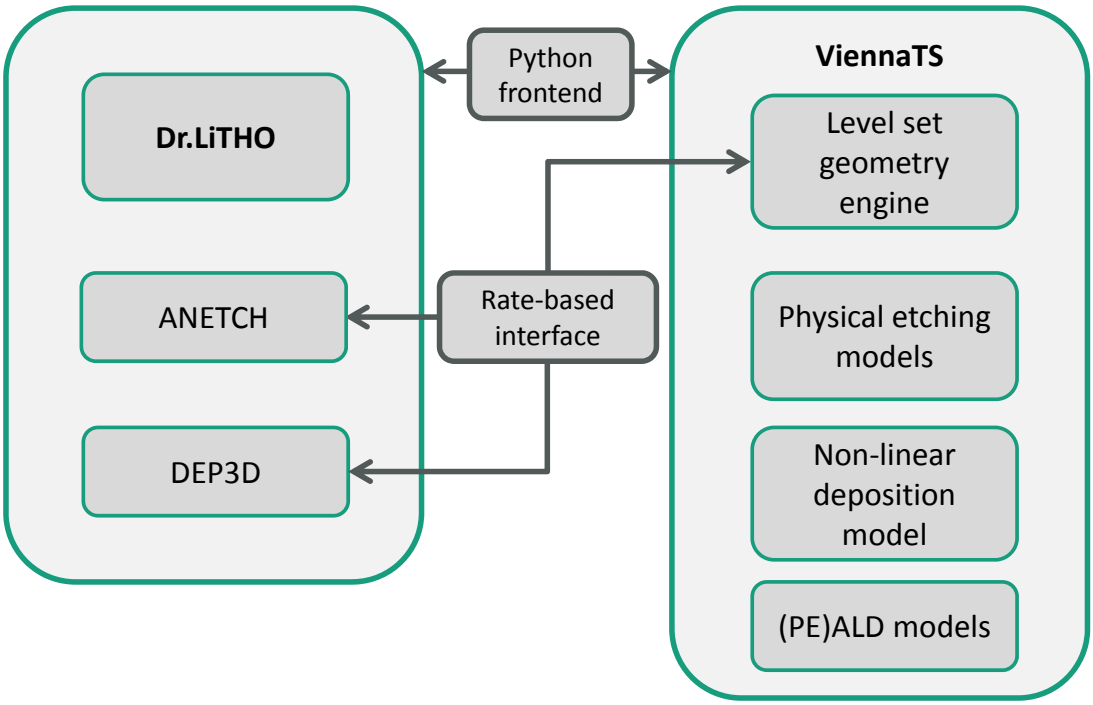
University of Glasgow

TU WIEN

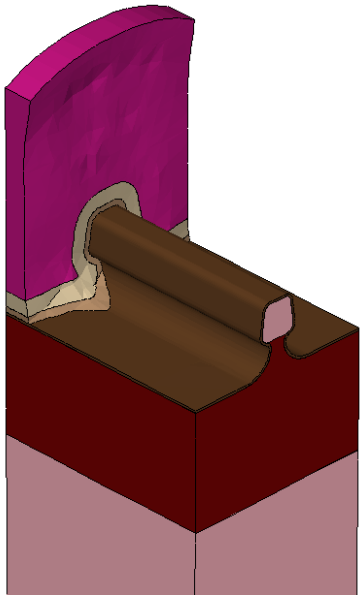
Software Integration and Variation-Aware Compact Models
Objectives

- Integrated tool chain of process, device and interconnect simulation software for advanced interconnects and advanced More Moore devices
- Compact model extraction for advanced interconnects
- Extraction of process- and statistical-variation-aware compact models for advanced devices
- Software provides capabilities to:
  - Capture all correlations between systematic and statistical process variability
  - Enable the assessment of the impact of variability on performance and reliability of critical circuits
  - Facilitate the development of Process Design Kits and enable full Design/Technology Co-Optimization (DTCO) of advanced technologies

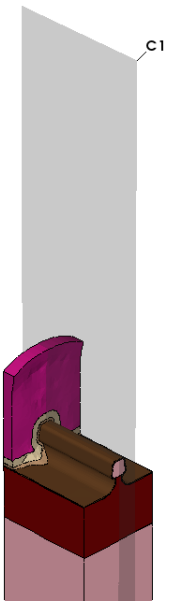
Software Integration
Topography Simulation Modules and their Interaction



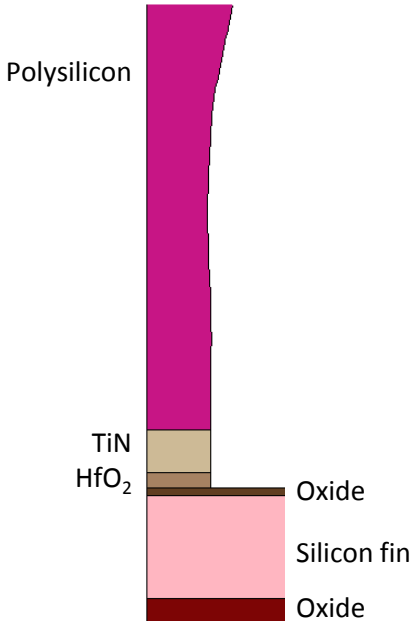
Integration of Topography Modules with Synopsys Tools via Boolean Operations



3D view of etched gate stack



Cut plane

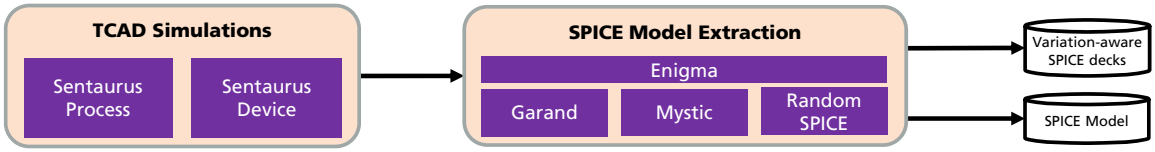


2D cut

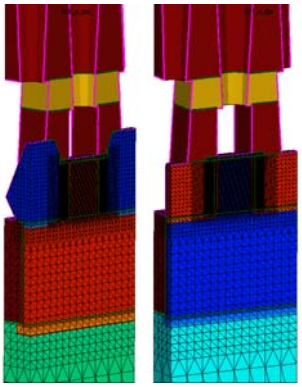
SUPERAID 7

Integration of Process and Device Simulation Software

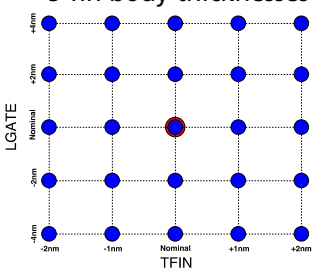
Pre-Wafer DTCO: TCAD-to-SPICE Integrated Flow



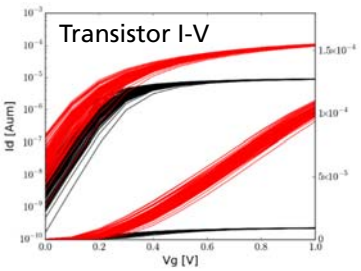
PMOS NMOS



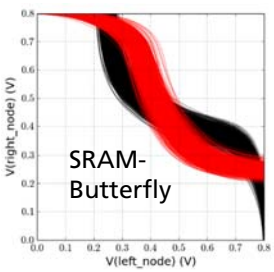
Global process variations:
5 gate lengths x
5 fin body thicknesses



200 Garand variability simulations for each global model



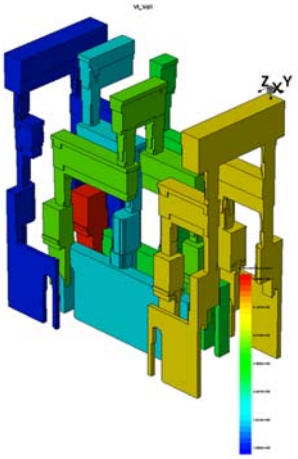
Circuit simulations using RandomSPICE / HSPICE

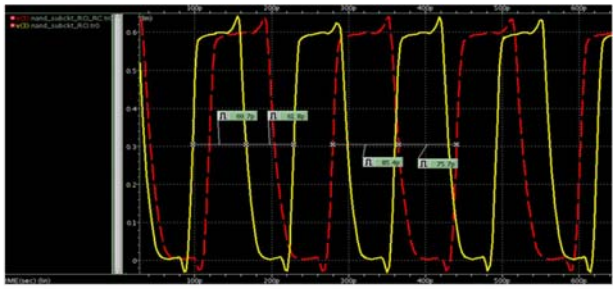


SUPERAID 7

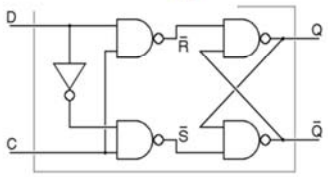
Compact Model Extraction for Advanced Interconnects

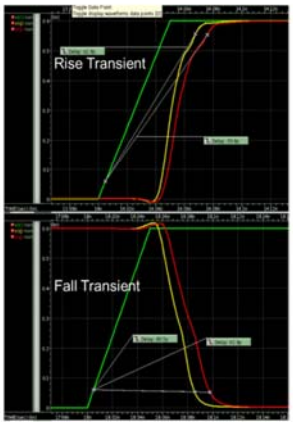
TCAD-based Early SPICE Modeling of BEOL





NAND-based ring oscillator with and w/o RC





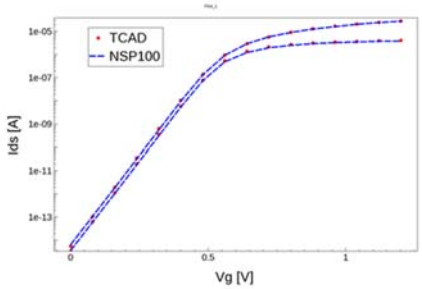
NAND-based latch circuit with and w/o RC

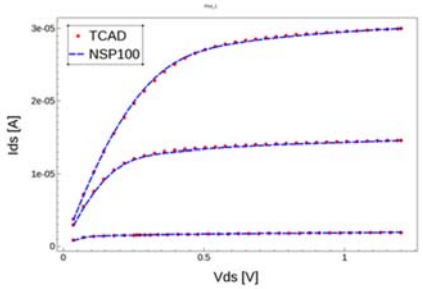
SUPERAID 7

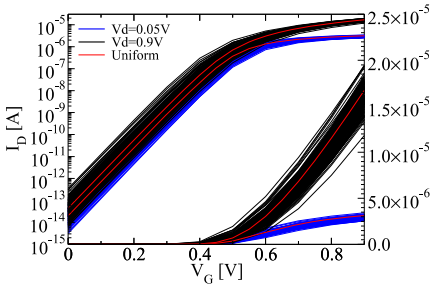
Process and Statistical-Variation-Aware Compact Models

Variation-Aware Compact Models for Tri-Gate Benchmark

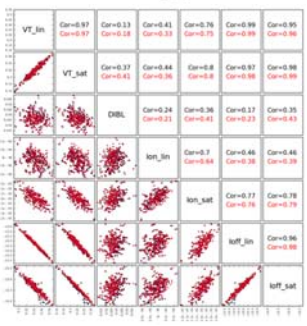
- TCAD simulation of nominal device, statistical variability and process Design of Experiment (DoE).
- LETI NSP compact model extraction fits TCAD target.
- ModelGen technology allows generation of compact models that retain all statistical correlations of FoMs across process variation DoE.



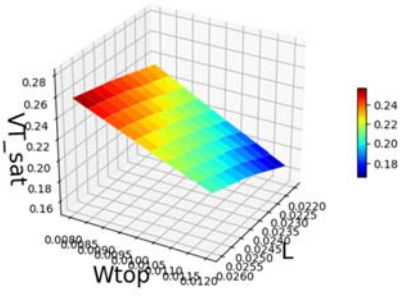




Statistical variability simulation in Garand, including random discrete dopants, line edge roughness and metal gate granularity.



Compact models preserve the figures of merit (FoM) correlations obtained from the statistical TCAD simulations



Variation of VT across the DoE space as captured by the response-surface compact model.

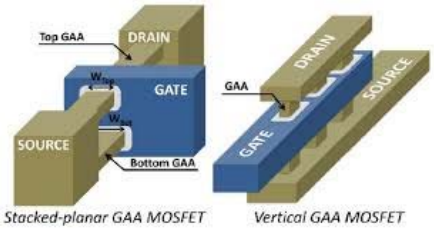
SUPERAID 7

Extraction of Process- and Statistical-Variation-Aware Compact Models for Advanced Devices

Before the project:

- BSIM-CMG was the only standard model to support 3D MOSFET architectures.
- Rectangular cross-section with rounded corners was not considered.
- Stacked-Nanowires/Nanosheets were not considered: no management of width variation between top and bottom wires; no parasitics elements.

Progress during the project:



Stacked-planar GAA MOSFET Vertical GAA MOSFET

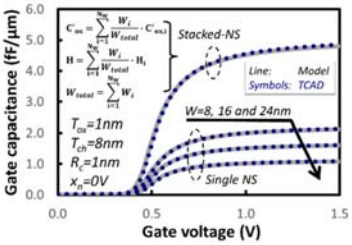
- A predictive and physical compact model for NanoWire/NanoSheet (NW/NS) Gate-All-Around (GAA) MOSFETs was developed.
- Based on a novel methodology for the calculation of the surface potential including quantum confinement, this model is able to handle arbitrary NW/NS cross-section shapes of stacked-planar and vertical GAA MOSFETs (circular, square, rectangular).
- The model is validated both by numerical simulations and experimental data.

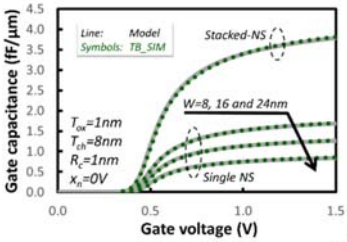
Extraction of Process- and Statistical-Variation-Aware Compact Models for Advanced Devices

Model features: Leti-NSP model

Interface states
Quantum confinement effect
Management of SiGe channel for p-Fet
Short channel effects (VT, Subthreshold-Slope)
DIBL
Electrical field dependence on mobility
Velocity saturation
Channel length modulation in saturation
Series resistances
Asymmetrical junctions
Overlap and Inner fringe capacitances
Gate tunneling currents
GIDL/GISL currents
Self heating effect
More physical modeling of channel length modulation
Gate (bottom part) to substrate parasitic capacitance for stacked GAA MOSFET
Quantum effect on carrier transport properties
Predictive model for parasitic elements (R and C)
Noise modeling (LF, HF)
Gate resistance model

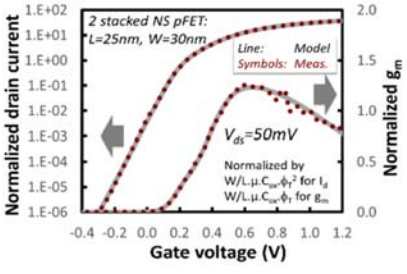
Core model Validation (from TCAD)





Quantum confinement effects validation on advanced simulation tool (tight-binding) WP4

Final validation on exp. data (from WP2)



Model is completed for SUPERAID7
Ongoing work: management of junctionless devices

Conclusions

- The SUPERAID7 simulation modules for topography steps (lithography, etching, deposition) have been tightly integrated and provide interfaces to device and interconnect simulation modules.
- The GSS TCAD-to-SPICE DTCO flow is fully integrated within the industry-standard Sentaurus Workbench, with an integrated data transfer between GSS tools based on a common database.
- Interconnect structures including process and statistical variability are simulated, and the resultant resistances and capacitances are captured in a SPICE netlist for inclusion in variability-aware circuit simulations.
- A predictive and physical compact model for Gate-All-Around (GAA) stacked NanoWire/NanoSheet (NW/NS) MOSFETs has been developed, validated on experimental data, and integrated with the GSS tools.
- The integrated TCAD-to-SPICE flow is used to take TCAD simulations of the benchmark devices, including process and statistical variability, and extract variability-aware compact models based on the Leti model for use in circuit simulations.