ICT Project No 688101
SUPERAID7
Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

D6.3: Summary of Results of SUPERAID7 Dissemination Actions (Events, Papers)

	Name	Organisation	Date
Edited	Eberhard Baer	Fraunhofer IISB	January 17, 2019

Contents

Abstract

This deliverable summarizes the dissemination actions of SUPERAID7 carried out by the organization of workshops and participation in further events and by the publication of papers in peer-reviewed journals and conference proceedings. The related presentations and papers are available for download in the public section at the SUPERAID7 webpage.

1. Introduction

Successful, broad and well targeted dissemination is an essential contribution to the exploitation of the project results. On the other hand it is important to make sure that open dissemination is not negatively affecting commercialization. In the following, the SUPERAID7 dissemination via events and papers is summarized. A particularly important additional channel for dissemination is the SUPERAID7 WWW (www.superaid7.eu) which is described in deliverable D6.4 "Final version of SUPERAID7 WWW including restricted section and including material from the SUPERAID7 Workshop".

2. Events

Conferences

Considerable research activities and high-level scientific results have been necessary to achieve the objectives of SUPERAID7. This requires close interaction with the scientific communities in various fields of TCAD. In consequence, it has been vital for SUPERAID7 to publish its results at conferences most important in the scientific and technological areas covered by the project.

Due to the topics of SUPERAID7, different scientific areas are relevant in terms of participation in conferences. Relevant for the project are for instance technology-oriented conferences such as IEDM or EUROSOI-ULIS, device simulation-oriented conferences such as SISPAD, and conferences on nanotechnology such as NMDC and SPIE. A selection of the most important events where results of SUPERAID7 have been presented is given at the SUPERAID7 website (see Appendix A). The SUPERAID7 papers published in the conference proceedings are part of the publications list at the SUPERAID7 website and are available for download there (see Appendix B).

Workshops

An essential part of the SUPERAID7 dissemination strategy has been the organization of workshops or the participation in workshops:

- SUPERAID7 participated in the **2018 European Forum on Electronics Components and Systems (EFECS)** held from November 20-22, 2018 in Lisbon, Portugal, via two SUPERAID7 posters presented by J. Lorenz, Fraunhofer IISB.
- The public **SUPERAID7 workshop "SUPERAID7 - Process variations from equipment effects to circuit and design impact"** was held on September 3, 2018 in conjunction with the ESSDERC/ESSCIRC conference in Dresden, Germany. It consisted of eight presentations from SUPERAID7 and one external industrial keynote. The latter was linked to the ECSEL project Way2GoFast. In total, the workshop was attended by about 20 participants. Further information is given in deliverable D1.8. At the SUPERAID7 webpage, all presentations of the workshop are available for download.

- SUPERAID7 participated in the **3rd European Nanoelectronics Forum 2016** held from November 23-24, 2016 in Rome, Italy, via a SUPERAID7 poster presented by J. Lorenz, Fraunhofer IISB.
- The SUPERAID7 project was also represented at the **PATMOS/VARI Conference 2016**, September 21-23, 2016, Bremen, Germany. At the workshop the presentation "Project SUPERAID7: Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm node" was given by J. Lorenz, Fraunhofer IISB.
- On September 5, 2106, SUPERAID7 co-organized two **workshops linked to the SISPAD 2016 conference** in Nuremberg, Germany:
    - Workshop 1 "Simulation of Advanced Interconnects"
    - Workshop 3 "Variability-Aware Design Technology Co-Optimization"

Further information about these workshops is provided at the SUPERAID7 webpage.

3. Papers

All publications of SUPERAID7 are available via either gold or green open access. The corresponding download links are provided in the list of publications at the SUPERAID7 website (see Appendix B).

Peer-Reviewed Publications

Publications in renowned scientific journals have been mandatory to attract attention to the results of the project. The peer-reviewed papers are either part of conference proceedings or have been submitted to journals. The papers are included in the list of publications at the SUPERAID7 website (see Appendix B).

Papers in Conference Proceedings

The SUPERAID7 papers published in conference proceedings are part of list of publications at the SUPERAID7 website (see Appendix B).

Appendix A: List of events at the SUPERAID7 webpage, status as of January 9, 2019

Appendix B: List of publications at the SUPERAID7 webpage, status as of January 17, 2019

SUPERAID 7

Events

SUPERAID7 - Events

2018 IEEE International Electron Devices Meeting ↗ (IEDM 2018)

December 1-5, 2018, San Francisco, United States

The following presentation will report on results of SUPERAID7:
S. Barraud et al., Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets
in: Session 21 (Tuesday, December 4, 2:15 pm, Continental Ballroom 5): Process and Manufacturing Technology - Advanced Gate All Around Process

SUPERAID7 is an exibitor at

European Forum for Electronic Components and Systems (EFECS) 2018 ↗

November 20-22, 2018, Lisbon, Portugal

SUPERAID7 posters at EFECS 2018

SUPERAID7 Workshop
Process Variations from Equipment Effects to Circuit and Design Impacts
(linked to ESSDERC/ESSCIRC 2018)

September 3, 2018, Dresden, Germany

Material for download

233rd Meeting of the Electrochemical Society (ECS Spring Meeting 2018) ↗

May 13-17, 2018, Seattle, United States

In an invited presentation results from SUPERAID7 were shown:
J. Lorenz, Process Variability for Devices at and beyond the 7 nm Node ↗

2017 IEEE International Electron Devices Meeting ↗ (IEDM 2017)

December 2-6, 2017, San Francisco, United States

The following paper reported on results of SUPERAID7:
S. Barraud et al., Performance and Design Considerations for Gate-All-around Stacked-NanoWires FETs

2017 International Conference on Solid State Devices and Materials (SSDM 2017) ⌐⌐

September 19-22, 2017, Sendai, Japan

An invited presentation showed results from SUPERAID7:

S. Barraud et al., Stacked-Wires FETs for Advanced CMOS Scaling

International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2017 ⌐⌐

September 7-9, 2017, Kamakura, Japan

Among others, a plenary presentation showed results from SUPERAID7:
J.-C. Barbé et al., Stacked Nanowires/Nanosheets Gate-All-Around MOSFET from Technology to Design Enablement

2016 ⌐⌐ IEEE International Electron Devices Meeting ⌐⌐ (IEDM 2016)

December 3-7, 2016, San Francisco, United States

The following papers reported on results from SUPERAID7:
Paper 7.5 - NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs, by O. Rozeau et al.
Paper 17.6 - Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain, by S. Barraud et al.

European Nanoelectronics Forum 2016 ⌐⌐

November 23-24, 2016, Rome, Italy

SUPERAID7 poster at ENF

PATMOS & VARI 2016 ⌐⌐
International Workshop on Timing Modeling, Organization and Simulation (PATMOS 2016) in conjunction with the European Workshop on CMOS Variability (VARI 2016)

September 21 to 23, 2016, Bremen, Germany

Presentation by J. Lorenz on SUPERAID7

International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2016 ⌐⌐
(organized by Fraunhofer IISB)

September 6-8, 2016, Nuremberg, Germany

In 6 papers at SISPAD 2016, results of SUPERAID7 were shown, please refer to the SUPERAID7 publications list for further information.

The SISPAD 2016 workshops WS1 (Simulation of Advanced Interconnects) and WS3 (Variability-Aware Design Technology Co-Optimization) were organized in cooperation with SUPERAID7.
Further information

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Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

Online in Internet; URL: https://www.superaid7.eu/en/events.html

Date: 9.1.2019 13:32

The SISPAD 2016 workshops WS1 (Simulation of Advanced Interconnects) and WS3 (Variability-Aware Design Technology Co-Optimization) were organized in cooperation with SUPERAID7.
Further information

SUPERAID **7**

SUPERAID7 - Publications

Public deliverables can be found here.

Selected journal and conference papers for the different work packages of the project can be found here.

SUPERAID7 Journal and Conference Papers

2019

J. Lorenz, E. Bär, S. Barraud, A.R. Brown, P. Evanschitzky, F. Klüpfel, L. Wang, Process Variability - Technological Challenge and Design Issue for Nanoscale Devices, Micromachines 10 (2019) 6   Download

T. Sadi, C. Medina-Bailon, M. Nedjalkov, J. Lee, O. Badami, S. Berrada, H. Carillo-Nunez, V. Georgiev, S. Selberherr, A. Asenov, Simulation of the Impact of Ionized Impurity Scattering on the Total Mobility in Si Nanowire Transistors, Materials 12 (2019) 124 Download

2018

T. Al-Ameri, Correlation between the Golden Ratio and Nanowire Transistor Performance, Appl. Sci. 8 (2018) 54   Download

E. Baer, J. Lorenz, The Effect of Etching and Deposition Processes on the Width of Spacers Created during Self-Aligned Double Patterning, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 236   Download

Z. Belete, E. Baer, A. Erdmann, Modeling of Block Copolymer Dry Etching for Directed Self-Assembly Lithography, Proc. of SPIE 10589 (2018) 105890U   Download

S. Berrada, J. Lee, H. Carillo-Nunes, C. Medina-Bailon, F. Adamu-Lema, V. Georgiev, A. Asenov, Quantum Transport Investigation of Threshold Voltage Variability in Sub-10nm Junctionless Si Nanowire FETs, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 244   Download

B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, Electrical Characterization of Vertically Stacked p-FET SOI Nanowires, Solid-State Electronics 141 (2018) 84   Download

B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, Methodology to Separate Channel Conductions of Two Level Vertically Stacked SOI Nanowire MOSFETs, Solid-State Electronics 149 (2018) 62   Download

L. Filipovic, R.L. de Orio, Modeling the Influence of Grains and Material Interfaces on Electromigration, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 83   Download

X. Klemenschits, S. Selberherr, L. Filipovic, Unified Feature Scale Model for Etching in SF_6 and Cl Plasma Chemistries, in: Proceedings of EUROSOI-ULIS 2018, 2018, p. 65   Download

X. Klemenschits, S. Selberherr, L. Filipovic, Modeling of Gate Stack Patterning for Advanced Technology Nodes: A Review, Micromachines 9 (2018) 631   Download

J. Lee, O. Badami, H. Carrillo-Nunez, S. Berrada, C. Medina-Bailon, T. Dutta, F. Adamu-Lema, V.P. Georgiev, Variability Predictions for the Next Technology Generations of n-type SixGe1−x Nanowire MOSFETs, Micromachines 9 (2018) 643   Download ⌐⌐

J. Lee, S. Berrada, H. Carillo-Nunez, C. Medina-Bailon, F. Adamu-Lema, V. Georgiev, A. Asenov, The Impact of Dopant Diffusion on Random Dopant Fluctuation in Si Nanowire FETs: A Quantum Transport Study, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 280   Download ⌐⌐

J.K. Lorenz, A. Asenov, E. Bär, S. Barraud, C. Millar, M. Nedjalkov, Process Variability for Devices at and beyond the 7 nm Node, in: Proceedings of the 18th Symposium on Advanced CMOS-Compatible Semiconductor Devices, Ed. J.A. Martino, J.P. Raskin, S. Selberherr, H. Ishii, F. Gamiz, B.Y. Nguyen, A. Yoshino, The Electrochemical Society, ECS Transactions 85-8, 2018, p. 113   Download ⌐⌐

J.K. Lorenz, A. Asenov, E. Bär, S. Barraud, F. Kluepfel, C. Millar, M. Nedjalkov, Process Variability for Devices at and beyond the 7 nm Node, ECS J. Solid State Science Technol. 7 (2018) P595   Download ⌐⌐

C. Medina-Bailon, T. Sadi, M. Nedjalkov, J. Lee, S. Berrada, H. Carillo-Nunez, V. Georgiev, S. Selberherr, A. Asenov, Study of the 1D Scattering Mechanisms´ Impact on the Mobility in Si Nanowire Transistors, in: Proceedings of EUROSOI-ULIS 2018, 2018, p. 17   Download

C. Medina-Bailon, T. Sadi, M. Nedjalkov, J. Lee, S. Berrada, H. Carillo-Nunez, V. Georgiev, S. Selberherr, A. Asenov, Impact of the Effective Mass on the Mobility in Si Nanowire Transistors, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 297   Download ⌐⌐

M. Nedjalkov, P. Ellinghaus, J. Weinbub, T. Sadi, A. Asenov, I. Dimov, S. Selberherr, Stochastic Analysis of Surface Roughness Models in Quantum Wires, Comp. Phys. Comm. 228 (2018) 30   Download ⌐⌐

2017

T. Al-Ameri, V.P. Georgiev, F. Adamu-Lema, A. Asenov, Simulation Study of Vertically Stacked Lateral Si Nanowires Transistors for 5-nm CMOS Applications, J. Electron Dev. Soc. 5 (2017) 466   Download

T. Al-Ameri, V. Georgiev, F. Adamu-Lema, A. Asenov, Does a Nanowire Transistor Follow the Golden Ratio, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 57   Download

J.-C. Barbé, S. Barraud, O. Rozeau, S. Martinie, J. Lacord, P. Blaise, Z. Zeng, L. Bourdet, F. Triozon, Y. Niquet, Stacked Nanowires/Nanosheets GAA MOSFET From Technology to Design Enablement, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 5   Download

S. Barraud et al., Performance and Design Considerations for Gate-All-Around Stacked-NanoWires FETs, in: Proceedings International Electron Devices Meeting (IEDM) 2017   Download ⌐⌐

S. Barraud, V. Lapras, M. Samson, B. Previtali, J. Hartmann, N. Rambal, C. Vizioz, V. Loup, C. Comboroure, F. Triozon, N. Bernier, D. Cooper, M. Vinet, Stacked-Wires FETs for Advanced CMOS Scaling , Proceedings 2017 International Conference on Solid State Devices and Materials (SSDM 2017)   Download ⌐⌐

B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, New Method for Individual Electrical Characterization of Stacked SOI Nanowire MOSFETs, in: Proceedings 2017 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)   Download ⌐⌐

B. Cardoso Paz, M. Pavanello, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires, in: Proceedings 2017 Joint International EUROSOI-ULIS Workshop   Download ⌐⌐

P. Ellinghaus, J. Weinbub, M. Nedjalkov, S. Selberherr, Analysis of Lense-governed Wigner Signed Particle Quantum Dynamics, Phys. Status Solidi RRL 11 (2017) 1700102   Download

P. Ellinghaus, M. Nedjalkov, J. Weinbub, S. Selberherr, Wigner Analysis of Surface Roughness in Quantum Wires, International Wigner Workshop (IW2), Book of Abstracts, 2017, p. 40   Download

L. Filipovic, R.L. de Orio, W. Zisser, S. Selberherr, Modeling Electromigration in Nanoscaled Copper Interconnects, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 161   Download

V.P. Georgiev, M.M. Mirza, A.I. Dochioiu, F.A. Lema, S.M. Amoroso, E. Towie, C. Riddet, D.A. MacLaren, A. Asenov, D.J. Paul, Experimental and Simulation Study of 1D Silicon Nanowire Transistors using Heavily Doped Channels, IEEE Trans. Nanotechnology 16

(2017) 727   Download ⬈

J. Weinbub, M. Nedjalkov, I. Dimov, S. Selberherr, Wigner-signed Particles Study of Double Dopant Quantum Effects, International Wigner Workshop (IW2), Book of Abstracts, 2017, p. 50   Download ⬈

Z. Zeng, F. Triozon, S. Barraud, Y.-M. Niquet, A Simple Interpolation Model for the Carrier Mobility in Trigate and Gate-All-Around Silicon NWFETs, IEEE, Trans. Electr. Dev. 64 (2017) 2485   Download ⬈

2016

T. Al-Ameri, V. Georgiev, F.-A. Lema, T. Sadi, X. Wang, E. Towie, C. Riddet, C. Alexander, A. Asenov, Impact of Strain on the Performance of Si Nanowires Transistors at the Scaling Limit: A 3D Monte Carlo / 2D Poisson Schrodinger Simulation Study, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 213   Download

S. Barraud et al., Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain, in: Proceedings International Electron Devices Meeting (IEDM) 2016   Download ⬈

L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Casse, S. Barraud, S. Martinie, D. Rideau, Y. Niquet, High and Low-field Contact Resistances in Trigate Devices in a Non-Equilibrium Green´s Functions Framework, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 291   Download

V.P. Georgiev, M.M. Mirza, A.-I. Dochioiu, F.-A. Lema, S.M. Amoroso, E. Towie, C. Riddet, D.A. MacLaren, A. Asenov, D.J. Paul, Experimental and Simulation Study of a High Current 1D Silicon Nanowire Transistor using Heavily Doped Channels, in: Proceedings of 2016 IEEE Nanotechnology Materials and Devices Conference (NMDC)   Download ⬈

O. Rozeau et al., NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs, in: Proceedings International Electron Devices Meeting (IEDM) 2016   Download ⬈

T. Sadi, E. Towie, M. Nedjalkov, C. Riddet, C. Alexander, L. Wang, V. Georgiev, A. Brown, C. Millar, A. Asenov, One-Dimensional Multi-Subband Monte Carlo Simulation of Charge Transport in Si Nanowire Transistors, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 23   Download

L. Wang, B. Cheng, P. Asenov, A. Pender, D. Reid, F. Adamu-Lema, C. Millar, A. Asenov, TCAD Proven Compact Modelling Re-centering Technology for Early 0.x PDKs, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 157   Download

Z. Zeng, F. Triozon, Y. Niquet, S. Barraud, Size-dependent Carrier Mobilities in Rectangular Silicon Nanowire Devices, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 257   Download

Z. Zeng, F. Triozon, Y. Niquet, Carrier Scattering by Workfunction Fluctuations and Interface Dipoles in high-κ/Metal Gate Stacks, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 369   Download

Publications on Partners' Background Work

2016

T. Al-Ameri, V.P. Georgiev, F. Adamu-Lema, X. Wang, A. Asenov, Influence of Quantum Confinement Effects and Device Electrostatic Driven Performance in Ultra-Scaled SixGe1-x Nanowire Transistors, in: Proceedings of 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), IEEE, 2016, pp. 234

A. Asenov, Y. Wang, B. Cheng, X. Wang, P. Asenov, T. Al-Ameri, V.P. Georgiev, Nanowire Transistor Solutions for 5 nm and Beyond, in: Proceedings of 17th International Symposium on Quality Electronic Design (ISQED), IEEE, 2016, pp. 269

E. Baer, J. Niess, Equipment Simulation for Studying the Growth Rate and its Uniformity of Oxide Layers Deposited by Plasma-Enhanced Oxidation, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2016 (SISPAD 2016), p. 137 Download

E. Baer, A. Burenkov, P. Evanschitzky, J. Lorenz, Simulation of Process Variations in FinFET Transistor Patterning, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2016 (SISPAD 2016), p. 299   Download

A. Burenkov, J. Lorenz, Simulation of Thermo-mechanical Effect in Bulk-silicon FinFETs, Materials Science in Semiconductor Processing 42 (2016) 242

L. Wang, T. Sadi, M. Nedjalkov, A. R. Brown, C. Alexander, B. Cheng, C. Millar, A. Asenov, Simulation Analysis of the Electro-thermal Performance of SOI FinFETs, in: Proc. of 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), IEEE, 2016, p. 56   Download

X. Wang, D. Reid, L. Wang, C. Millar, A. Burenkov, P. Evanschitzky, E. Bär, J. Lorenz, A. Asenov, Process Informed Accurate Compact Modelling of 14-nm FinFET Variability and Application to Statistical 6T-SRAM Simulations, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2016 (SISPAD 2016), p. 303   Download

2015

E. Baer, P. Evanschitzky, J. Lorenz, F. Roger, R. Minixhofer, L. Filipovic, R.L. de Orio, S. Selberherr, Coupled Simulation to Determine the Impact of across Wafer Variations in Oxide PECVD on Electrical and Reliability Parameters of Through-silicon Vias, Microelectronic Engineering 137 (2015) 141

S. Barraud, M. Cassé, L. Gaben, P. Nguyen, J.M. Hartmann, M.P. Samson, V. Maffini-Alvaro, C. Tabone, C. Vizioz, C. Arvet, P. Pimenta-Barros, F. Glowacki, N. Bernier, O. Rozeau, M.A. Jaud, S. Martinie, J. Laccord, F. Allain, B. De Salvo, and M. Vinet, "Opportunities and challenges of nanowire-based CMOS technologies", S3S conference, 2015

A. Burenkov, J. Lorenz, Y. Spiegel, F. Torregrosa, Simulation of Plasma Immersion Ion Implantation into Silicon, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2015 (SISPAD 2015), p. 218 Download

L. Filipovic, A.P. Singulani, F. Roger, S. Carniello, S. Selberherr, Intrinsic Stress Analysis of Tungsten-lined open TSVs, Microelectr. Reliab. 55 (2015) 1843

L. Gaben, S. Barraud, M.-A. Jaud, S. Martinie, O. Rozeau, J. Lacord, G. Hiblot, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet, "Stacked-Nanowire and FinFET transistors: guideline for the 7nm node", SSDM conference, 2015

L. Gaben, S. Barraud, P. Pimenta-Barros, Y. Morand, J. Pradelles, M.-P. Samson, B. Previtali, P. Besson, F. Allain, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet, "Omega-Gate nanowire transistors realized by sidewall image transfer patterning: 35nm channel pitch and opportunities for stacked-Nanowires architectures", SSDM conference, 2015

R. Nagy, A. Burenkov, J. Lorenz, Numerical Evaluation of the ITRS Transistor Scaling, J. Comput. Electron. 14 (2015) 192

J. Pelloux-Prayer, M. Cassé, F. Triozon, S. Barraud, Y.-M. Niquet, J.-L. Rouvière, O. Faynot, G. Reimbold, "strain effect on mobility in nanowire MOSFETs down to 10nm width: geometrical effects and piezoresistive model", ESSDERC conference, 2015

F. Roger, A. Singulani, S. Carniello, L. Filipovic, S. Selberherr, Global Statistical Methodology for the Analysis of Equipment Parameter Effects on TSV Formation, in: Proceedings VARI Conference 2015, p. 39

L. Wang, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, A. Asenov, Impact of Self-Heating on the Statistical Variability in Bulk and SOI FinFETs, IEEE Trans. Electr. Dev. 62 (2015) 2106

L. Wang, T. Sadi, M. Nedjalkov, A. R. Brown, C. Alexander, B. Cheng, C. Millar, A. Asenov. An Advanced Electro-Thermal Simulation Methodology For Nanoscale Device, in: Proceedings of IEEE 2015 International Workshop on Computational Electronics (IWCE 2015), p. 1

L. Wang, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, A. Asenov, 3D Electro-Thermal Simulations of Bulk FinFETs with Statistical Variations, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2015 (SISPAD 2015), p. 112 Download

X. Wang, D. Reid, L. Wang, A. Burenkov, C. Millar, J. Lorenz, A. Asenov, Hierarchical Variability-Aware Compact Models of 20nm Bulk CMOS,in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2015 (SISPAD 2015), p. 325 Download

2014

S.M. Amoroso, L. Gerrer, M. Nedjalkov, R. Hussin, C. Alexander, A. Asenov, Modeling Carrier Mobility in Nano-MOSFETs in the Presence of Discrete Trapped Charges: Accuracy and Issues, IEEE Trans. Electr. Dev. 61 (2014) 1292

A. Burenkov, J. Lorenz, Y. Spiegel, F. Torregrosa, Simulation of AsH3 Plasma Immersion Ion Implantation into Silicon, in: Proceedings International Conference on Ion Implantation Technology (IIT) 2014

L. Filipovic, R.L. de Orio, S. Selberherr, Effects of Sidewall Scallops on the Performance and Reliability of Filled Copper and Open Tungsten TSVs, in: Proc. IEEE 21st International Symposium on the Physical and Failure Analysis of Integrated Ciruits (IPFA) 2014, p. 321

L. Filipovic, R.L. de Orio, S. Selberherr, A. Singulani, F. Roger, R. Minixhofer, Effects of Sidewall Scallops on Open Tungsten TSVs, Proceedings International Relaibility Physics Symposium (IRPS) 2014

L. Filipovic, R.L. de Orio, S. Selberherr, Process and Reliability of SF6/O2 Plasma Etched Copper TSVs, Proceedings EuroSimE 2014

L. Filipovic, F. Rudolf, E. Baer, P. Evanschitzky, J. Lorenz, F. Roger, A. Singulani, R. Minixhofer, S. Selberherr, Three-Dimensional Simulation for the Reliability and Electrical Performance of Through-Silicon Vias, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2014 (SISPAD 2014), p. 341 Download

L. Filipovic, S. Selberherr, The Effects of Etching and Deposition on the Performance and Stress Evolution of Open Through Silicon Vias, Microelectr. Reliab. 54 (2014) 1953

J. Lorenz, E. Bär, A. Burenkov, P. Evanschitzky, A. Asenov, L. Wang, X. Wang, A.R. Brown, C. Millar, D. Reid, Simultaneous Simulation of Systematic and Stochastic Process Variations, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2014 (SISPAD 2014), p. 289 Download

P. Nguyen, S. Barraud, C. Tabone, L. Gaben, M. Cassé, F. Glowacki, J.-M. Hartmann, M.-P. Samson, V. Maffini-Alvaro, C. Vizioz, N. Bernier, C. Guedj, C. Mounet, O. Rozeau, A. Toffoli, F. Alain, D. Delprat, B. Y. Nguyen, C. Mazuré, O. Faynot, M. Vinet, "Dual-Channel CMOS Co-Integration with Si NFET and Strained-SiGe PFET in Nanowire Device Architecture Featuring Sub-15nm Gate Length", IEDM conference, 2014

J. Pelloux-Prayer, M. Cassé, S. Barraud, P. Nguyen, M. Koyama, Y.-M. Niquet, F. Triozon, I. Duchemin, A. Abisset, A. Idrissi-Eloudrhiri, S. Martinie, J.-L. Rouvière, H. Iwai, and G. Reimbold, "Study of the piezoresistive properties of NMOS and PMOS Omega-Gate SOI Nanowire transistors: scalability effects and high stress level", IEDM conference, 2014

L. Wang, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, A. Asenov, 3D Coupled Electro-Thermal Simulations for SOI FinFET with Statistical Variations Including the Fin Shape Dependence of the Thermal Conductivity, 2014 IEEE 12th International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2014), Guilin, China, Oct. 2014

L. Wang, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, A. Asenov, 3D Coupled Electro-Thermal FinFET Simulations Including the Fin Shape Dependence of the Thermal Conductivity, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2014 (SISPAD 2014), p. 269 Download

L. Wang, A.R. Brown, C. Millar, A. Burenkov, X. Wang, A. Asenov, J. Lorenz, Simulation for Statistical Variability in Realistic 20 nm MOSFET, in: Proceedings of the 15th International Conference on Ultimate Integration on Silicon (ULIS), 2014, p. 5

X. Wang, D. Reid, L. Wang, A. Burenkov, C. Millar, B. Cheng, A. Lange, J. Lorenz, E. Baer, A. Asenov, Variability-Aware Compact Model Strategy for 20-nm Bulk MOSFETs, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2014 (SISPAD 2014), p. 293 Download

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Date: 17.1.2019 14:51