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SUPERAID7

Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7nm Node

D6.5: Guide to Research Data Disseminated From SUPERAID7

	Name	Organisation	Date
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Contents

Abstract

This document summarizes and links to research data generated within the SUPERAID7 project which could be disseminated without compromising confidentiality issues or commercial interest of partners. Experimental data used in SUPERAID7 could only be included to a limited extent, because it mainly resulted from background or sideground work of project or cooperation partners. Therefore, data included mainly refers to physical models developed, their comparison with literature or other models, generic benchmark studies or variability studies. The dissemination of these data is based on a hierarchical access principle. Here, this document serves as the entry point and guide in which an inventory of the data generated and disseminated is given, together with a link to the detailed data, which were in most cases published in journals or conference proceedings, and made available Open Access.

1. Introduction

Within the SUPERAID7 a software system has been established for the simultaneous simulation of the impact of systematic and stochastic process variations on device and circuits. In order to efficiently achieve this goal, the project has been based on the integration of a limited set of software modules, enhanced or newly developed by the partners, with background software from partners and commercial tools. In order to benchmark and to demonstrate the software system developed, experimental data existing from background or sideground work with the involvement of the SUPERAID7 partner CEA/LETI has been re-used, because it was neither necessary nor feasible, within the resource and time limitations of the project, to carry out a significant number of new experiments. Therefore SUPERAID7 and/or its partners are in most cases not owners of the data used in the project.

Based on this, the data to be used in SUPERAID7 and the access to them were characterized in the SUPERAID7 proposal as follows:

"Data used in the project will

- *generally consist of measured process results, device or circuit characteristics;*
- *either be re-used from background or sideground work of partners, or*
- *be provided by members of the ISAB under non-disclosure conditions, or*
- *be extracted from the literature;*
- *the overall target is the comparison between simulation and experiment.*

Frequently beside confidentiality also the need-to-know principle will have to be applied.
In view of this

- *data will (if the restriction defined by the external owner allows) be stored in a repository on the internal SUPERAID7 WWW page, where it will only be accessible to the SUPERAID7 partners;*
- *related comparisons with simulations will also be stored there;*
- *limited distribution of selected original data but especially of results of the comparison between simulation and experiment will be made in scientific publications and/or to the ISAB."*

In consequence of that situation, during the proposal phase the consortium had opted out of the Open Research Data Pilot.

Later in the project, this additional deliverable D6.5 "Guide to Research Data Disseminated From SUPERAID7" was introduced following discussions between the EC and the consortium. The purpose of this new deliverable is described in the abstract given above. Its content was also defined in the Data Management Plan of SUPERAID7:

"Data will be selected for dissemination to the public based on the following criteria:

- *Dissemination must not be in conflict with confidentiality issues. In particular, this will exclude most or all experimental data obtained from background or sideground cooperations of partners.*
- *Among the data not blocked by confidentiality issues the consortium will choose the data which is considered most interesting to the public.*

Data to be disseminated will mainly consist of comparisons between simulation and experiments from literature, generic benchmark studies, or variability studies.
The main route for dissemination of data will be via scientific open access publications. Where appropriate and possible, supporting or more detailed data will be made available via the public WWW of SUPERAID7."

The access to the released research data has been organized via the public part of the SUPERAID7 WWW, which according to the Description of the Action will be kept up-to-date and accessible at least for three years after the end of the SUPERAID7 project, which means at least until the end of 2021. The following two chapters summarize which data are available, and where to find them at the SUPERAID7 WWW page.

2. Open Research Data linked to SUPERAID7 Publications

As foreseen in the Grant Agreement, all peer-reviewed publications from SUPERAID7 are accessible via Gold Open Access or at least via Green Open Access. They are accessible in the public section of the SUPERAID7 WWW, under the link https://www.superaid7.eu/en/project/publications.html . In total these are 40 publications. In the following, a list of these publications is given, together with the information *(in italics)* which kind of data linked to this publication is available via this WWW page, or why no data is available. Where appropriate, references to the related work packages (WPs) of SUPERAID7 are given.

Publications from 2016

[1] T. Al-Ameri, V. Georgiev, F.-A. Lema, T. Sadi, X. Wang, E. Towie, C. Riddet, C. Alexander, A. Asenov, Impact of Strain on the Performance of Si Nanowires Transistors at the Scaling Limit: A 3D Monte Carlo / 2D Poisson Schrodinger Simulation Study, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 213

This paper shows a background simulation based on 3D Monte Carlo that was used to validate the simulation methods developed in WP4.

[2] S. Barraud, V. Lapras, M.P. Samson, L. Gaben, L. Grenouillet, V. Maffini-Alvaro, Y. Morand, J. Daranlot, N. Rambal, B. Previtalli, S. Reboh, C. Tabone, R. Coguand, E. Augendre, O. Rozeau, J.M. Hartmann, C. Vizioz, C. Arvet, P. Pimenta-Barros, N. Posseme, V. Loup, C. Comboroure, C. Euvrard, V. Balan, I. Tinti, G. Audoit, N. Bernier, D. Cooper, Z. Saghi, F. Allain, A. Toffoli, O. Faynot, M. Vinet, Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain, in: Proceedings International Electron Devices Meeting (IEDM) 2016

This paper includes sideground data used for the validation of advanced simulation tools developed in WPs4/5/6.

[3] L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Casse, S. Barraud, S. Martinie, D. Rideau, Y. Niquet, High and Low-field Contact Resistances in Trigate Devices in a Non-Equilibrium Green´s Functions Framework, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 291

Comparison between NEGF simulation (WP4) and experimental data (sideground data from LETI)

[4] V.P. Georgiev, M.M. Mirza, A.-I. Dochioiu, F.-A. Lema, S.M. Amoroso, E. Towie, C. Riddet, D.A. MacLaren, A. Asenov, D.J. Paul, Experimental and Simulation Study of a High Current 1D Silicon Nanowire Transistor using Heavily Doped Channels, in: Proceedings of 2016 IEEE Nanotechnology Materials and Devices Conference (NMDC)

This paper shows comparison between simulation and experimental data from one of our collaborators in GU. This work is a side-ground for simulation methods developed in WP4.

[5] O. Rozeau, S. Martini, T. Poiroux, F. Triozon, S. Barraud, J. Lacord, Y.M. Niquet, C. Tabone, R. Coquand, E. Augendre, M. Vinet, O. Faynot, J.-Ch. Barbe, NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs, in: Proceedings International Electron Devices Meeting (IEDM) 2016

Description of compact model developed in WP5 and comparison with experimental data (sideground data from LETI).

[6] T. Sadi, E. Towie, M. Nedjalkov, C. Riddet, C. Alexander, L. Wang, V. Georgiev, A. Brown, C. Millar, A. Asenov, One-Dimensional Multi-Subband Monte Carlo Simulation of Charge Transport in Si Nanowire Transistors, in: Proceedings of 2016 Inter-

national Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 23

This paper shows our first results on 1D MS MC develop in WP4. No experimental data is used in this paper.

[7] L. Wang, B. Cheng, P. Asenov, A. Pender, D. Reid, F. Adamu-Lema, C. Millar, A. Asenov, TCAD Proven Compact Modelling Re-centering Technology for Early 0.x PDKs, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 157

Some experimental data from literature used, as cited therein.

[8] Z. Zeng, F. Triozon, Y. Niquet, S. Barraud, Size-dependent Carrier Mobilities in Rectangular Silicon Nanowire Devices, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 257

Description of carrier mobility model based on NEGF simulation developed in WP4.

[9] Z. Zeng, F. Triozon, Y. Niquet, Carrier Scattering by Workfunction Fluctuations and Interface Dipoles in high-κ/Metal Gate Stacks, in: Proceedings of 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2016), p. 369

Variability study based on NEGF simulation developed in WP4.

Publications from 2017

[10] T. Al-Ameri, V.P. Georgiev, F. Adamu-Lema, A. Asenov, Simulation Study of Vertically Stacked Lateral Si Nanowires Transistors for 5-nm CMOS Applications, J. Electron Dev. Soc. 5 (2017) 466

This paper describes preliminary simulation data which we obtained during developing the methods and algorithms in WP4. No experimental data is used from this project but we validated the result to experimental data from literature.

[11] T. Al-Ameri, V. Georgiev, F. Adamu-Lema, A. Asenov, Does a Nanowire Transistor Follow the Golden Ratio, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 57

Initial simulations work for 3D MC and DD which is linked to WP4. No experimental data is used in this paper.

[12] J.-C. Barbé, S. Barraud, O. Rozeau, S. Martinie, J. Lacord, P. Blaise, Z. Zeng, L. Bourdet, F. Triozon, Y. Niquet, Stacked Nanowires/Nanosheets GAA MOSFET From Technology to Design Enablement, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 5

Description of model developed in WP4 and WP5 in agreement with sideground data described in WP2.

[13] S. Barraud, V. Lapras, B. Previtali, M.P. Samson, J. Lacord, S. Martinie, M.A. Jaud, S. Athanasiou, F. Trizon, O. Rozeau, J.M. Hartmann, C. Vizioz, C. Comboroure, F. Andrieu, J.C. Barbe, M, Vinet, T. Ernst, Performance and Design Considerations for Gate-All-Around Stacked-NanoWires FETs, in: Proceedings International Electron Devices Meeting (IEDM) 2017

This paper includes sideground data used for the validation of advanced simulation tools developed in WP4/5/6.

[14] S. Barraud, V. Lapras, M. Samson, B. Previtali, J. Hartmann, N. Rambal, C. Vizioz, V. Loup, C. Comboroure, F. Triozon, N. Bernier, D. Cooper, M. Vinet, Stacked-Wires FETs for Advanced CMOS Scaling , Proceedings 2017 International Conference on Solid State Devices and Materials (SSDM 2017)

This paper includes sideground data used for the validation of advanced simulation tools developed in WP4/5/6.

[15] B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, New Method for Individual Electrical Characterization of Stacked SOI Nanowire MOSFETs, in: Proceedings 2017 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)

This paper includes sideground data used for the validation of advanced simulation tools developed in WP4/5/6.

[16] B. Cardoso Paz, M. Pavanello, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires, in: Proceedings 2017 Joint International EUROSOI-ULIS Workshop

This paper includes sideground data used for the validation of advanced simulation tools developed in WP4/5/6.

[17] P. Ellinghaus, M. Nedjalkov, J. Weinbub, S. Selberherr, Wigner Analysis of Surface Roughness in Quantum Wires, in: Book of Abstracts of the 2nd International Wigner Workshop (IW2), (2017), p. 40

Typical parameters used from literature cited.

[18] P. Ellinghaus, J. Weinbub, M. Nedjalkov, S. Selberherr, Analysis of Lense-governed Wigner Signed Particle Quantum Dynamics, Phys. Status Solidi RRL 11 (2017) 1700102:

Paper deals with software functionality. Therefore only generic data used.

[19] L. Filipovic, R.L. de Orio, W. Zisser, S. Selberherr, Modeling Electromigration in Nanoscaled Copper Interconnects, in: Proceedings of 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2017), p. 161

Typical parameters and geometries used from literature cited.

[20] V.P. Georgiev, M.M Mirza, A.-I. Dochioiu, F.-A. Lema, S.M. Amoroso, E. Towie, C. Riddet, D.A. MacLaren, A. Asenov, D.J. Paul, Experimental and simulation study of 1D silicon nanowire transistors using heavily doped channels, *IEEE Transactions on Nanotechnology*, 16(5), pp. 727-735.

This paper shows comparisons between simulation and experimental data from one of our collaborators in GU. This work is a side-ground for simulation methods developed in WP4.

[21] J. Weinbub, M. Nedjalkov, I. Dimov, S. Selberherr, Wigner-signed Particles Study of Double Dopant Quantum Effects, in: Book of Abstracts of the 2nd International Wigner Workshop (IW2), (2017), p. 50

Typical parameters used from literature cited.

[22] Z. Zeng, F. Triozon, S. Barraud, Y.-M. Niquet, A Simple Interpolation Model for the Carrier Mobility in Trigate and Gate-All-Around Silicon NWFETs, IEEE. Trans. Electr. Dev. 64 (2017) 2485

Description of carrier mobility model based on NEGF simulation developed in WP4.

Publications from 2018

[23] T. Al-Ameri, Correlation between the Golden Ratio and Nanowire Transistor Performance, Appl. Sci. 8 (2018) 54

Initial simulations work for 3D MC and DD which is linked to WP4. No experimental data is used in this paper and this paper is extension of paper [11].

[24] E. Baer, J. Lorenz, The Effect of Etching and Deposition Processes on the Width of Spacers Created during Self-Aligned Double Patterning, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 236

Typical parameters used in agreement with literature cited.

[25] Z. Belete, E. Baer, A. Erdmann, Modeling of Block Copolymer Dry Etching for Directed Self-Assembly Lithography, Proc. of SPIE 10589 (2018) 105890U

Models and data for calibration taken from literature as cited in paper.

[26] S. Berrada, J. Lee, H. Carillo-Nunes, C. Medina-Bailon, F. Adamu-Lema, V. Georgiev, A. Asenov, Quantum Transport Investigation of Threshold Voltage variability in Sub-10nm Junctionless Si Nanowire FETs, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 244

This work is based on the developed NEGF solver in task 4.1.3 in WP4. No experimental data is used from this project but our work is validated by comparison to existing literature results.

[27] B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, Electrical Characterization of Vertically Stacked p-FET SOI Nanowires, Solid-State Electronics 141 (2018) 84

This paper includes sideground data used for the validation of advanced simulation tools developed in WP4/5/6.

[28] B. Cardoso Paz, M. Casse, S. Barraud, G. Reimbold, M. Vinet, O. Faynot, M. Pavanello, Methodology to Separate Channel Conductions of Two Level Vertically Stacked SOI Nanowire MOSFETs, Solid-State Electronics 149 (2018) 62

This paper includes sideground data used for the validation of advanced simulation tools developed in WP4/5/6.

[29] L. Filipovic, R.L. de Orio, Modeling the Influence of Grains and Material Interfaces on Electromigration, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 83

Typical parameters and geometries used from literature cited.

[30] X. Klemenschits, S. Selberherr, L. Filipovic, Unified Feature Scale Model for Etching in SF_6 and Cl Plasma Chemistries, in: Proceedings 2018 Joint International EUROSOI-ULIS Workshop

Mainly generic data and parameters used. Process models from literature as cited.

[31] X. Klemenschits, S. Selberherr, L. Filipovic, Modeling of Gate Stack Patterning for Advanced Technology Nodes: A Review, Micromachines 12 (2018) 631

Review paper, where all data is from literature as cited.

[32] J. Lee, S. Berrada, H. Carillo-Nunez, C. Medina-Bailon, F. Adamu-Lema, V. Georgiev, A. Asenov, The Impact of Dopant Diffusion on Random Dopant Fluctuation in Si nanowire FETs: A Quantum Transport Study, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 280

This work is based on the developed NEGF solver in task 4.1.3 in WP4. No experimental data is used from this project. We used parameters and geometry from existing literature data.

[33] J. Lee, O. Badami, H. Carrillo-Nunez, S. Berrada, C. Medina-Bailon, T. Dutta, F. Adamu-Lema, V. P. Georgiev, A. Asenov, Variability predictions for the next technology generations of n-type SixGe1-x nanowire MOSFETs. *Micromachines*, 9(12), 643.

This work describes variability in nanowires in SiGe allows based on the developed NEGF solver in task 4.1.3 in WP4. We used parameters and geometry from existing literature data.

[34] J.K. Lorenz, A. Asenov, E. Bär, S. Barraud, C. Millar, M. Nedjalkov, Process Variability for Devices at and beyond the 7 nm Node, in: Proceedings of the 18th Symposium on Advanced CMOS-Compatible Semiconductor Devices, Ed. J.A. Martino, J.P. Raskin, S. Selberherr, H. Ishii, F. Gamiz, B.Y. Nguyen, A. Yoshino, The Electrochemical Society, ECS Transactions 85-8, 2018, p. 113

Generic data used. TEM micrographs from literature as cited.

[35] J.K. Lorenz, A. Asenov, E. Bär, S. Barraud, F. Kluepfel, C. Millar, M. Nedjalkov, Process Variability for Devices at and beyond the 7 nm Node, ECS J. Solid State Science Technol. 7 (2018) P595

Mainly generic data used. Process flow and data for nanowire benchmark confidential, from background work.

[36] C. Medina-Bailon, T. Sadi, M. Nedjalkov, J. Lee, S. Berrada, H. Carillo-Nunez, V. Georgiev, S. Selberherr, A. Asenov, Study of the 1D Scattering Mechanisms´ Impact on the Mobility in Si Nanowire Transistors, in: Proceedings of EUROSOI-ULIS 2018, 2018, p. 17

This work shows the developed 1D MC approach in WP4 of SUPERAID7. Information from literature is used as input data.

[37] C. Medina-Bailon, T. Sadi, M. Nedjalkov, J. Lee, S. Berrada, H. Carillo-Nunez, V. Georgiev, S. Selberherr, A. Asenov, Impact of the Effective Mass on the Mobility in Si Nanowire Transistors, in: Proceedings of 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2018), p. 297

This work shows the developed 1D MC approach in SUPERAID7 in WP4. Background information is used from cited papers.

[38] M. Nedjalkov, P. Ellinghaus, J. Weinbub, T. Sadi, A. Asenov, I. Dimov, S. Selberherr, Stochastic Analysis of Surface Roughness Models in Quantum Wires, Comp. Phys. Comm. 228 (2018) 30

Paper deals with software functionality: Used data generic/from cited papers.

Publications from 2019

[39] J. Lorenz, E. Bär, S. Barraud, A.R. Brown, P. Evanschitzky, F. Klüpfel, L. Wang, Process Variability–Technological Challenge and Design Issue for Nanoscale Devices, Micromachines 1 (2019) 6

No experimental data except for TEM data from confidential process flow included.

[40] T. Sadi, C. Medina-Bailon, M. Nedjalkov, J. Lee, O. Badami, S. Berrada, H. Carillo-Nunez, V. Georgiev, S. Selberherr, A. Asenov, Simulation of the Impact of Ionized Impurity Scattering on the Total Mobility in Si Nanowire Transistors, Materials 12 (2019) 124

The paper reveals our latest progress and result in MC and KG methods development. The simulations are compared to other numerical methods and experimental data from literature.

Some further publications from SUPERAID7 will be made after the end of the project. Whereas they will still be added to the list in the SUPERAID7 WWW page, they can of course not be mentioned in this deliverable. The SUPERAID7 home page also mentions public events which were organized or co-organized by SUPERAID7, and which material is available from them.

3. Conclusions

The SUPERAID7 project focused on the development of a software system for the simulation of the impact of systematic and stochastic process variability on devices and circuits. For model development and benchmarking, largely data published before in the literature are used. The project results were published in a large number of Open Access papers, as listed in this deliverable and on the public WWW page of the SUPERAID7 project.