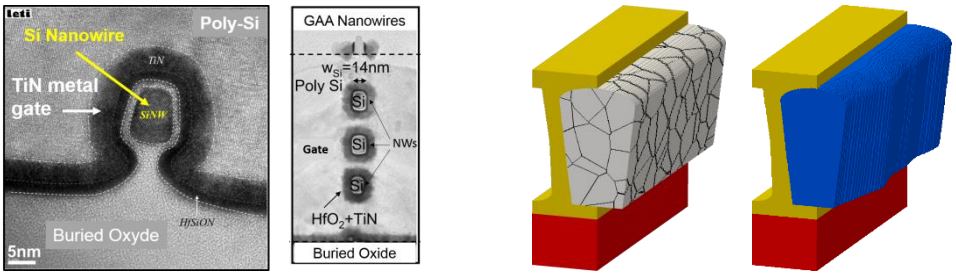
SUPERAID7 – STABILITY UNDER PROCESS VARIABILITY FOR ADVANCED INTERCONNECTS AND DEVICES BEYOND 7 NM NODE

Introduction

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled More Moore, process variability is getting ever more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Modelling and simulation (TCAD) offers the unique possibility to investigate the impact of process variations and trace their effects on subsequent process steps and on devices and circuits.

Within SUPERAID7 we:

- **establish a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits, down to the 7 nm node and below, including interconnects**
- **improve physical models and extend compact models**
- **study advanced device architectures such as tri-gate/Ω-gate nanowire transistors or stacked nanowires, including alternative channel materials**



(a) (b) (c) (d)

Examples for device architectures studied in the SUPERAID7 benchmarks
(a) Ω-gate nanowire transistor
(b) Stacked gate-all-around nanowires

Example for stochastic process variations which can introduce resistance variations in short range interconnects
(c) Copper granularity
(d) Line-edge roughness

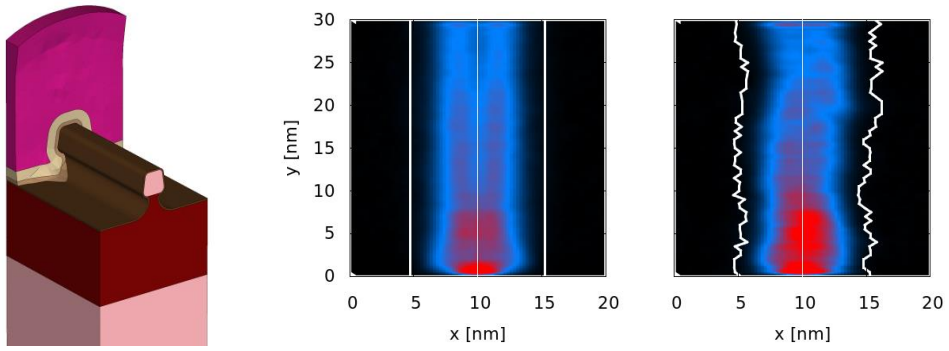
Work packages

The work package **"Specifications and Benchmarks"** is dedicated to the key features of the simulation system from the point of view of exploitation beyond the project. Specifications are defined for the 7 nm tri-gate and 5 nm stacked-nanowire technologies to be simulated. Morphological data and associated measured electrical characteristics for these devices are described in order to perform process and device simulations, and comparisons between experimental data and simulations are carried out.

In the work package **“Variation-aware Equipment and Process Simulation”** the work is focused on the integration of the topography modules from Fraunhofer IISB and TU Wien (lithography, etching, deposition) and on the development of physical models for topography steps. The latter is based on an analysis of the current capabilities of the modules and the resulting requirements for adaptations with respect to the SUPERAID7 benchmarks but also with respect to the needs of the simulation end-user community as a whole.

Within the work package **“Variation-aware Device and Interconnect Simulation”** a set of confined scattering models and a ballistic version of a non-equilibrium Green's function simulator have been developed. Ab-initio quantum simulations of surface roughness with realistic More-Moore device parameters obtained from CEA-Leti have been successfully completed. A prototype fast field solver has been developed that can be used to extract resistances and capacitances for advanced interconnect structures. This includes the capability to model global and statistical local variability due to line edge roughness and metal granularity.

The work package **“Software Integration and Variation-aware Compact Models”** focuses on the integration of the software modules for process, device, and interconnect simulation. Furthermore, compact models are developed, such as the predictive and physical compact model LETI-NSP for gate-all-around stacked nanowire/nanosheet MOSFETs.



(a) (b) (c)

(a) 3D process simulation of gate stack etching which is part of the sequence for the fabrication of the Ω-gate nanowire transistor shown in Figure (a) on the first page

Simulated electron density (red: high, blue: low) in ideal (b) and rough (c) wires: quantum repulsion keeps the density away from the boundaries

First results from SUPERAID7 have already been commercialized, including the integrated TCAD to SPICE DTCO (design technology co-optimization) flow made commercially available by Synopsys. Furthermore, the LETI-NSP compact model is being proposed for international standardization via the Compact Model Coalition (CMC) to allow the inclusion of LETI-NSP in all major ECAD (electronic computer-aided design) tools.

Partners

Fraunhofer IISB (Coordinator)
with Chair of Electron Devices, University of Erlangen-Nuremberg as Linked Third Party

Gold Standard Simulations, now part of Synopsys

CEA-Leti

University of Glasgow

TU Wien

Contact and further information

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