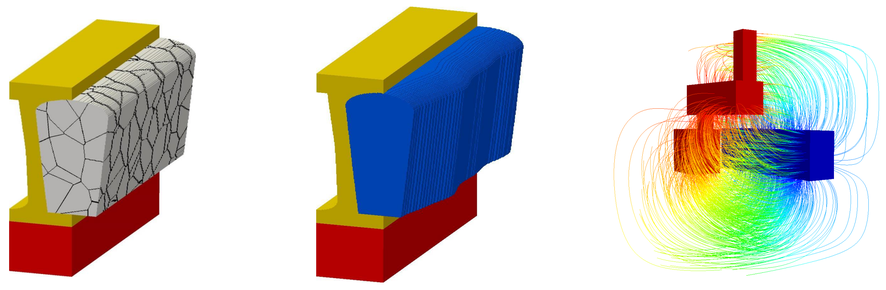
The project leading to this application has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 688101.

SUPERAID7

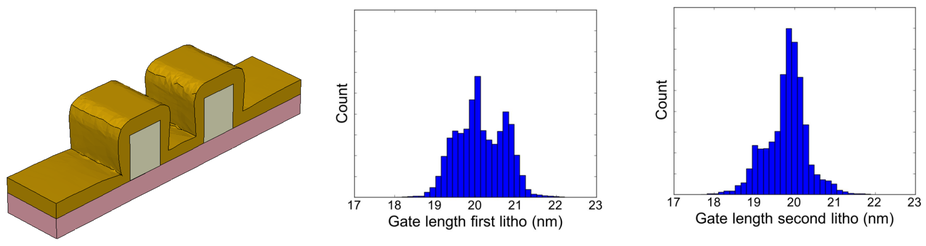
Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node

General description

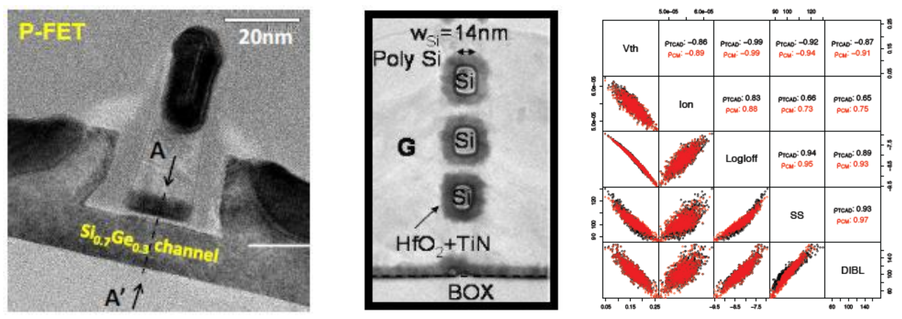
Modelling and simulation (TCAD) offer the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated. TCAD is a vital component for variability-aware Design-Technology Co-Optimization (DCTO), which is a key approach to optimize not only the performance but also the yield for aggressively scaled CMOS devices and circuits. SUPERAID7 builds upon the successful FP7 project SUPERTHEME which focused on advanced *More-than-Moore* devices, and establishes a software system for the simulation of the impact of systematic and statistical process variations on advanced *More Moore* devices and circuits down to the 7 nm node and below, including especially interconnects. This needs improved physical models and extended compact models. Device architectures addressed in the benchmarks include especially TriGate/ΩGate FETs and stacked nanowires, including alternative channel materials. The software developed is benchmarked utilizing background and sideground experiments of the partner CEA. Main channels for exploitation are software commercialization via the partner Synopsys and use in subsequent research projects at partners, including support of device architecture activities at CEA.



Left and middle: Examples for interconnect variability (copper granularity and line edge roughness; right: 3D interconnect electrical simulation (GSS)



Left: Self-aligned double patterning of fins (Fraunhofer IISB); litho-etch-litho-etch (LELE) patterning of gates: first (middle) and second (right) incremental lithography step (Fraunhofer IISB)



Trigate transistor (left) and stacked Gate-All-Around nanowires (middle) (both CEA/Leti) as examples for target structure; right: Example for local variability in statistical compact model (GSS)

Goals / Objectives

- Development of a software system for the simulation of the impact of systematical and statistical process variations for advanced extended CMOS devices and interconnects
- Close interaction with leading European technology development projects (esp. KET Pilot Lines) via partner CEA/Leti and some members of the SUPERAID7 Industrial and Scientific Advisory Board
- Continued attention on data reduction / hierarchical simulation – from discretization of equipment to compact models – and on correlations
- Specific focus on advanced integrated topography simulation, carrier transport models for nanowire transistors and/or alternative channel materials, interconnect modeling and simulation

Societal impact / Results

The software suite being developed in SUPERAID7 enables the assessment and minimization of the impact of process variations on advanced *extended CMOS* devices and circuits. This helps to optimize fabrication processes, device and circuit properties, and finally yield in semiconductor fabrication, and contributes to enabling further applications of micro and nanoelectronics.

Looking ahead

Future developments are planned in four main directions:

- Development of the variability-aware simulation ranging from equipment to circuit level
- Internal use of SUPERAID7 software at partners' sites for the development and optimization of equipment, processes, devices and circuits
- Demonstration of the software for DCTO applications
- Exploitation of the software developed via commercial offer of the SUPERAID7 partner Synopsys

Partners

- Fraunhofer IISB, Erlangen
- Gold Standard Simulations Ltd (GSS), Glasgow – now part of Synopsys
- CEA-Leti, Grenoble
- University of Glasgow
- Technische Universität Wien

Countries involved

- Germany
- Austria
- France
- United Kingdom

Additional information

More information is given at www.superaid7.eu

This includes among others

- Public deliverables, posters, information on software tools
- Currently 25 publications on SUPERAID7 results

SUPERAID 7

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Process Variations

- ❑ Systematic variation: Equipment-induced inhomogeneity of process results – e.g. variations of layer thickness across wafer, or from wafer to wafer
- ❑ Systematic variation: Uncertainties / drifts of equipment settings – e.g. distance between last lens and illuminated area in lithography
- ❑ Layout effects: Not only in lithography neighbouring features may influence each other. E.g.: Difference of inner and outer lines in SADP, temperature profiles in millisecond annealing influenced by local reflectivity
- ❑ Stochastic variations of process results due to granularity of matter – e.g. random dopant fluctuations (RDF)

Impact of Process Variations

- ❑ Process variations are propagated through the fabrication process
  ⇒ Variations of device performance (e.g. threshold voltage) and circuit properties (e.g. static noise margin) – reducing yield (Fig. 1)
- ❑ Same source of variation may influence different device and circuit data – e.g. channel length of one and channel width of another transistor
  ⇒ Correlations are essential and must be traced

Technologies Considered

- ❑ SUPERAID7 approach applicable to all advanced CMOS and interconnect technologies – both *More Moore* and *More than Moore*
- ❑ Project especially addresses additional requirements of 7 nm node and beyond – e.g. three-dimensional architectures, quantum effects

Examples for Results

- ❑ Integrated three-dimensional topography simulator (lithography/ etching/deposition), interfaced to external equipment simulation and to SENTAURUS software suite (Figs. 2 & 3)
  ⇒ Study of correlations introduced by multipatterning steps
- ❑ Accurate and efficient models for carrier transport in nanoscale devices, including quantum effects (Fig. 4)
  ⇒ Enabling statistical device simulation for nanoscale transistors
- ❑ Prototype tool for 3D interconnect variability simulation
  ⇒ Inclusion of interconnect performance into variability studies
- ❑ New compact model LETI-NSP for three-dimensional transistors such as FinFETs and nanowires
- ❑ Extended hierarchical approach to extract variation- and correlation aware compact models (Fig. 5)
- ❑ Enables extraction of compact models which simultaneously include systematic, layout-induced, and statistical variations (Fig. 6)

Some Highlights

Events organized by SUPERAID7

- SISPAD 2016 Workshop WS1 "Simulation of Advanced Interconnects" (co-organized with H2020 project CONNECT), Nuremberg, Germany, Sept. 5, 2016
- SISPAD 2016 Workshop WS3 "Variability-Aware Design Technology Co-Optimization" (co-organized with FP7 projects SUPERTHEME and MoRV), Nuremberg, Germany, Sept. 5, 2016
- ESSDERC 2018 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts", Dresden, Germany, Sept. 3, 2018

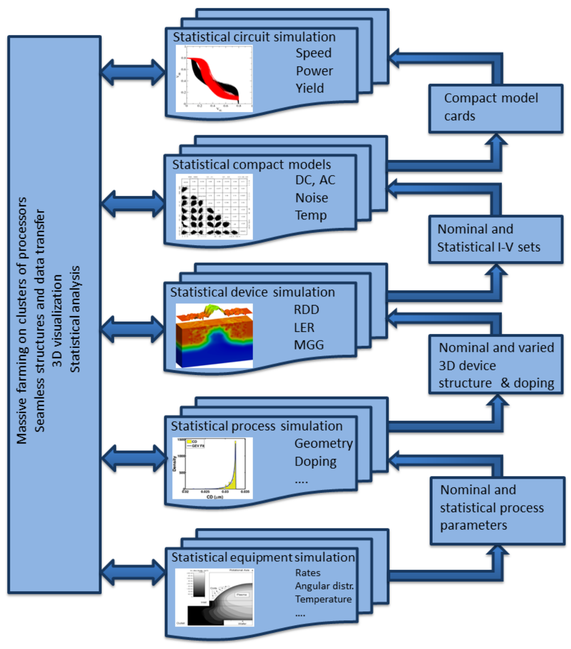

Fig. 1: Impacts of variations to be considered at various levels of simulation.

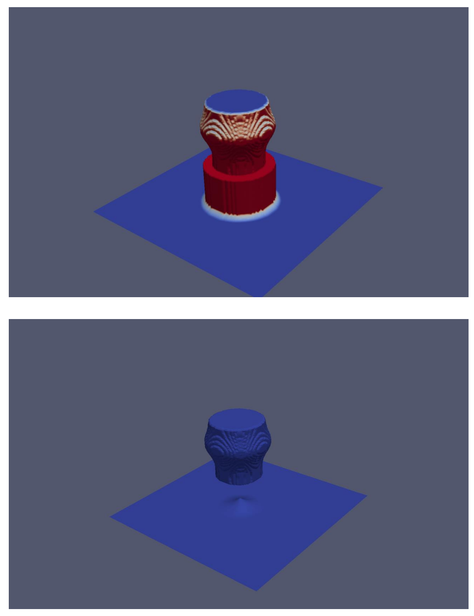

Fig. 2: Example for integrated topography simulation (lithography and etching): Influence of real resist shape on directional (top) and isotropic (bottom) etch process

Fig. 3: 3D process simulation of gate stack etching for the fabrication of an Ω-gate nanowire transistor

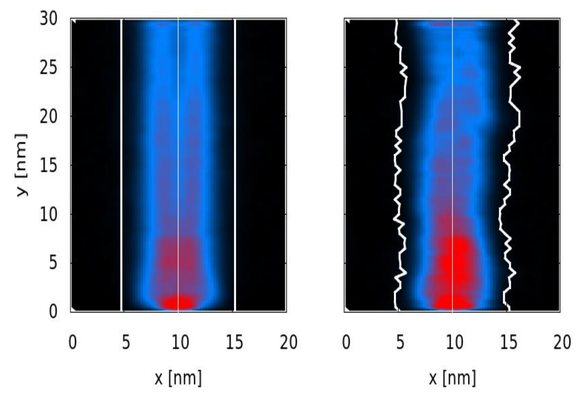

Fig. 4: Simulated electron density (red: high, blue: low) in ideal (b) and rough (c) wires: quantum repulsion keeps the density away from the boundaries

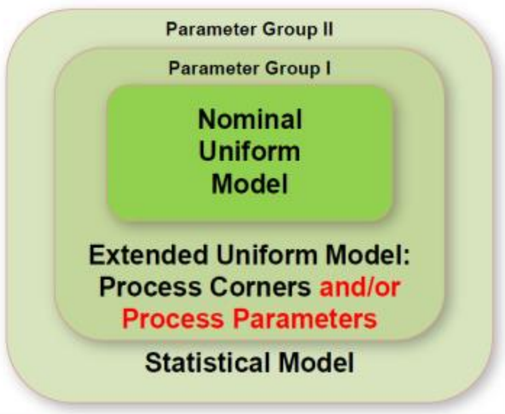

Fig. 5: Extraction and generation of hierarchical compact model aware of systematic and statistical process variations

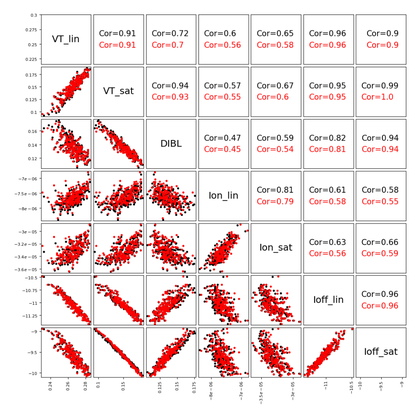

Fig. 6: Statistical model fitting results for nMOS nanowire devices (black: TCAD results; red: compact model results) in process DoE (at xGeFin=0.303, FinSpDepoFactor=1.01, GateFocusVar= 0.04)

Conference presentations

SUPERAID7 so far made 19 presentations at key international conferences such as ECS, EUROSOI-ULIS, IEDM, SISPAD and SPIE. This has included 3 invited presentations:

- J.-Ch. Barbe et al., Stacked Nanowires/Nanosheets GAA MOSFET From Technology to Design Enablement, SISPAD 2017, Sept. 7 to 9, Kamakura, Japan
- S. Barraud et al., Performance and Design Considerations for Gate-All-around Stacked-NanoWires FETs, IEDM 2017, Dec. 2-6, San Francisco, CA, USA
- J. Lorenz et al., Process Variability for Devices at and beyond the 7 nm Node, 233rd ECS Meeting, May 13-17, 2018, Seattle, WA, USA

Partners

Fraunhofer IISB · leti CEA tech · University of Glasgow · IμE · SYNOPSYS® Silicon to Software™

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