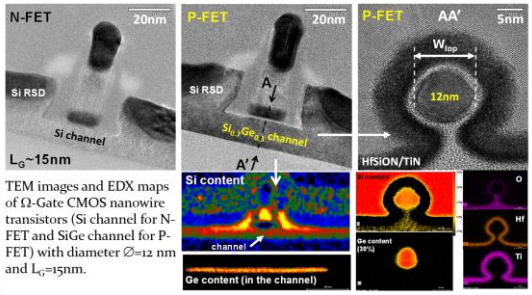
SUPERAID 7

Horizon 2020 Project SUPERAID7
Summary for Publication of the Report for Project Year 1 (2016)

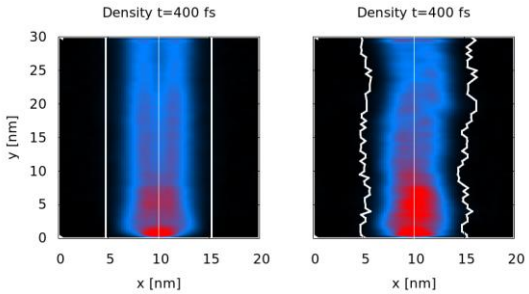
Figures and captions added at the Participant Portal:



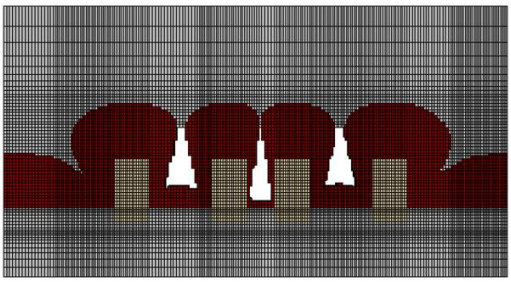
TEM images and EDX maps of Ω-Gate CMOS nanowire transistors (Si channel for N-FET and SiGe channel for P-FET) with diameter ∅=12 nm and L_G=15nm.

The Ge content is estimated to be 30% (using semi-quantitative EDX approach)

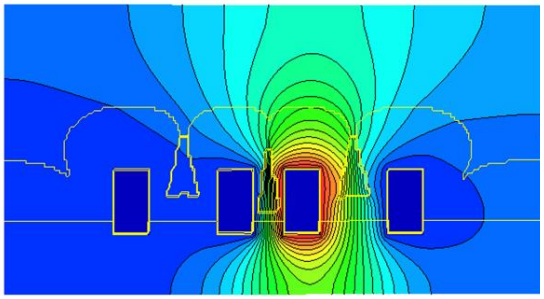
Example for nanowire devices used by CEA in SUPERAID7 (CEA)



Electron density in ideal and rough wires (TU Wien)



M3-level interconnect structure: (a) as imported from WP3 tools (Fraunhofer and GSS)



M3-level interconnect structure: Electrostatic potential solution (GSS)

A1.1 Summary of the context and overall objectives of the project

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled More Moore, process variability is getting ever more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data. This important requirement for and capability of simulation is among others highlighted in the International Technology Roadmap for Semiconductors ITRS.

SUPERAID7 builds upon the successful FP7 project SUPERTHEME which focused on advanced More-than-Moore devices, and establishes a software system for the simulation of the impact of systematic and

statistical process variations on advanced More Moore devices and circuits down to the 7 nm node and below, including especially interconnects. This needs improved physical models and extended compact models. Device architectures addressed in the benchmarks include especially TriGate/ΩGate FETs and stacked nanowires, including alternative channel materials. The software developed will be benchmarked utilizing background and sideground experiments of the partner CEA. Main channels for exploitation will be software commercialization via the partner GSS and support of device architecture activities at CEA. Furthermore, an Industrial Advisory Board initially consisting of GLOBALFOUNDRIES and STMicroelectronics will contribute to the specifications and will get early access to the project results.

A1.2 Work performed from the beginning of the project to the end of the period covered by the report and main results achieved so far

Within WP1 “Project Management” standard management actions were carried out, including the organization of the interactions with internal and external partners, of internal procedures for optimizing the work and the quality of documents, and of dissemination actions like the SUPERAID7 WWW and participation in conferences and in two events organized or co-organized by the EC.

The first 12 months of WP2 “Specifications and Benchmarks” were dedicated to the key features of the simulation system from the point of view of exploitation beyond the project, the definition and specifications of 7nm Trigate (FinFET) technology to be simulated, and the collection of morphological data and associated measured electrical characteristics for these devices in order to perform process and device simulation in WP3/WP4.

The work of WP3 “Variation-Aware Equipment and Process Simulation” was focused on the integration of the topography modules from Fraunhofer IISB and TU Wien (lithography, etching, deposition) and on the development of physical models for topography steps. The latter is based on an analysis of the current capabilities of the modules and the resulting requirements for adaptations with respect to the SUPERAID7 benchmarks but also with respect to needs from the simulation end-user community as a whole.

In WP4 “Variation-Aware Device and Interconnect Simulation” a set of confined scattering models and a ballistic version of a Non-Equilibrium Green's Function Simulator have been developed. Ab-initio quantum simulations of surface roughness with realistic More-Moore device parameters obtained from CEA-LETI has been successfully completed. In task 4.2 we have developed a fast field solver that can be used to extract resistance and capacitance from advanced interconnect structures. This includes the capability to model global and statistical local variability due to line edge roughness and metal granularity.

Within WP5 “Software Integration and Variation-Aware Compact Models”, the integration of the GSS interconnect simulator with output from the WP3 topography tools has been achieved. GSS develops a compact model for advanced interconnects, and has tested their SPICE model extraction on a representative 14nm FinFET technology. Results show excellent agreement with original TCAD data. CEA-LETI developed a SPICE model for sub-7nm 3D MOSFET architectures like FinFET and Stacked-Nanowire/Nanosheet GAA MOSFET.

Within WP6 “Dissemination” in the reporting period primarily the SUPERAID7 WWW page has been set up, which consists of a public, a restricted a confidential and an internal section. Besides this several papers on results from SUPERAID7 were already published, and presentations made at SISPAD 2016 and

IEDM 2016, and also a poster presented at the European Nanoelectronics Forum held in November 2016 in Rome.

WP7 “Exploitation” will only formally start at the beginning of the second year of the project. Nevertheless the commercialization of first results from SUPERAID7 has already started.

A1.3 Progress beyond the state of the art, expected results until the end of the project and potential impacts

(including the socio-economic impact and the wider societal implications of the project so far)

In the following the progress and expected results are outlined for the four technical work packages WP2 to WP5.

The results obtained in WP2 during the first year of the project summarize, for the first time, a very detailed database on morphological/electrical results of Trigate nanowire (NW) devices including a wide range of NW width, height and transport orientation. Moreover, the electron and hole transport is described for both unstrained and (tensile/compressive) strain Si and SiGe channels. In the second part of this project, this work will be extended to gate-all-around stacked nanowires devices including inner spacers and SiGe source-drain (S/D) stressors.

The current set of SUPERAID7 topography modules developed and improved in WP3 “Variation-Aware Equipment and Process Simulation” allows the simulation of integrated topography process sequences using various levels of physical modeling for all steps involved, that is, lithography, etching, and deposition. The possibility to simulate all topography steps in an integrated environment and to provide the structures to device and interconnect simulation is – to our knowledge – beyond state-of-the-art. Within WP4, a 1D multi-subband simulator based on novel transport models accounting for quantum effects of confinement is the central entity of task 4.1. Models being developed for this also include parameters obtained from first-principle confinement-aware simulations (DFT) of the band structure, enabling a more efficient description of scattering. The interconnect simulator being developed in task 4.2 will allow the effects of global and statistical local variability in interconnects to be extracted and used for a complete analysis of the effects of the combined variability on circuit performance. The reliability of novel interconnect geometries (task4.4) will be analyzed using state-of-the-art models for the process-induced and electromigration-induced stresses. Within WP5 a fully integrated tool flow has been developed by GSS. The integration of the tool flow with Synopsys Sentaurus Workbench (SWB) will be improved and used to generate a full design-technology co-optimisation (DTCO) flow with devices based on the design of CEA-Leti in WP2. Realistic interconnects for this technology will be included through the GSS interconnect simulator. Full global and local statistical variability in devices and interconnects will be included through to circuit simulation.