Variability aware simulations of nano-scale devices

Dr. Vihar Georgiev, University of Glasgow, Glasgow, UK

ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

University of Glasgow

SUPERAID 7

Outline

- Introduction
  - Project flow and link between the Work Packages
- Long range, short range and statistical variability
- Time-dependent variability
- Statistical variability example
- Conclusions and outlook

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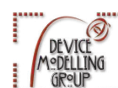
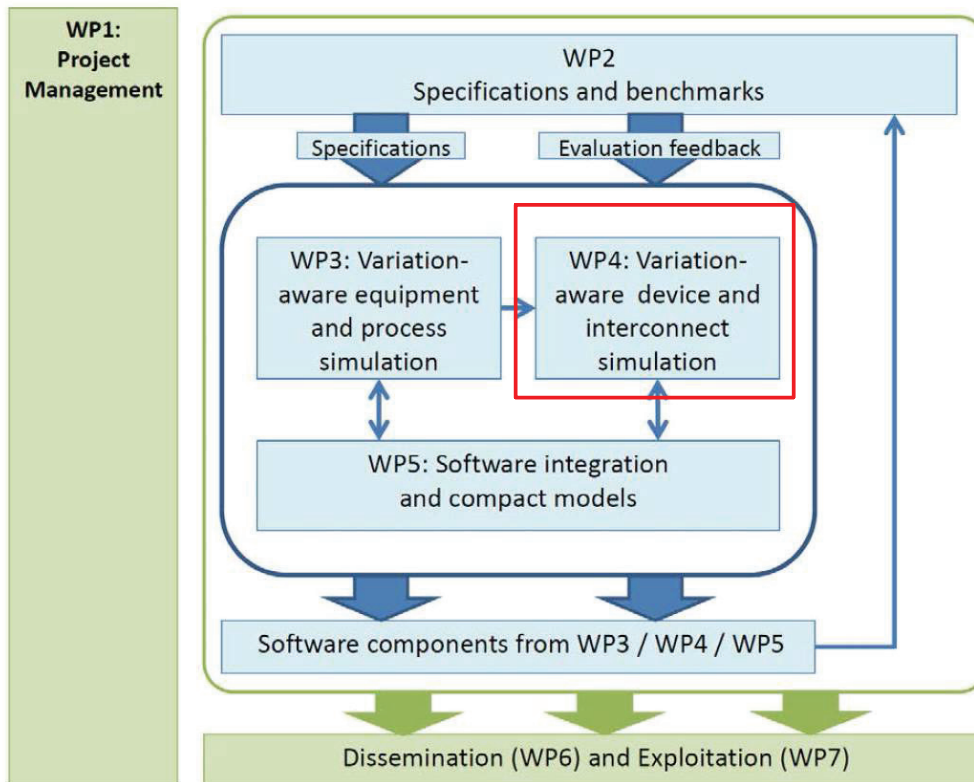


SUPERAID 7

Introduction – project context



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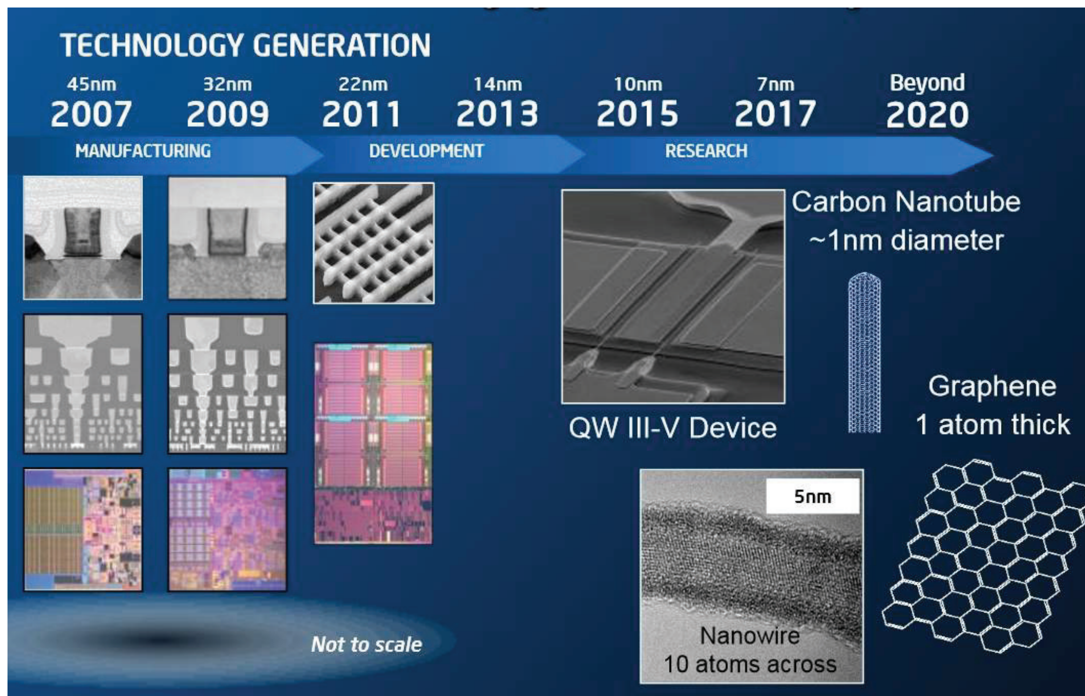
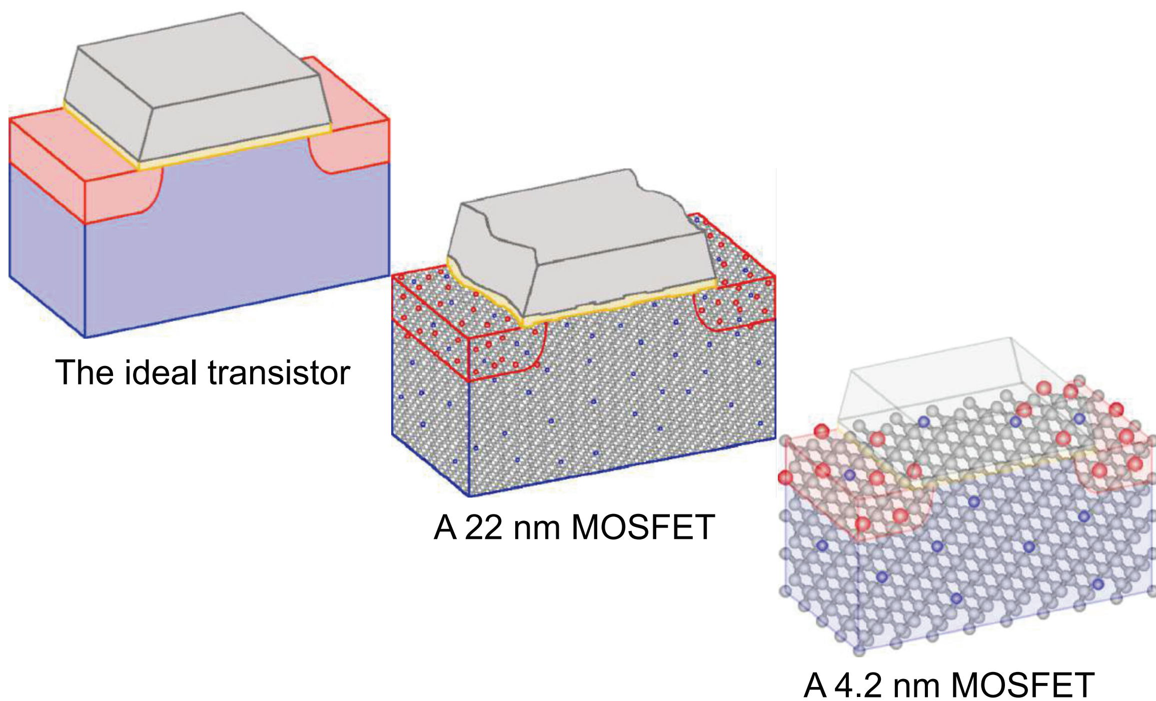
Saturation in performance and increasing variability drives the CMOS innovations



Intel, ISSCC

Statistical variability



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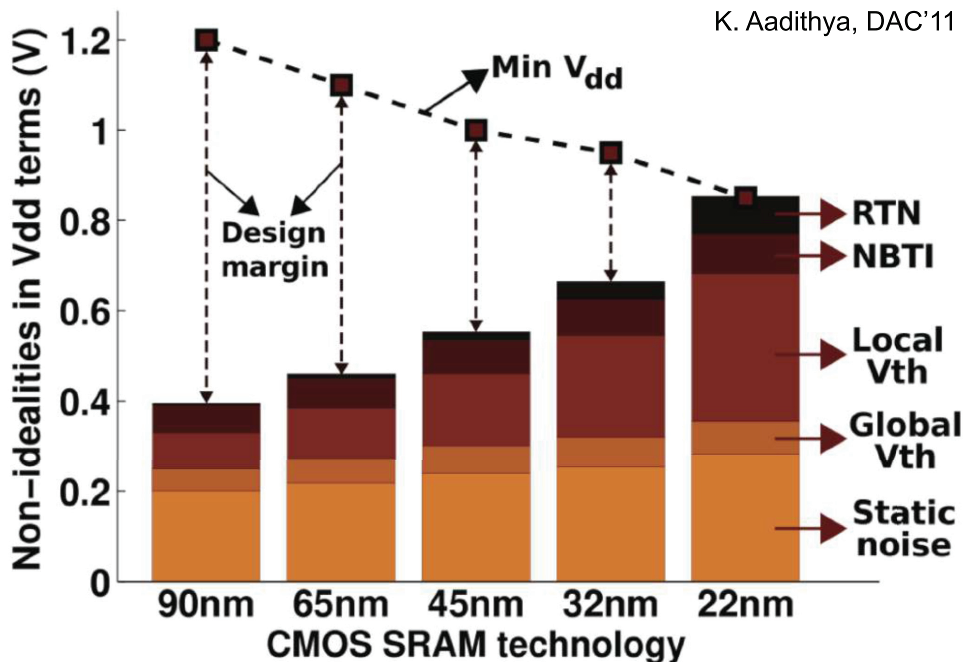
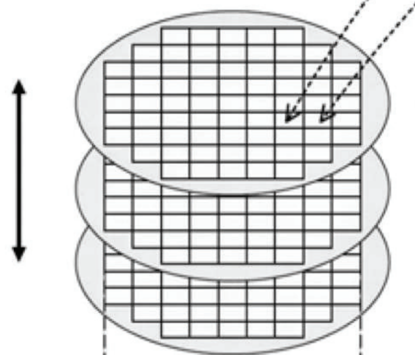
Variability is one of the major challenges associated with scaling

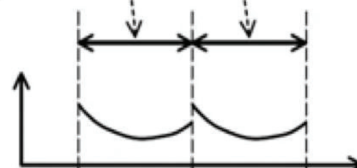


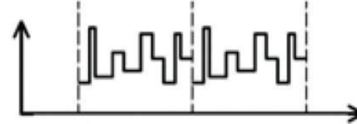
Variability results in higher parametric yield losses

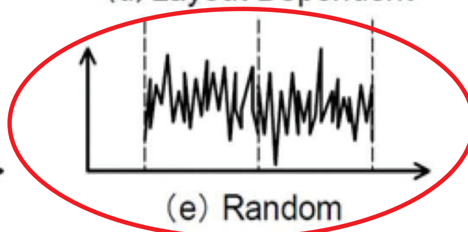
Variability classification

After K. Takeuchi (NEC)





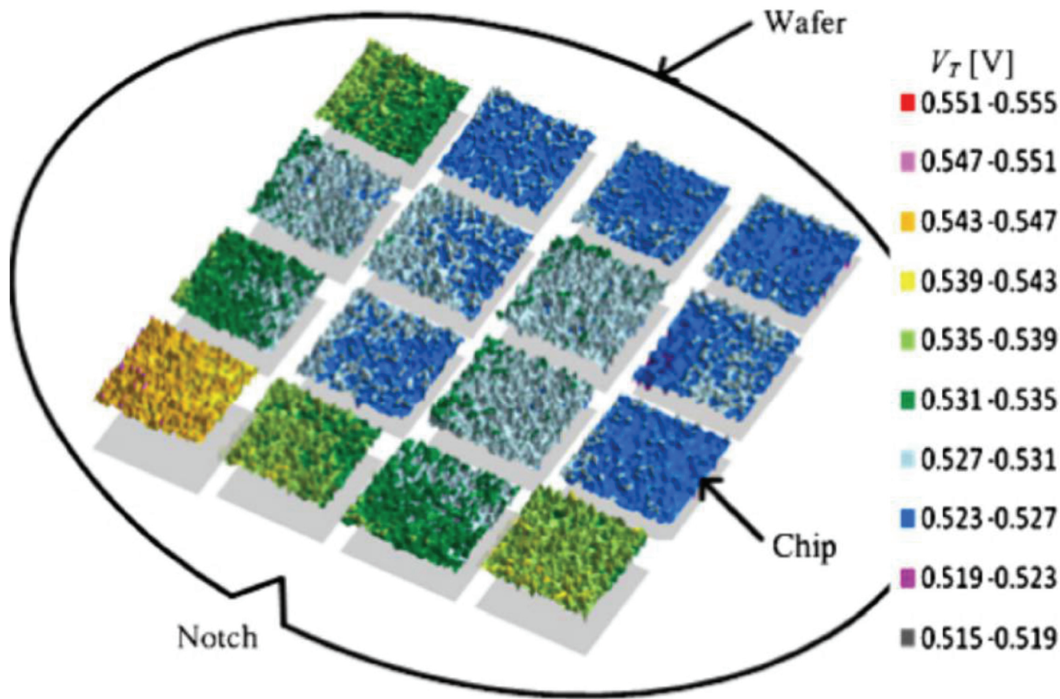




Global – Local
Systematic – Statistical

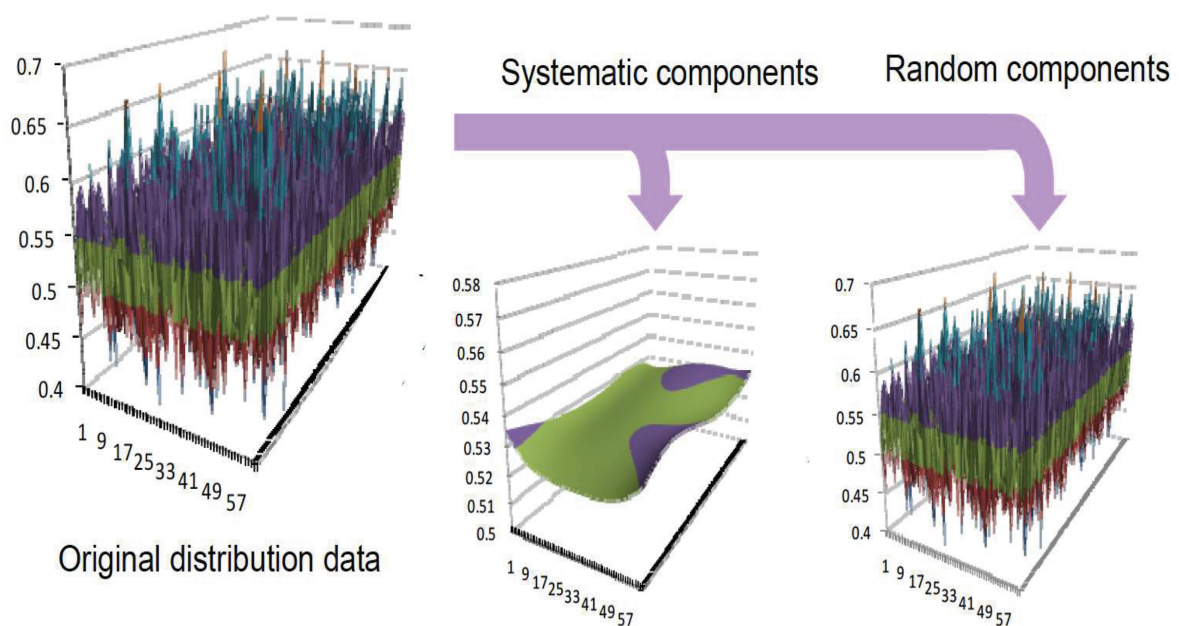
Wafer to wafer
Across the wafer
Across the chip

Variability in 65 nm (L=60 nm, W=140 nm)



T. Hiramoto (Tokyo Univ)

Variability in 65 nm (L=60 nm, W=140 nm)



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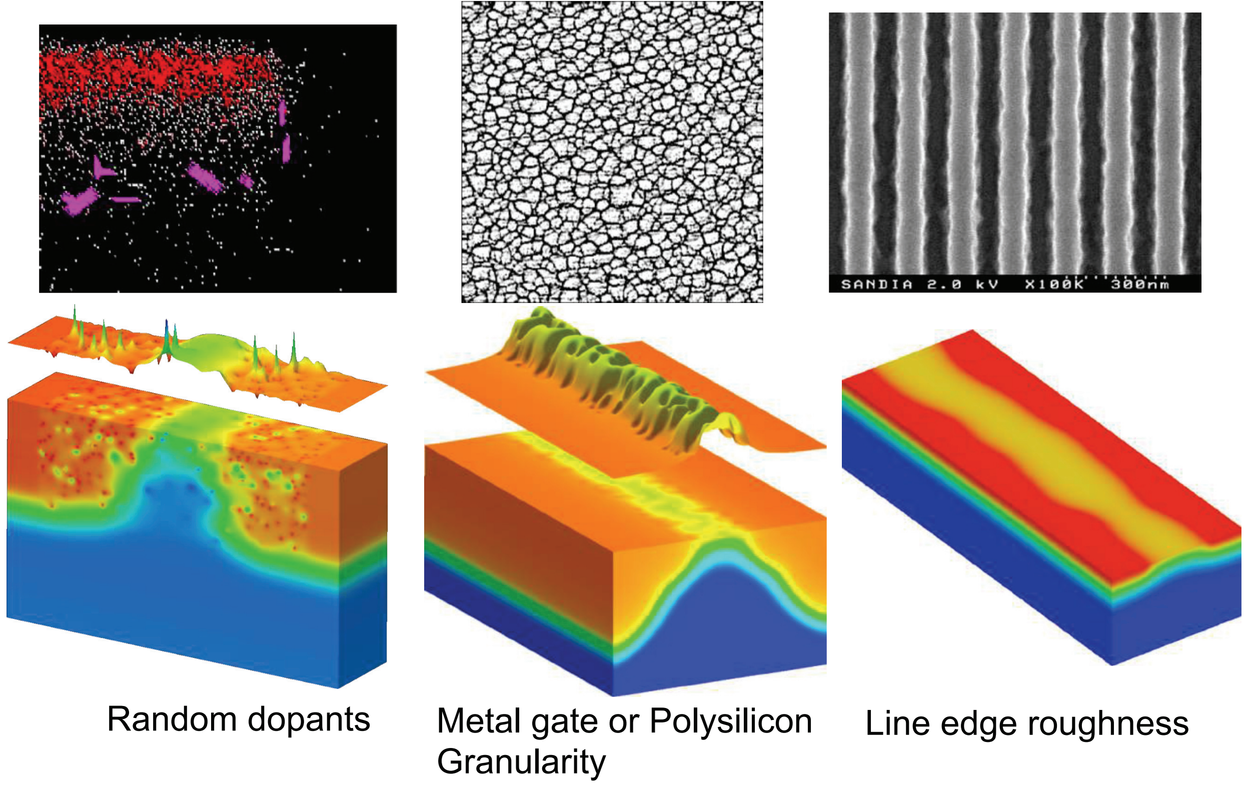
Sources of statistical variability

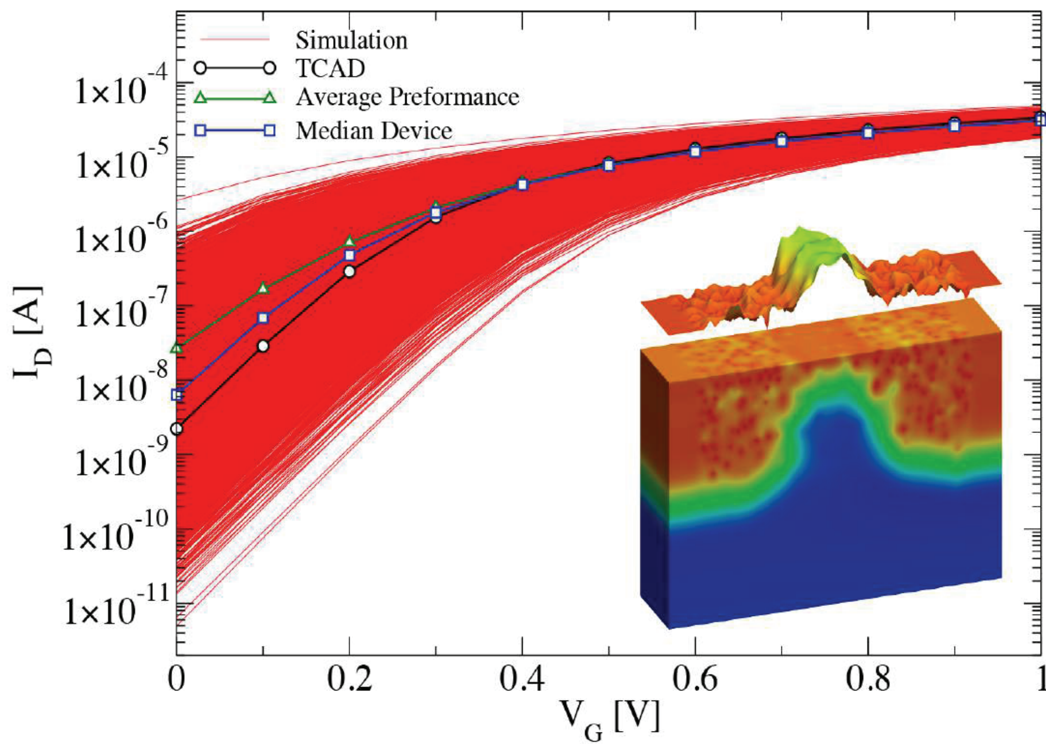


Random dopants

Metal gate or Polysilicon Granularity

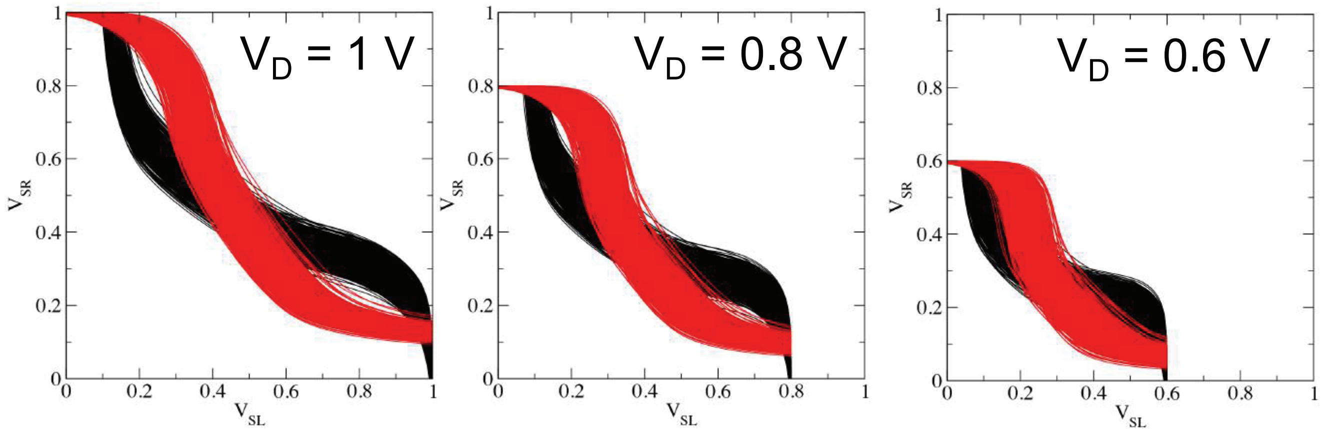
Line edge roughness

Variability in 20 nm CMOS



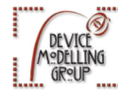
Statistical variability fuels the power crisis

The SRAM yield depends critically on supply voltage



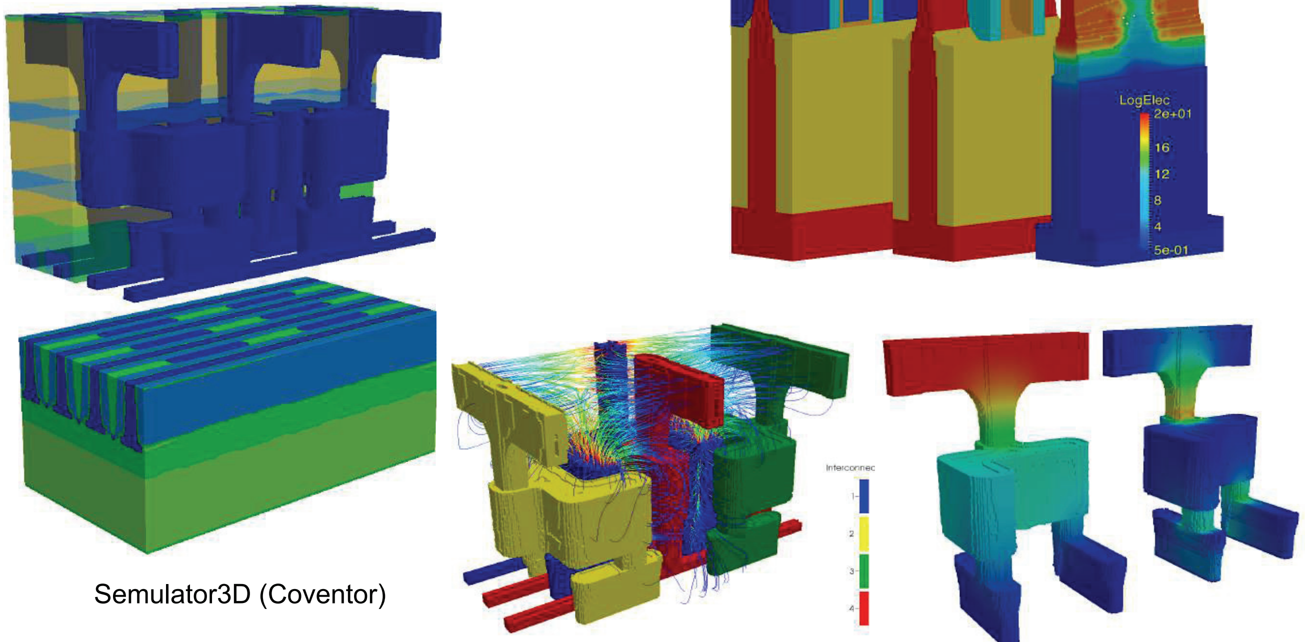
20nm SRAM butterfly curves as a function of V_{DD}

The butterfly eye is closing rapidly with the reduction of the supply voltage. This keeps the system on chip (SoC) supply voltage high increasing the dynamic power.

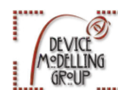


Both transistor and interconnect variability need to be considered

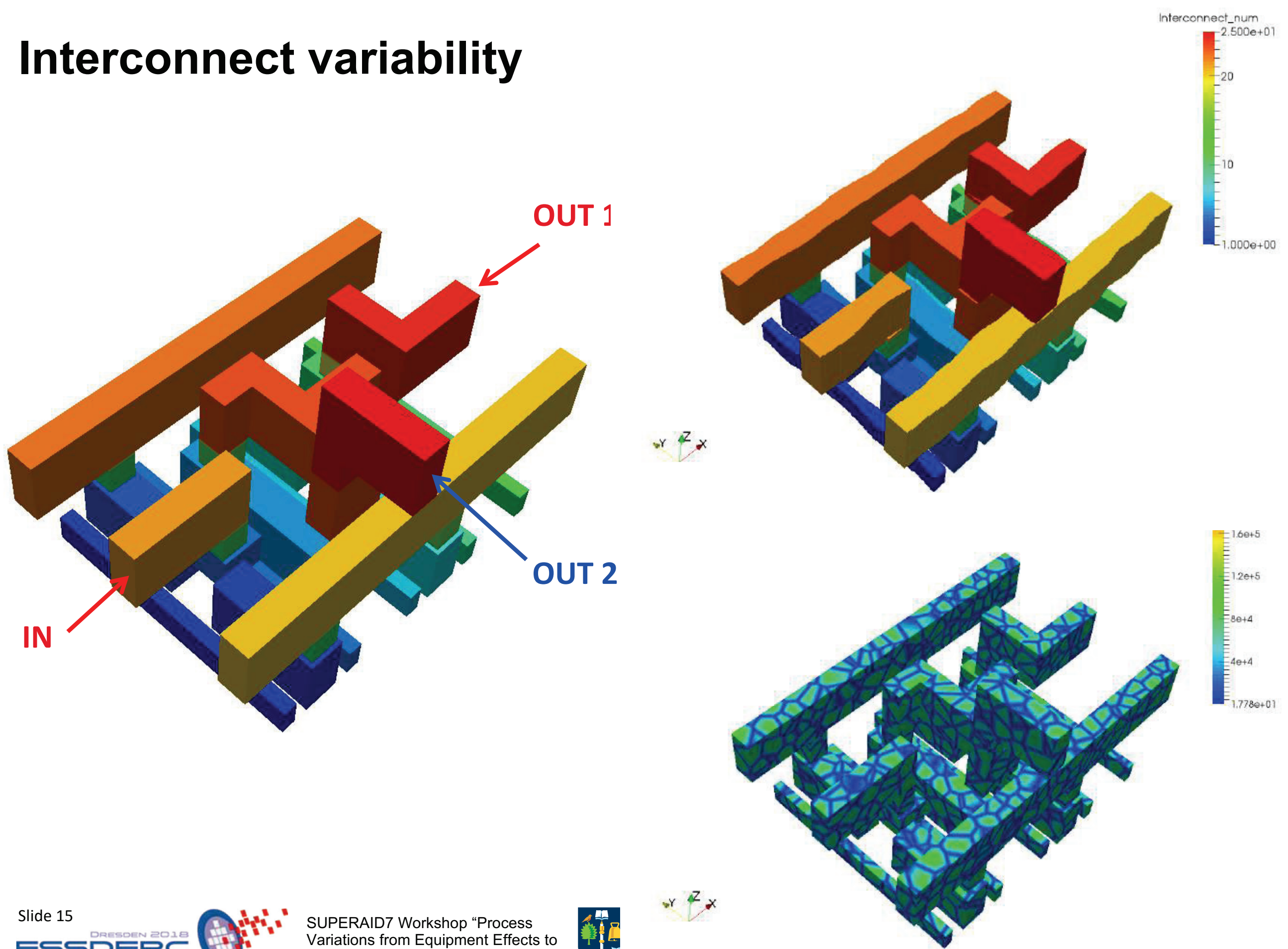
Emulation of Intel 14 nm FinFET CMOS



Semulator3D (Coventor)



Interconnect variability



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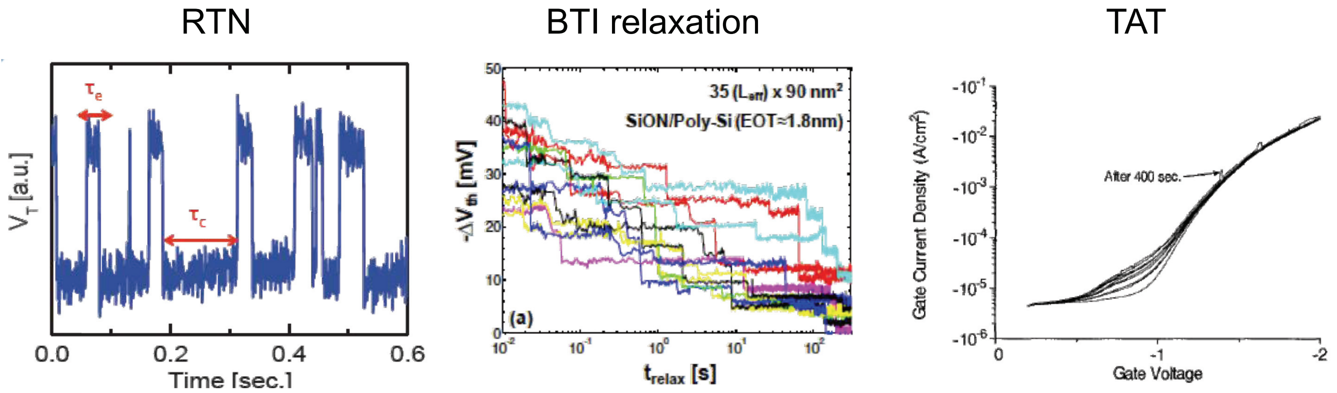
Time-dependent variability

- Random Telegraph Noise (**RTN**)
- Bias Temperature Instability (**BTI**)
- Trap Assisted Tunneling (**TAT**)
- Hot carrier injection (**HCI**)



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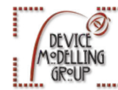
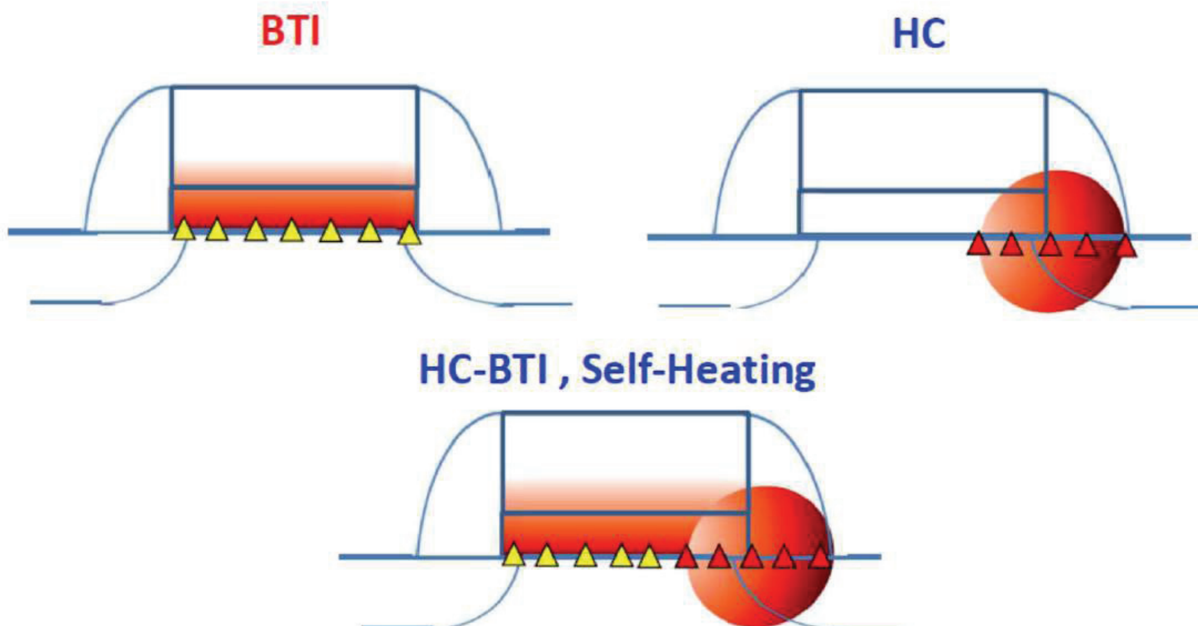


BTI vs HCI

BTI – uniform trap distribution and charge trapping
HCI – non-uniform trap distribution and charge trapping



A. Bravaix

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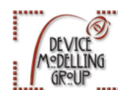
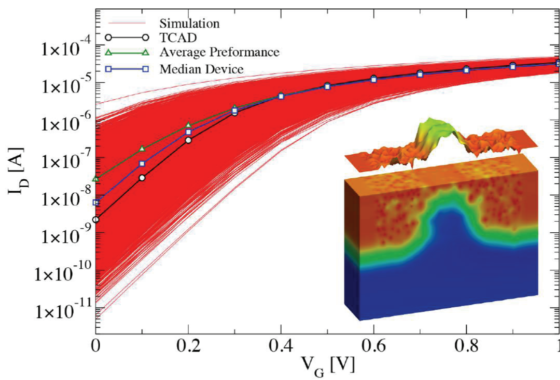
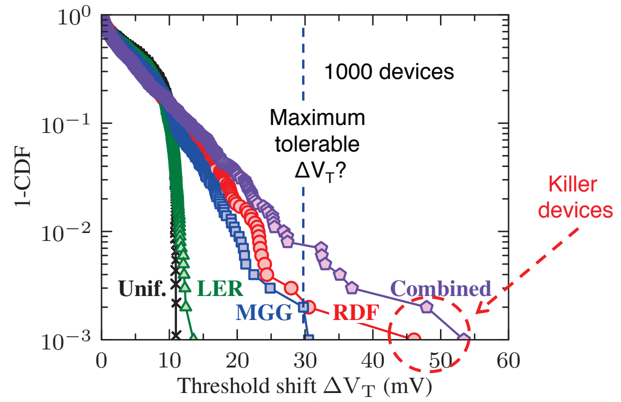
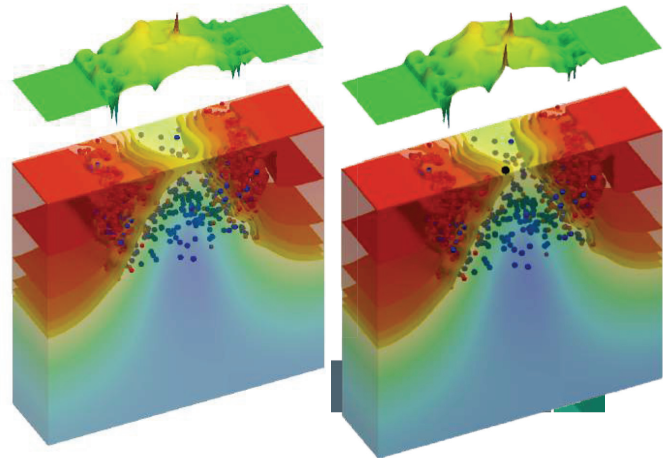


Strong interplay between statistical variability and statistical reliability





Parameter		n-MOS
L_g	[nm]	25
EOT	[nm]	0.85
X_j	[nm]	15
N_A	[E18/cm^3]	4.5
V_{dd}	[V]	1
I_{off}	[nA]	100
I_{on}	[μA]	1351
Spacer	[nm]	24



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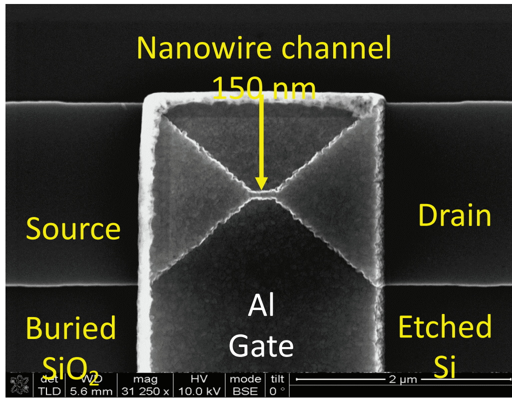
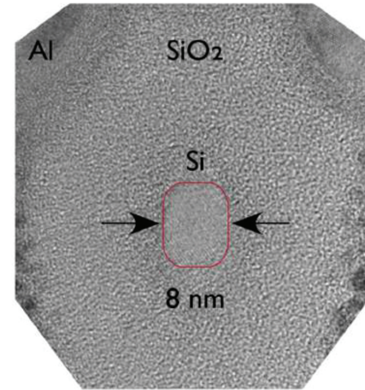
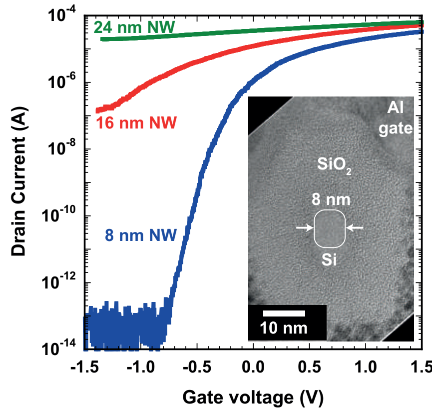
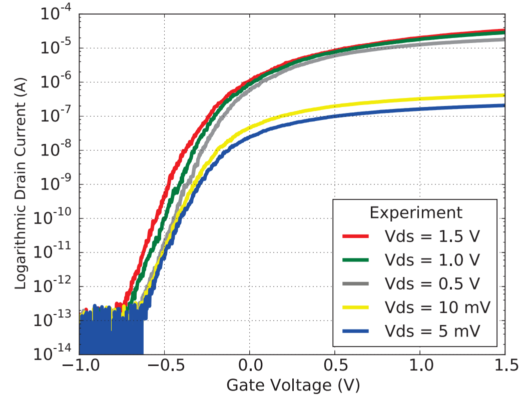
Simulations of junctionless nanowires





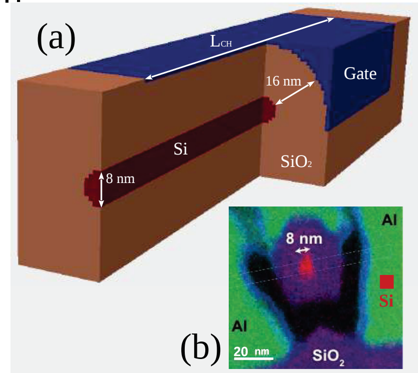


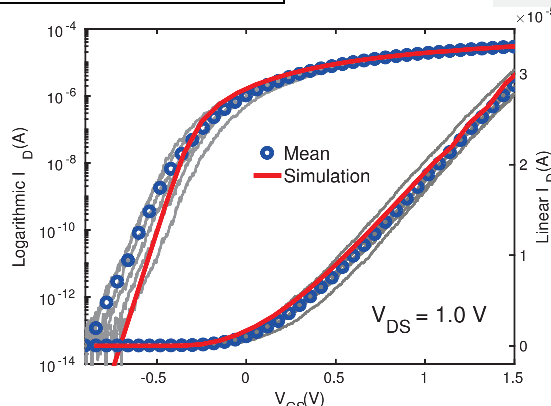


Simulations of junctionless nanowires

TCAD implementation

Si Nanowire	Parameters
Channel Diameter	8 nm
Channel Doping	1e19, 4e19,8e19 (donors)
Oxide thickness	16 nm
Gate Length	10, 25, 50, 100, 150 nm
V_D	5 mV and 1 V
Channel Length	150 nm





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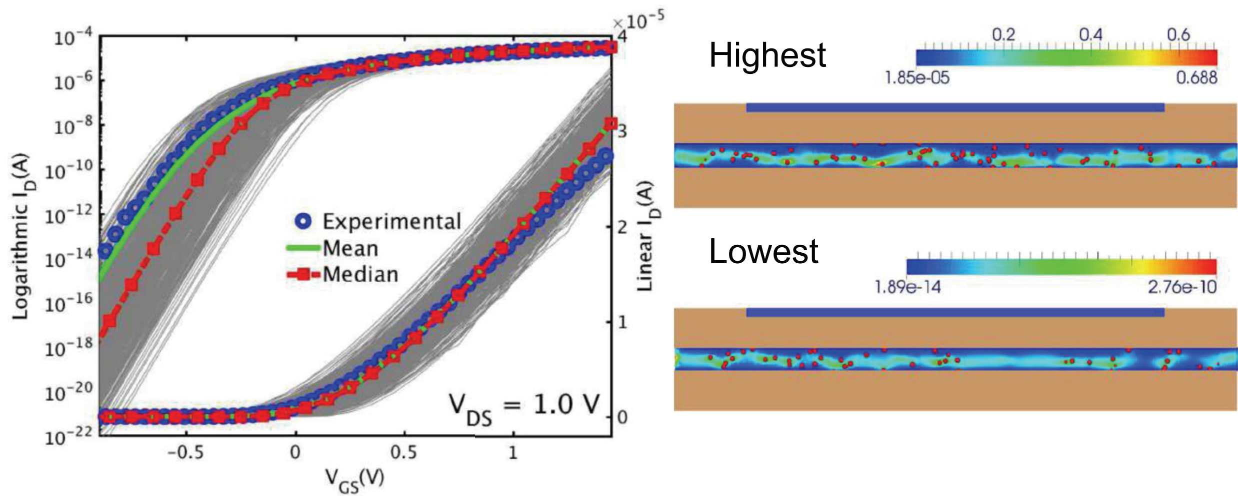
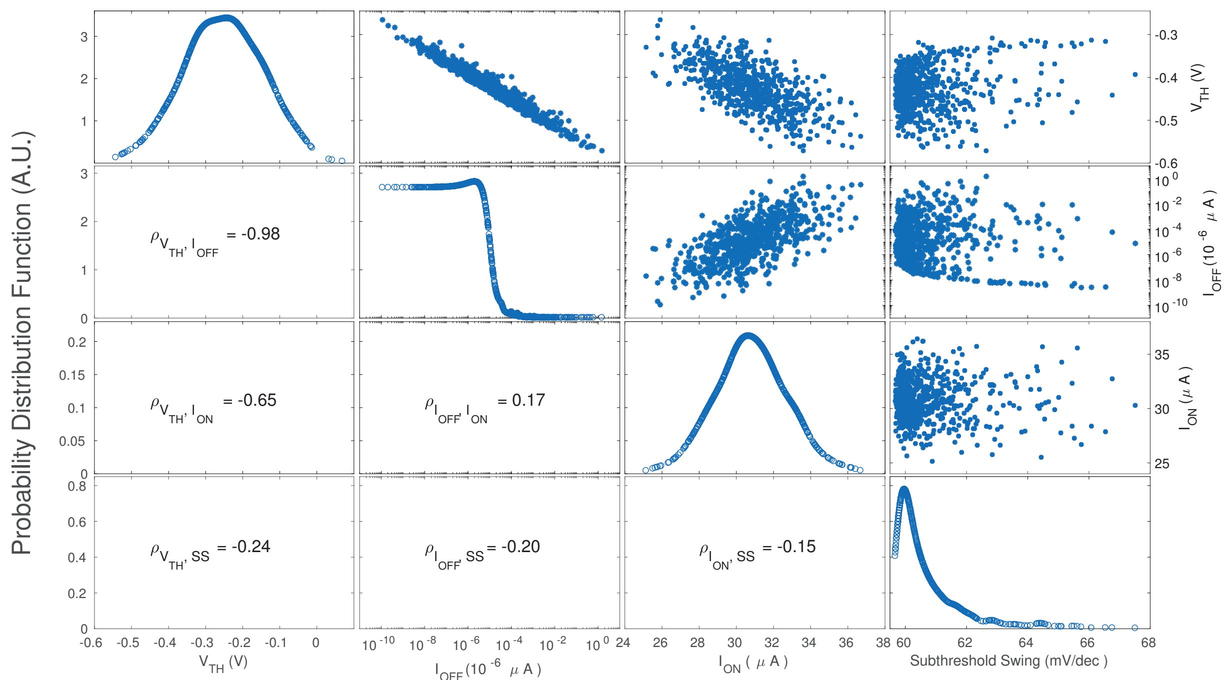


I_D–V_G characteristics of over 500 JL transistors with random distributed dopants. The last two are identical in the high gate bias region, e.g., V_G > 0 V, and in agreement with the experimental data.

Simulated 3-D dopant position and current density contours corresponding to JL transistors with (a) the highest and (b) the low OFF-currents. Current density units are A/μ m^2.

Simulations of junctionless nanowires



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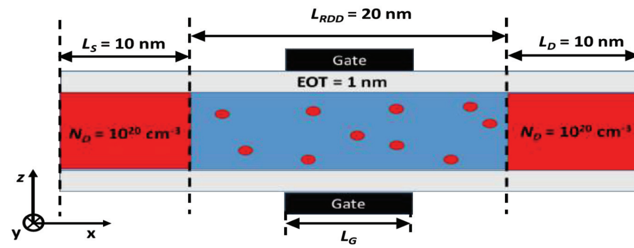
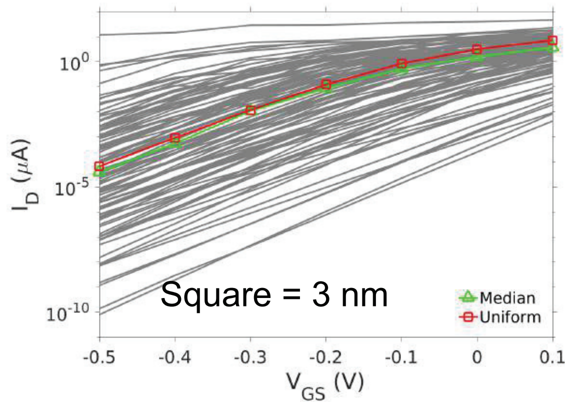
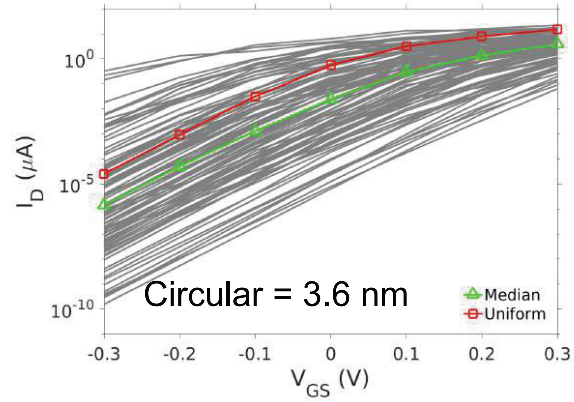


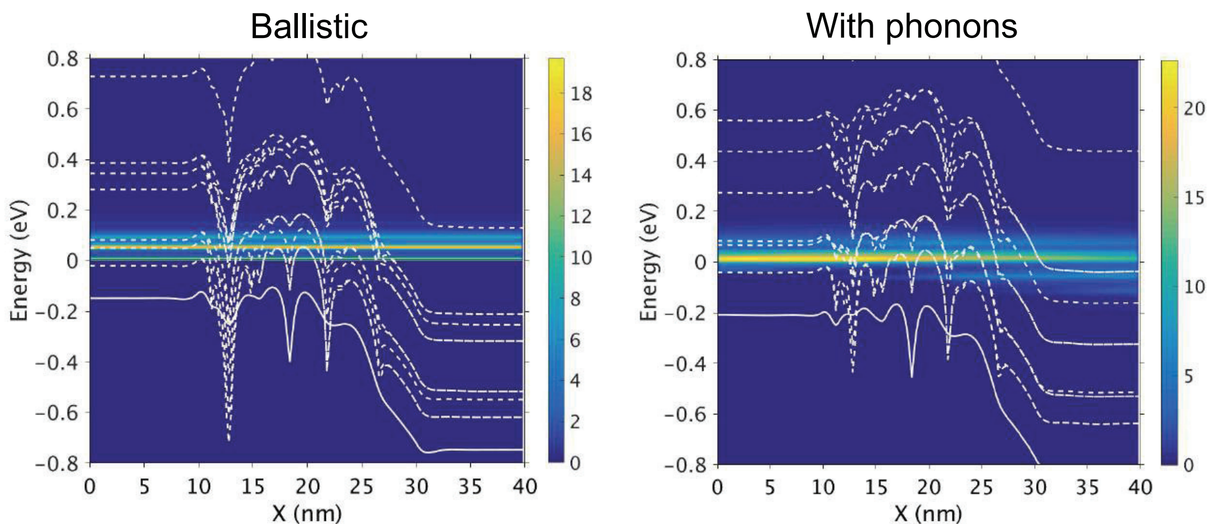




I_D-V_G characteristics at V_{DS} = 0.6 V for the device with a square cross-section and L_G = 10 nm.

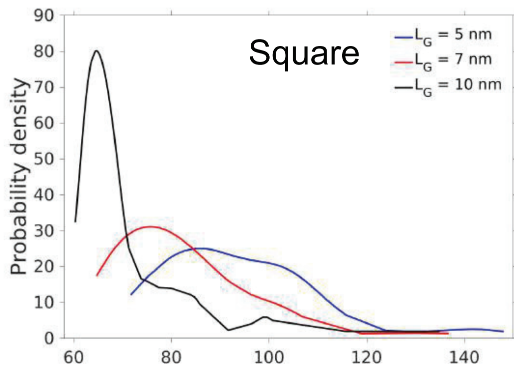
I_D-V_G characteristics at V_{DS} = 0.6 V for the device with a square cross-section and L_G = 5 nm.

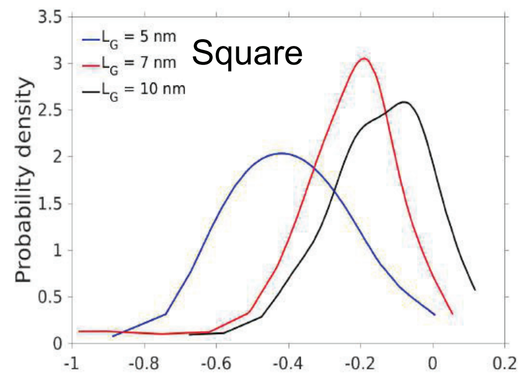
Simulations of junctionless nanowires

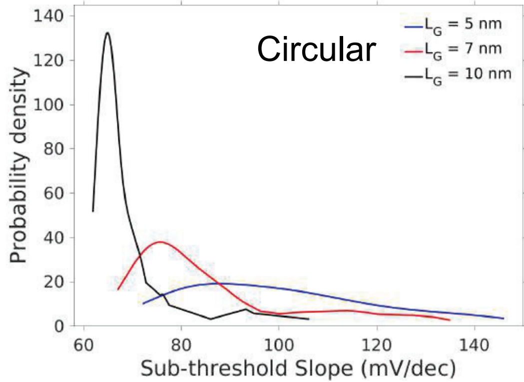


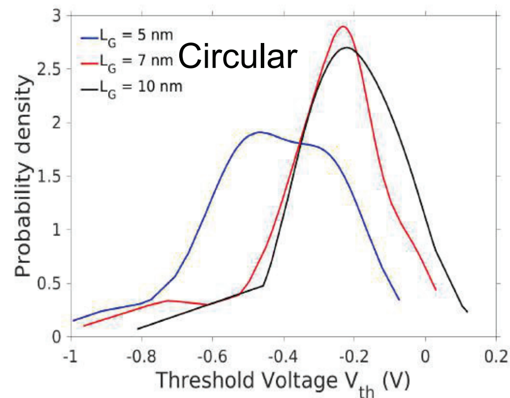
Current spectrum in μA/eV for the square device with L_G = 10 nm at V_{GS} = 0.3 V and V_{DS} = 0.6 V in ON-state (I_D = 13.59μA). The Fermi levels at the source and drain are respectively at 0 and -0.6 eV. The sub-bands are plotted in dashed lines. The solid line is the bulk conduction band in the middle of the device.

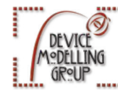
Simulations of junctionless nanowires



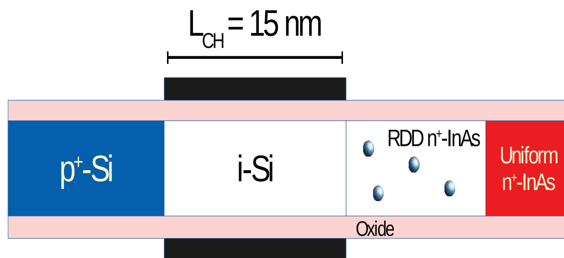


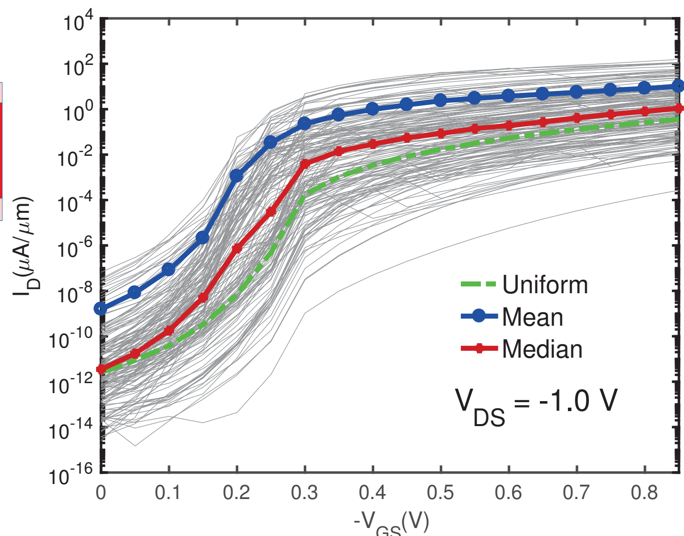




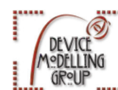


Simulations Si-InAs nanowire TFETs





$I_D - V_{GS}$ characteristics of the 150 Si-InAs nanowire TFETs with randomly distributed dopants (gray curves). The statistical mean and median are also plotted. The Si-InAs nanowire TFET with a uniform doping profile is shown as reference. The current is normalised by $2\pi R$.



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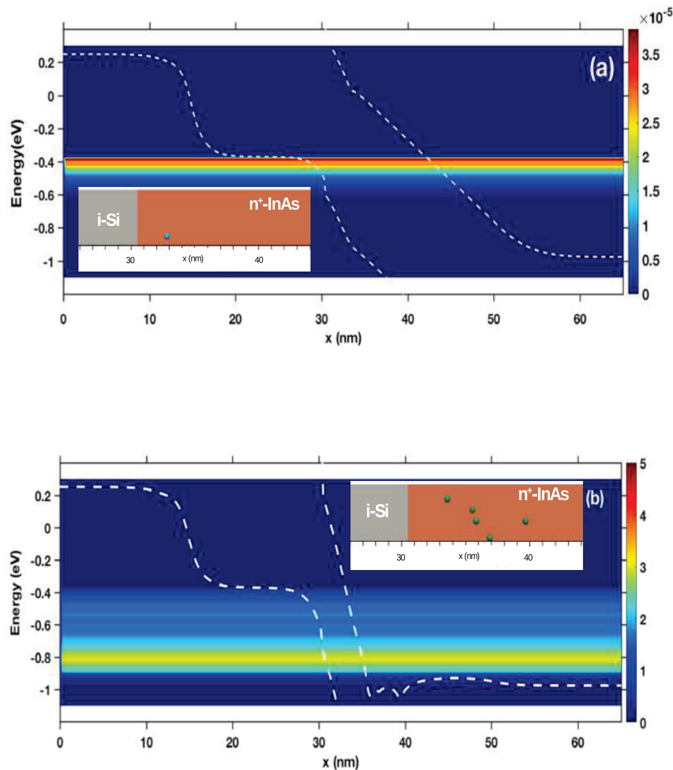
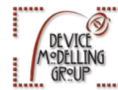


Simulated ON-state current-spectra of the Si-InAs nanowire TFETs with (a) one and (b) five dopants. The units are μA/eV. The insets show their position in each TFET. The white dashed-lines denote the highest valence and the lowest conduction sub-bands.



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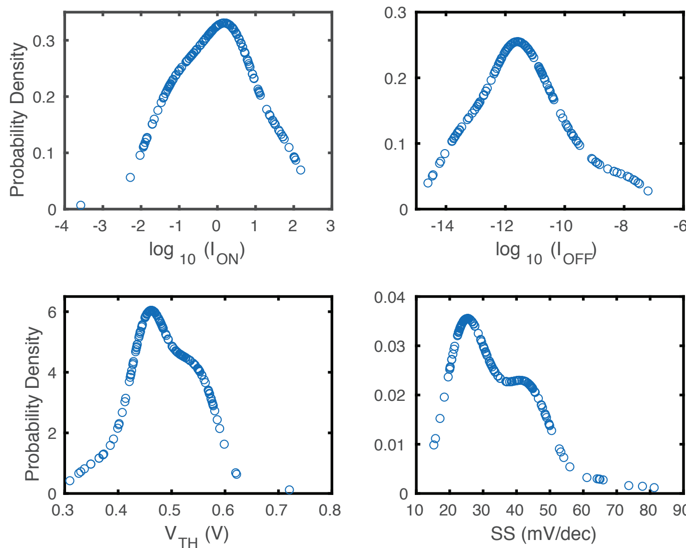
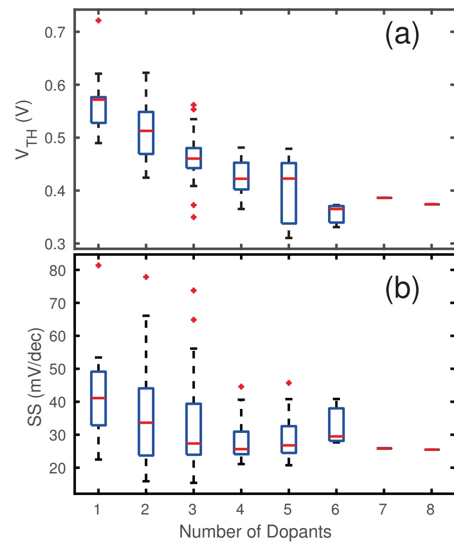
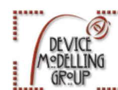


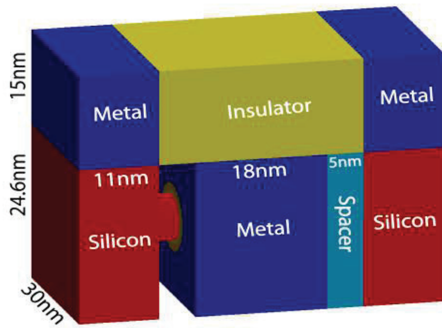


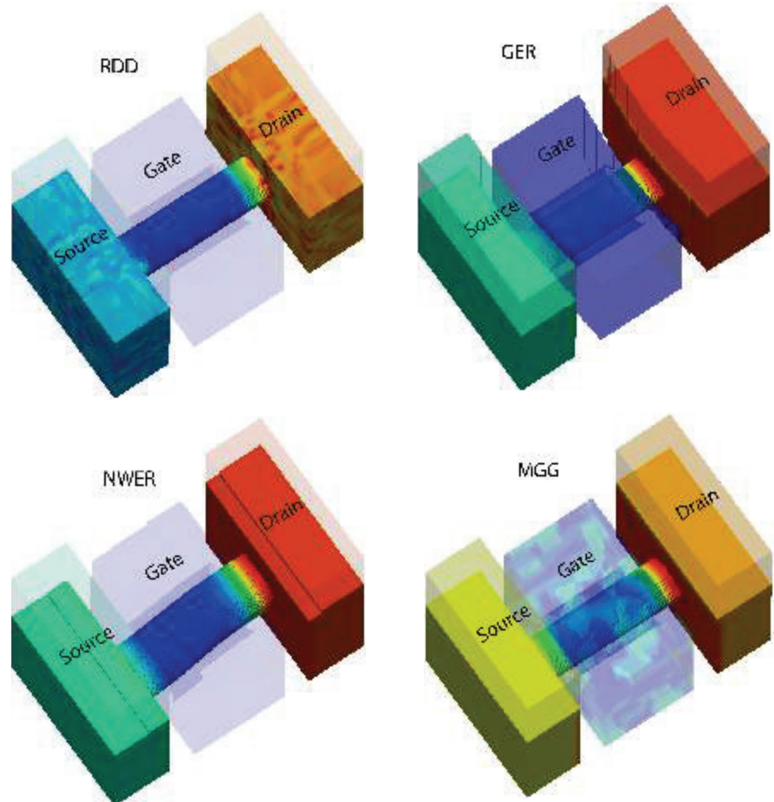
Probability density functions of the most important Figures of Merit obtained from the simulation of the ensemble of 150 Si-InAs nanowire TFETs.

Statistical analysis of (a) threshold voltage and (b) subthreshold.

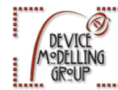


Statistical simulations of a Si nanowire transistor



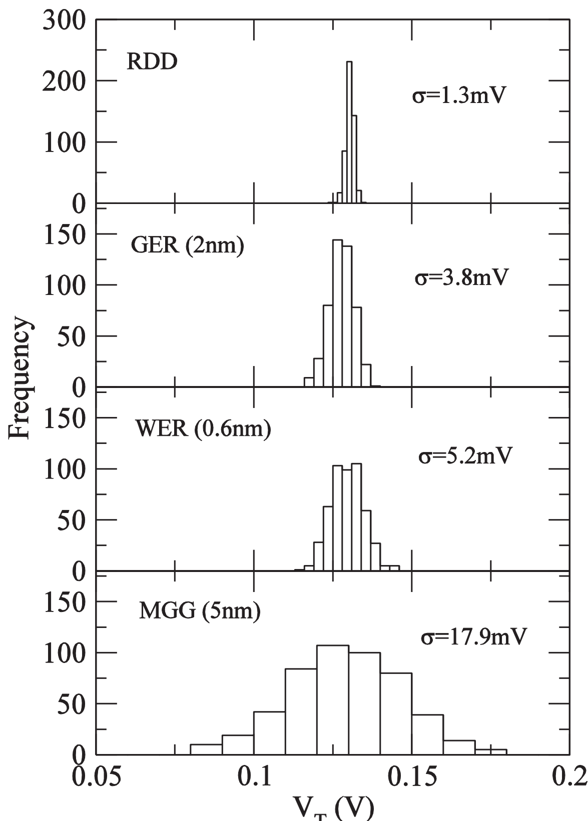


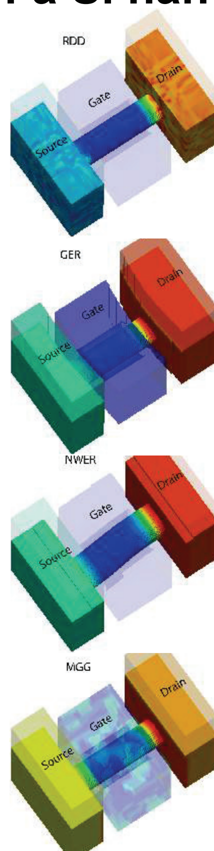
M2 Pitch	36nm
M1 Pitch	36nm
Gate Pitch	50nm
Fin Pitch	30nm
V_{DD}	0.7V
EOT	1.2nm
Leakage	3nA/µA

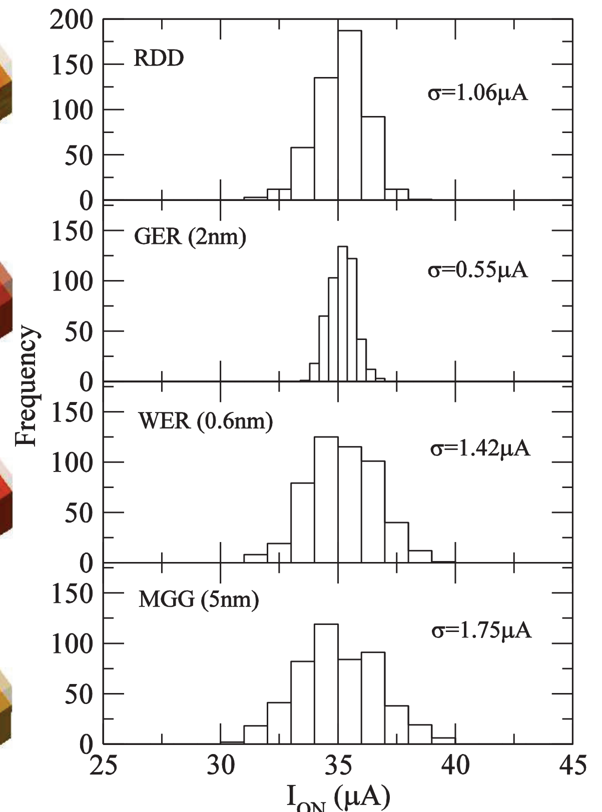


Statistical simulations of a Si nanowire transistor

1000 devices







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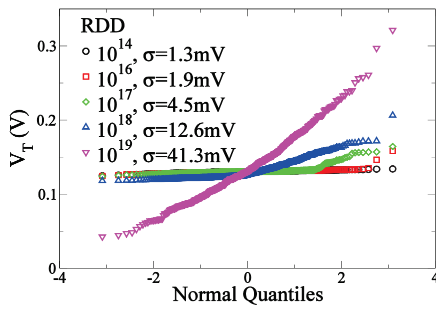
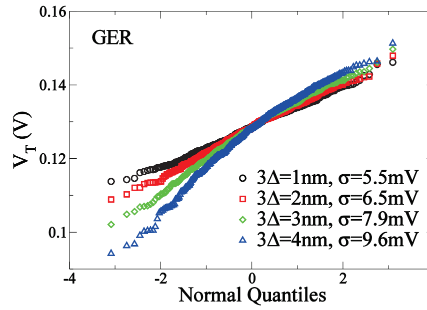
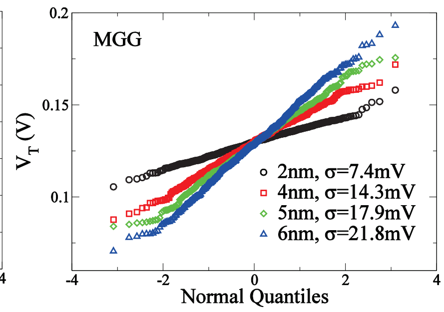
Statistical simulations of a Si nanowire transistor

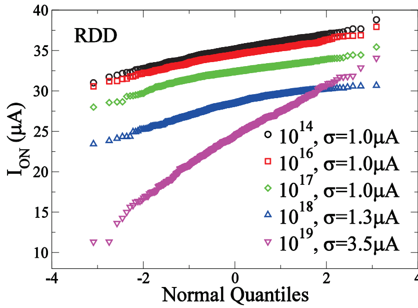
V_T – variability

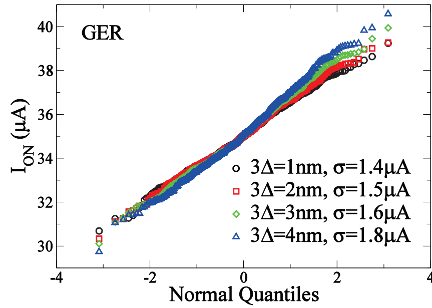


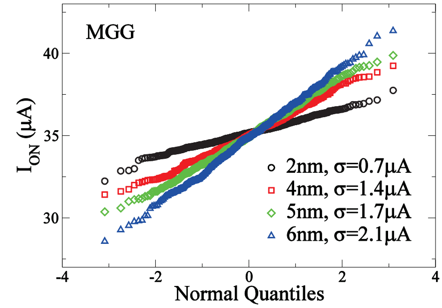


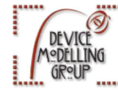


I_{ON} – variability

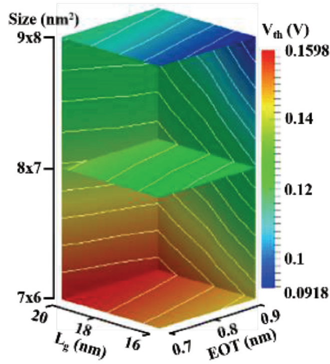




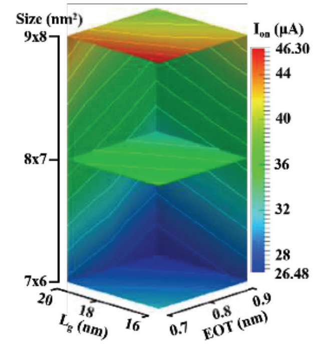


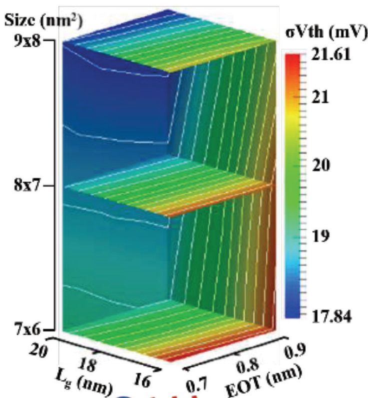


Statistical simulations of a Si nanowire transistor

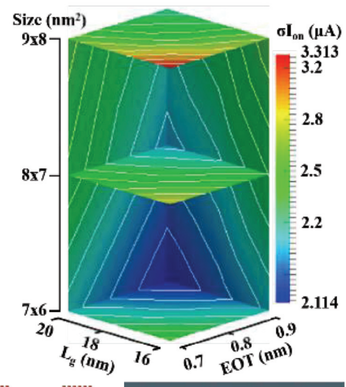


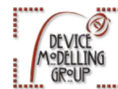
Global Variability





Local & Global Variability





Conclusions and outlook

- Variability is one of the major challenges associated with scaling
- There is global and local variability
  - Local (statistical) variability has significant impact on the current technology
  - Sources of variability: RDD, MGG, GER, NWER
- Variability should be taken into account in design and fabrication process

University of Glasgow

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