3D Devices: Experiment & Simulation

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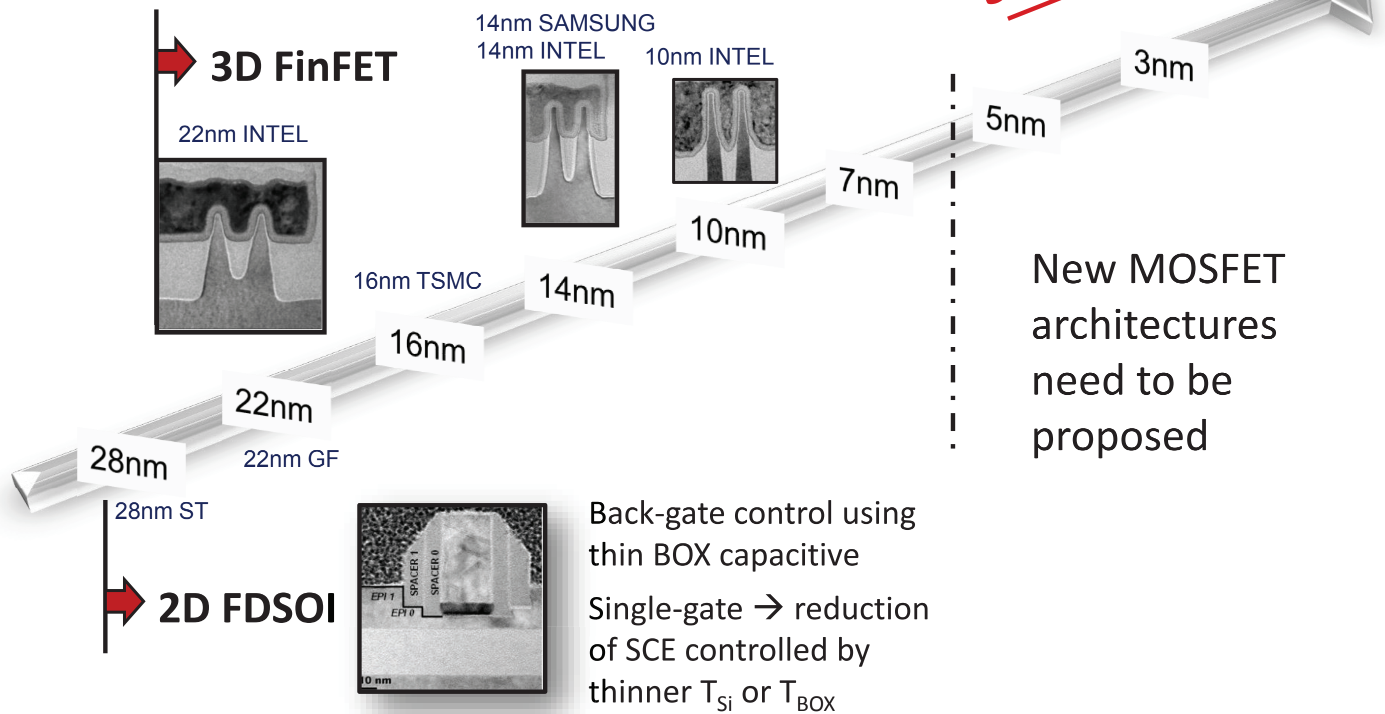
ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

Outline

- Introduction and Motivation
- Performance and Design Consideration
- 3D Process Integration for Stacked-Wires FETs
- Electrical Characterization
- Conclusions and Outlook

Context of this work



Context of this work

Recent press release

May | 2017

Samsung set to lead the future of foundry with comprehensive process roadmap down to 4nm

4LPP (4nm Low Power Plus): 4LPP will be the first implementation of **next generation device** architecture – MBCFET^{TM} structure (Multi Bridge Channel FET). MBCFET^{TM} is Samsung's unique GAAFET (**Gate All Around FET**) technology that uses a **Nanosheet device** to overcome the physical scaling and performance limitations of the FinFET architecture.

https://news.samsung.com/global/samsung-set-to-lead-the-future-of-foundry-with-comprehensive-process-roadmap-down-to-4nm

June | 2017

IBM claims 5nm Nanosheet breakthough

IBM researchers and their partners have developed a new transistor architecture based **on Stacked Silicon Nanosheets** that they believe will make FinFETs obsolete at the 5nm node

http://www.eetimes.com/document.asp?doc_id=1331850&

GAA MOSFET devices are becoming an industrial reality

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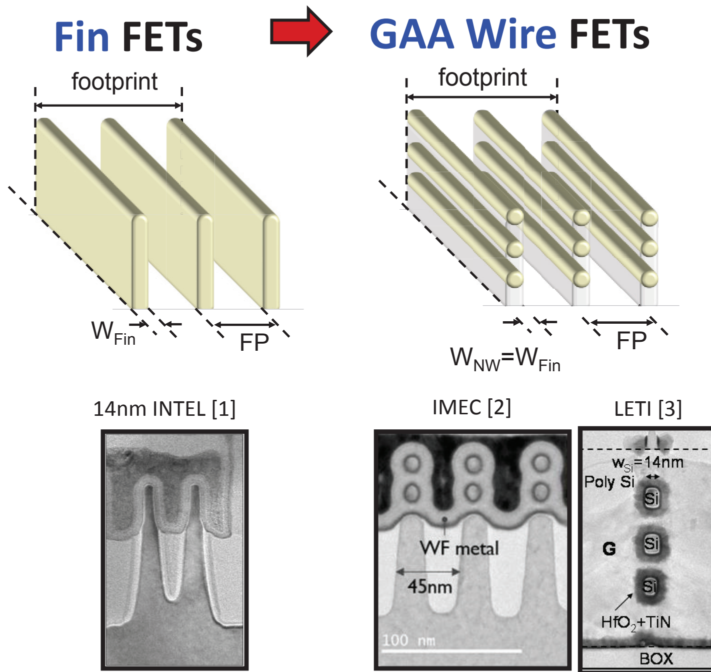
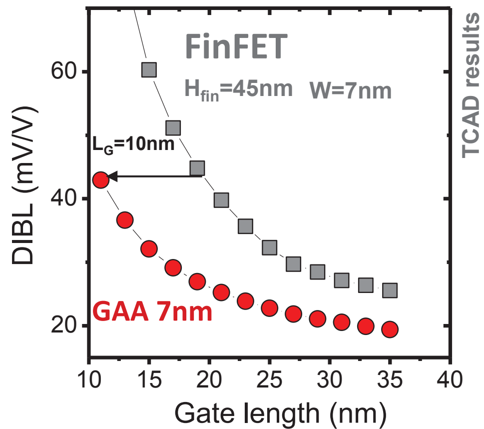
Motivation



- Wire FETs can be view as an evolutionary step from the FinFET
- Wire FETs share many of the same process steps as the FinFET
- GAA FETs provides a better electrostatics than FinFET



[1] S. Natarajan et *al.*, IEDM, 2014.
[2] H. Mertens et *al.*, VLSI Technology, 2016.
[3] C. Dupré et *al.*, IEDM, 2008.

Introduction – Goals and Strategy

Main Objective of SUPERAID7

Simulation of the impact of systematic and statistical process variations on devices, interconnects and circuits down to the 5nm node

WP1
Project
managment

WP2: Specifications and benchmarks

Define specifications for two generations of devices (**7nm Trigate and 5nm GAA Stacked-Wires FETs**) – process-flow/morphological data/electrical data…

→ to provide input data for the calibration/validation of simulation tools

→ to give a feedback to other WP after the comparison between simulation and experiment

WP3: Variation-aware equipment and **process simulation**

WP4: Variation-aware **device and interconnect simulation**

WP5: Software integration and **compact models**

Dissemination (WP6) and exploitation (WP7)

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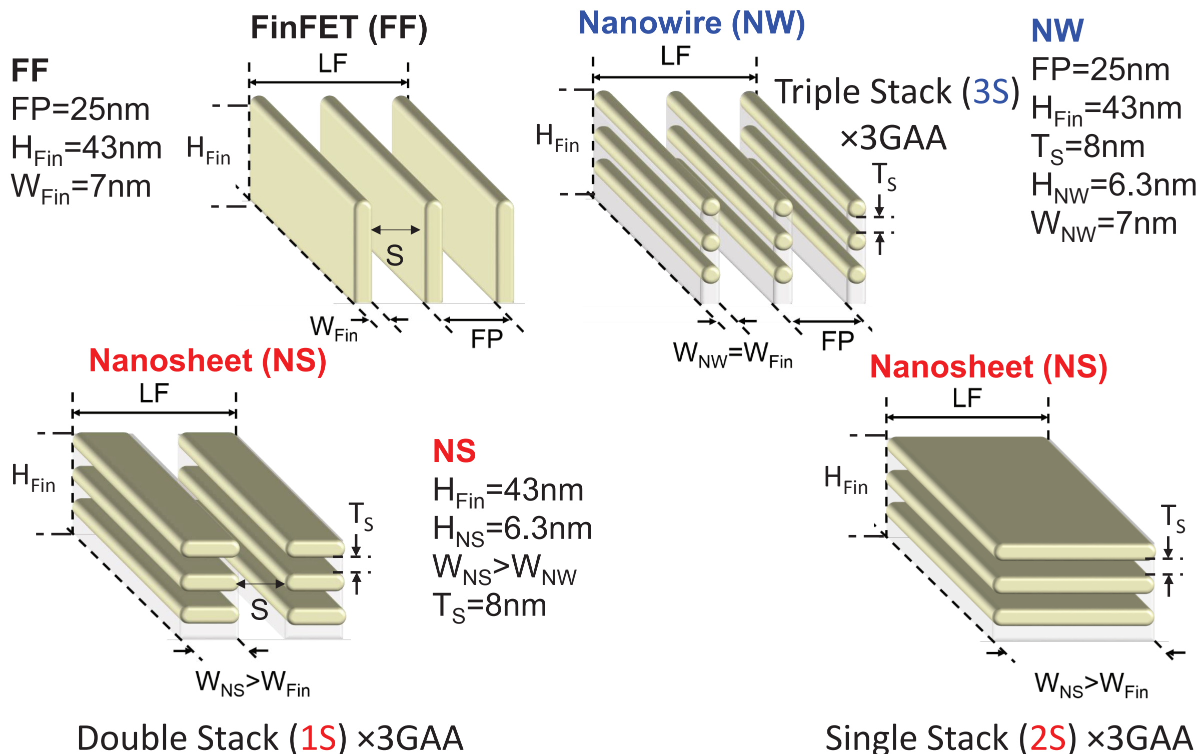
Performance and Design Consideration



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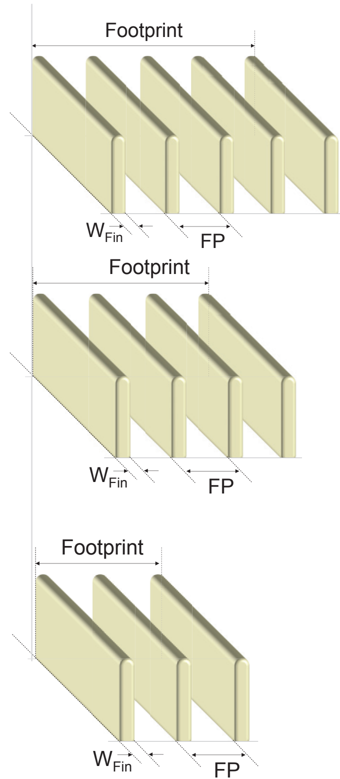
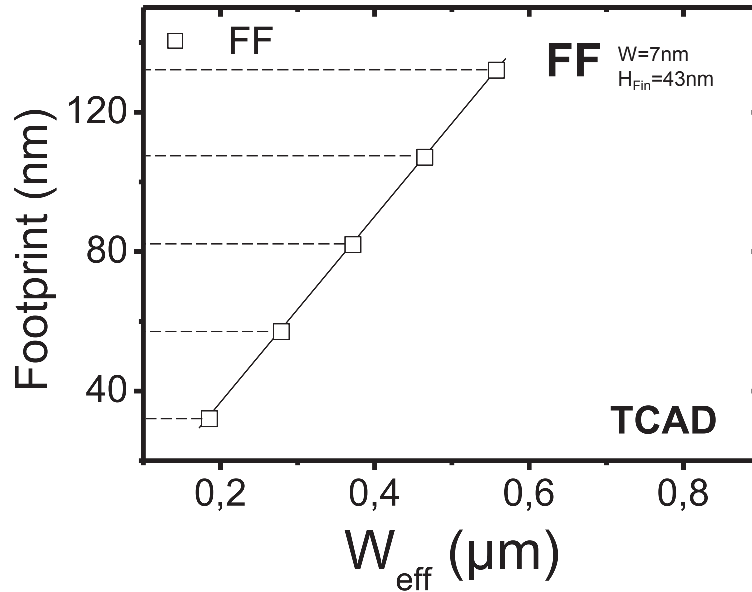
Effective width of FinFET

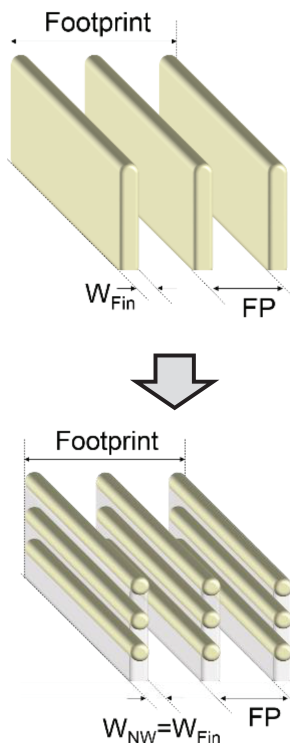


$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$



S. Barraud et al., IEDM 2017

FinFET versus GAA Nanowires



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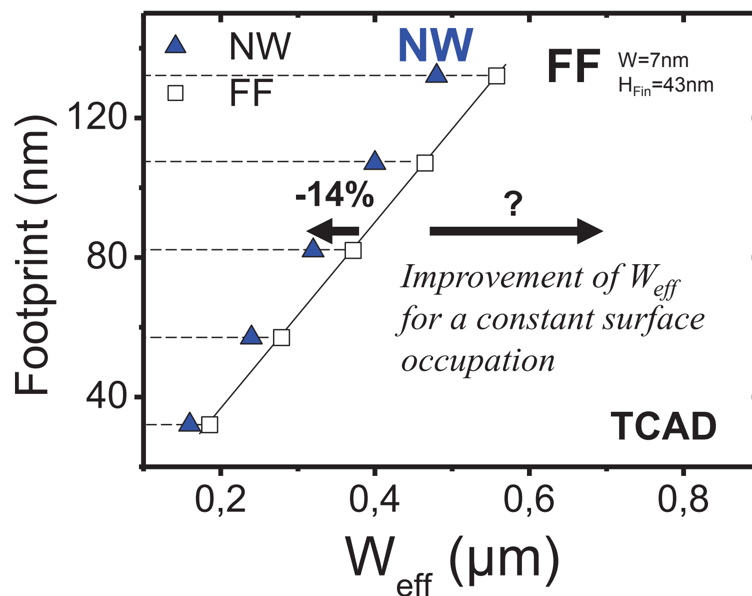
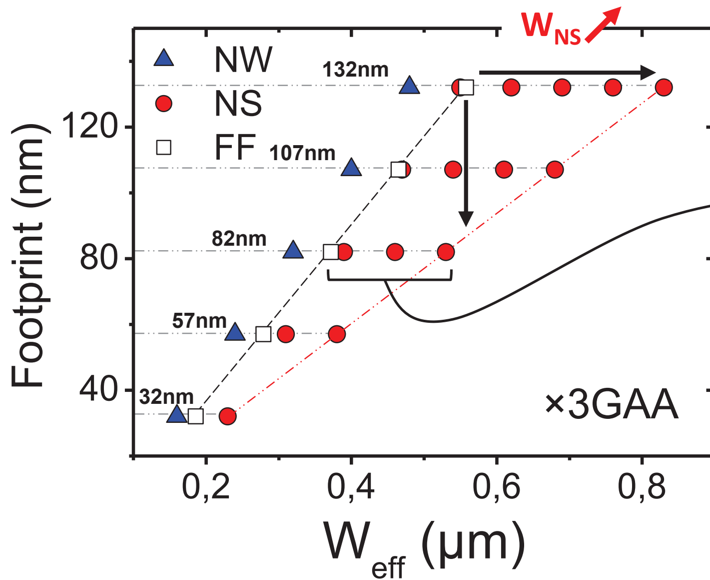
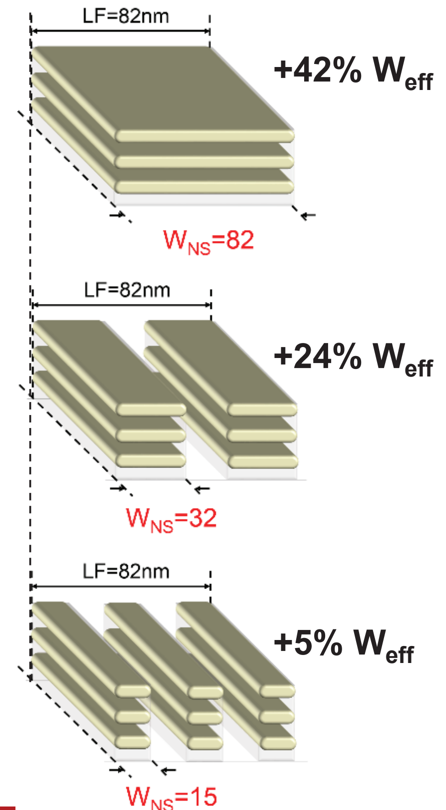


S. Barraud et al., IEDM 2017

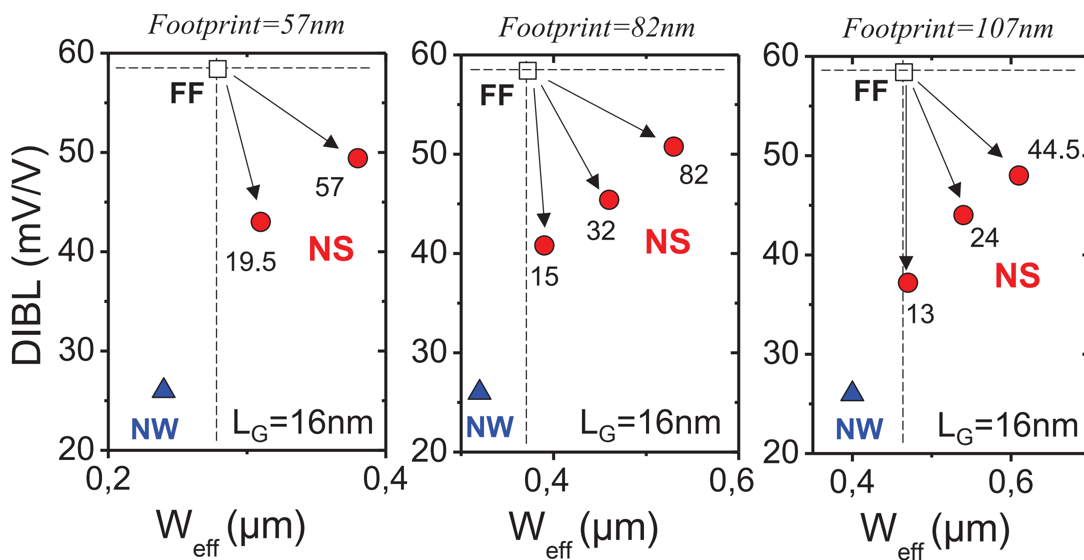
GAA Nanowires versus GAA Nanosheets

$$I_{DS} = \mu \times C_{ox} \times \frac{W_{eff}}{L_G}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$





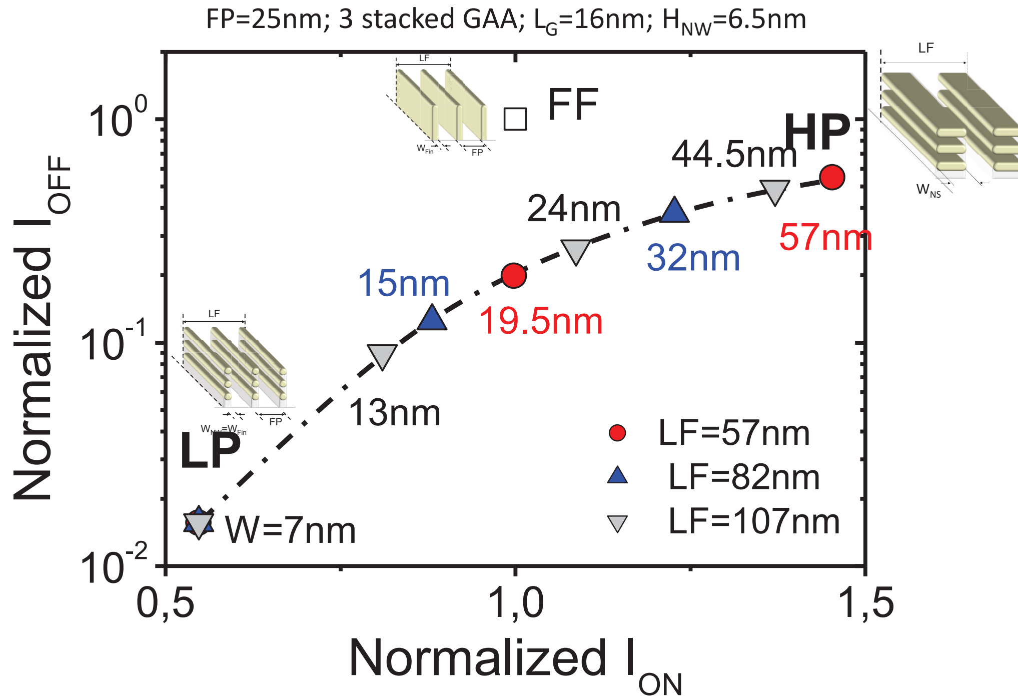
Tradeoff between SCE and W_{eff}



GAA stacked-nanosheets maximize W_{eff} (*i.e.* drive current) per layout footprint with improved channel electrostatics.

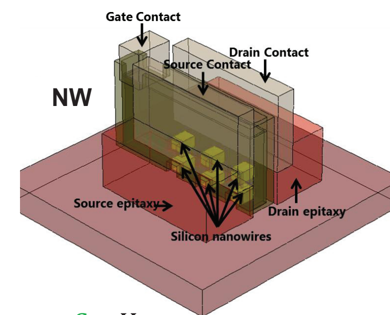
S. Barraud et al., IEDM 2017

Power/Performance Optimization



Parasitic capacitances and delay

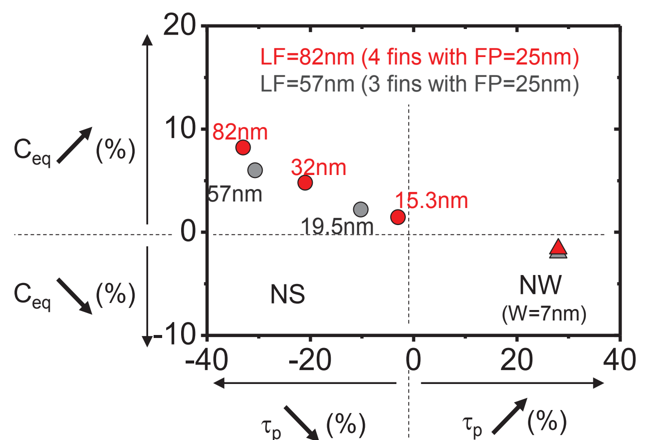
A delay reduction of around 20% is expected for W_{NS}~30nm



τ: Delay
I_{eff}: Effective drive current
$I_{eff}=(I_H+I_L)/2$
$I_H=I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$
$I_L=I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD})$
Supply voltage V_{DD}=0.7V
FO=3
L_G=16nm
Spacer size: 4.2nm
EOT=0.67nm
$C_{back-end}$=2fF
M=2: Miller effect in inverter

$$\tau = \frac{C_{eq}.V_{dd}}{N_{stack}.I_{eff}}$$

$$C_{eq} \approx (\mathrm{M}+2.\mathrm{FO}).C_{gd0} + {}^{3}/_{4}.\frac{\varepsilon_{SiO_2}.L_g.w_{eff}}{t_{inv}}.\mathrm{FO} + \frac{C_{back-end}}{2}$$



What have we learned?

- GAA NS structures could be used to maximize the effective width which will improve the drive current without increasing power density (lower DIBL than in short-channel FinFET devices).
- A delay reduction of around 20% is expected for W_{NS}~30nm
- Nanosheet transistors offer more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width

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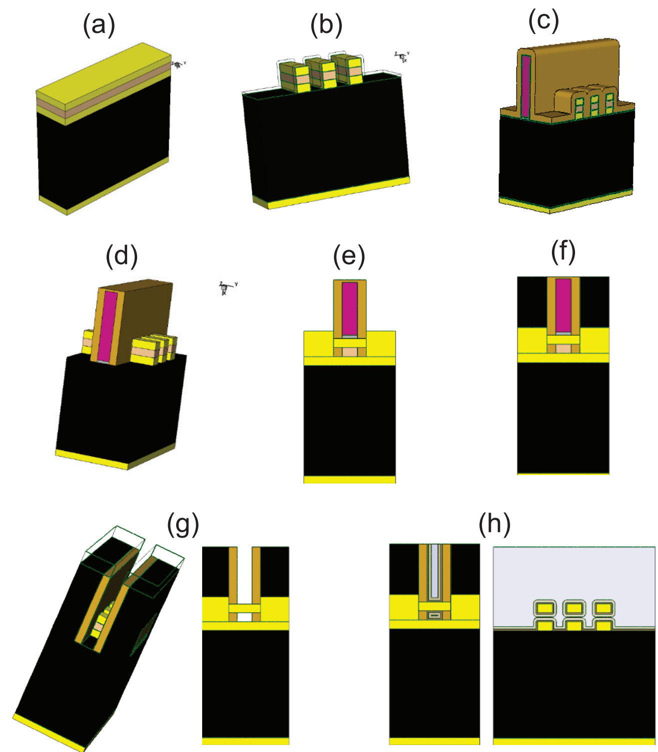
Process Flow of GAA Stacked Wires FETs

RMG process
Self-Aligned Contacts (**SAC**)
SIT Fin patterning (FP=40nm)

- SOI substrate
- (a) SiGe/Si epitaxy
- (b) Fin patterning (SIT process)
- Dumy gate deposition / CMP
- Dummy gate patterning
- (c,d,e) Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- (f) ILD deposition / CMP
- (g) Dummy gate removal
- Release of Si NW (SiGe etching)
- Gate dielectric (HfO_2 2nm)
- (h) TiN deposition
- Fill metal (W) deposition / CMP
- Self-aligned contact (SAC) +
- M1 BEOL



* Blue module: specific technical requirements for stacked wires FETs (as compared to FinFET devices)

Device Fabrication – (Si/SiGe) multilayer

Vertically Stacked GAA Si Nanosheet FET

- SOI substrate
- SiGe/Si epitaxy
- Fin patterning (SIT process)
- Dumy gate deposition / CMP
- Dummy gate patterning
- Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- ILD deposition / CMP
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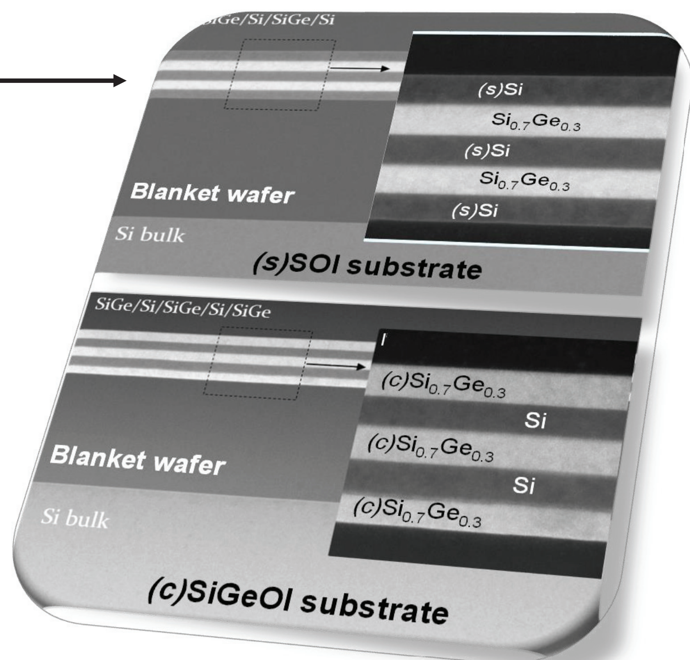
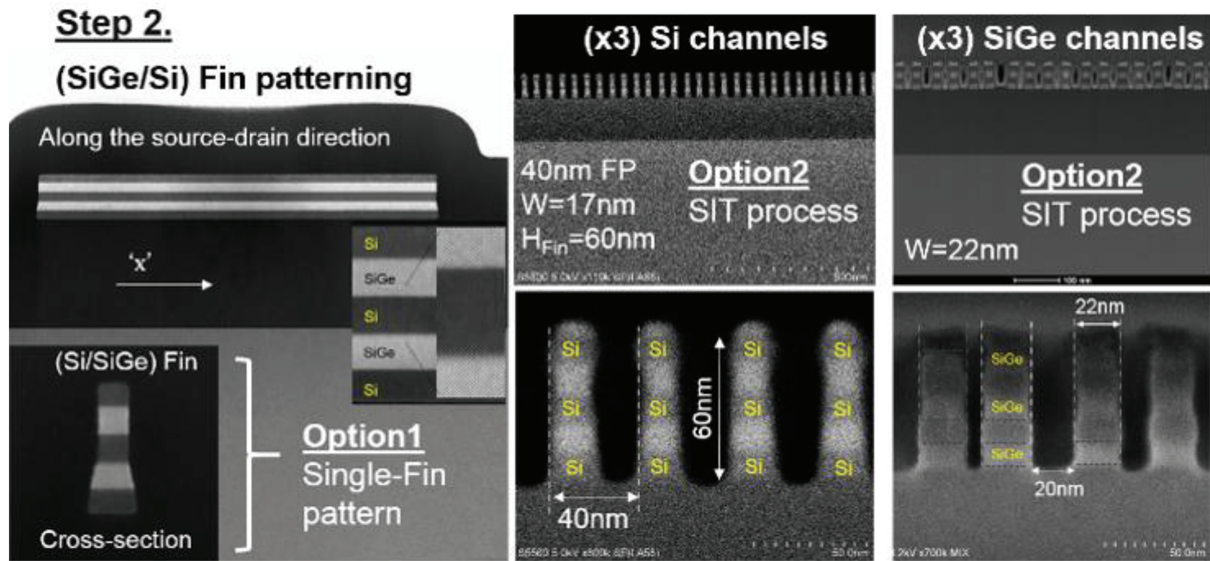


Epitaxial growth of ($Si_{0.7}Ge_{0.3}/Si$) multilayers

S. Barraud et al., IEDM 2016

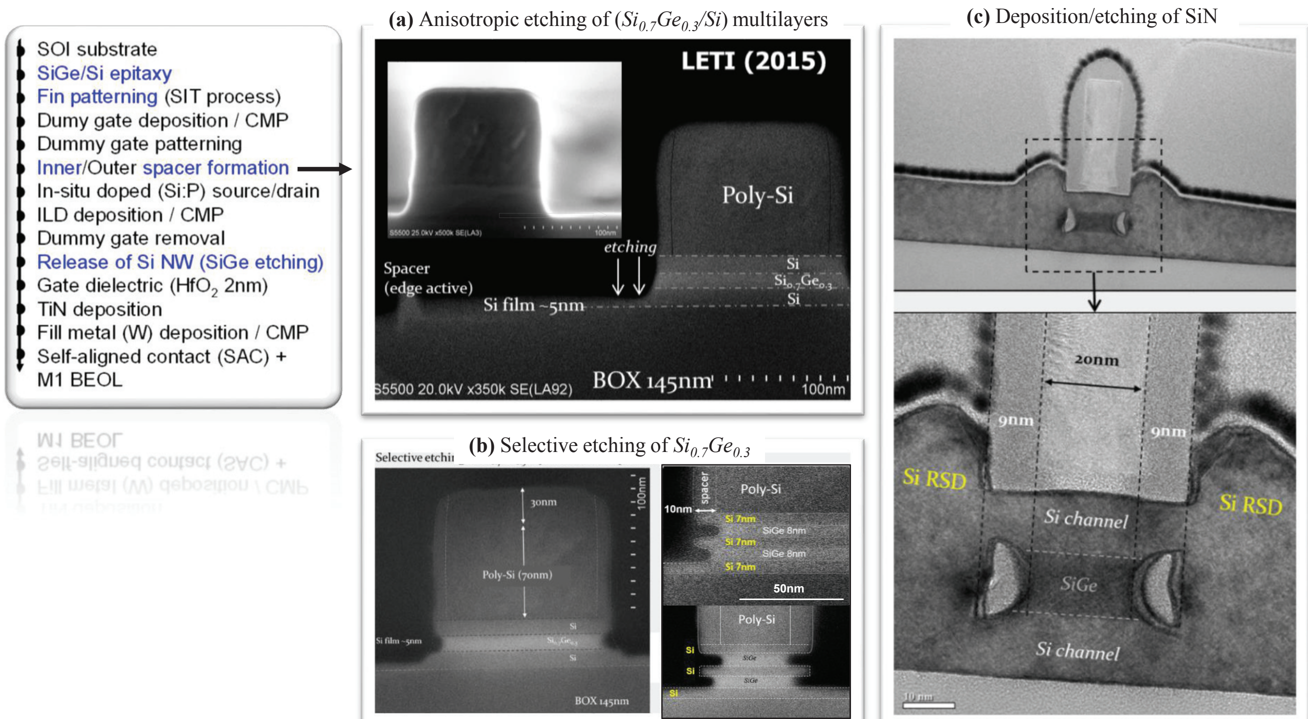
Device Fabrication – Fin patterning



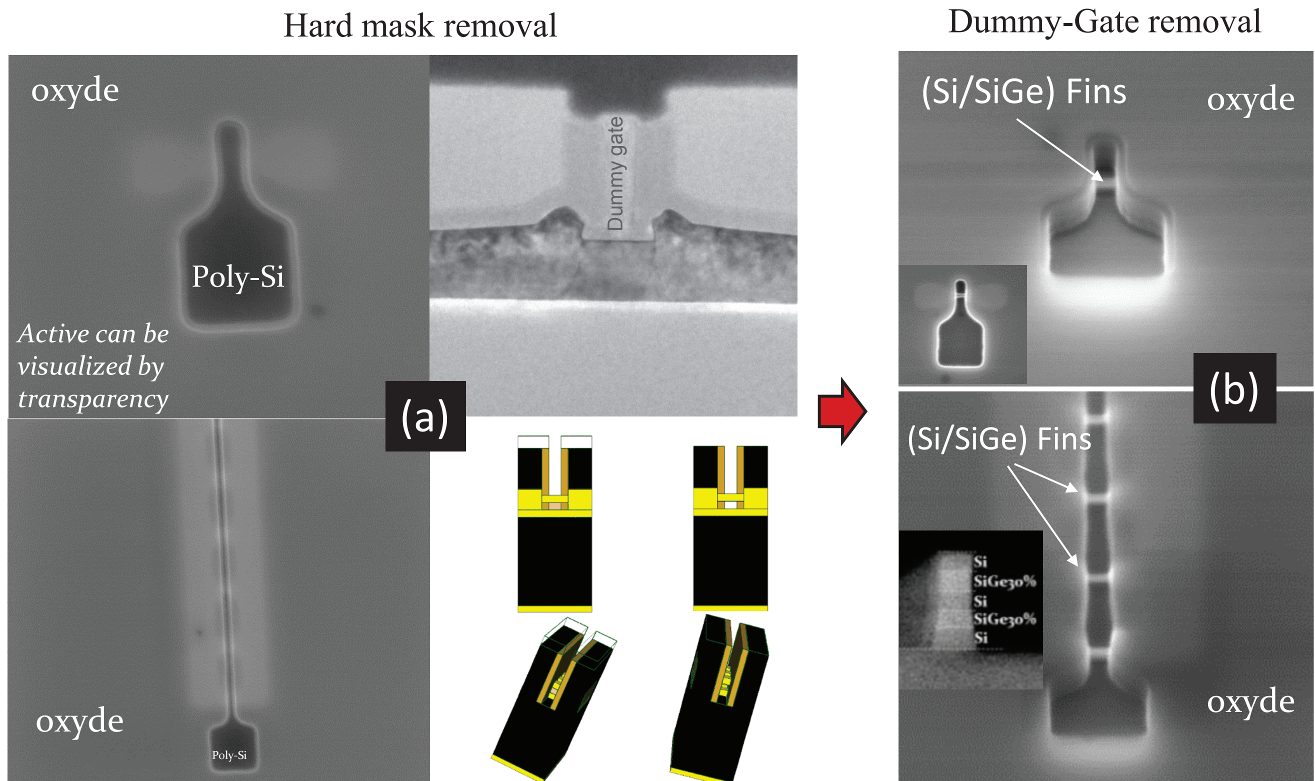
TEM images after etching of **(Si/SiGe) fins**. Two types of fins patterning were used: **(Left) single-Fin process and (Right) dense arrays of fins with a SIT process**. Our SIT-based patterning technique yields **40 nm-pitch fins which are 60 nm high and 20 nm wide** for both Si and SiGe channels

Device Fabrication – Outer/Inner Spacer

Vertically Stacked GAA Si Nanosheet FET



Device Fabrication – RMG module



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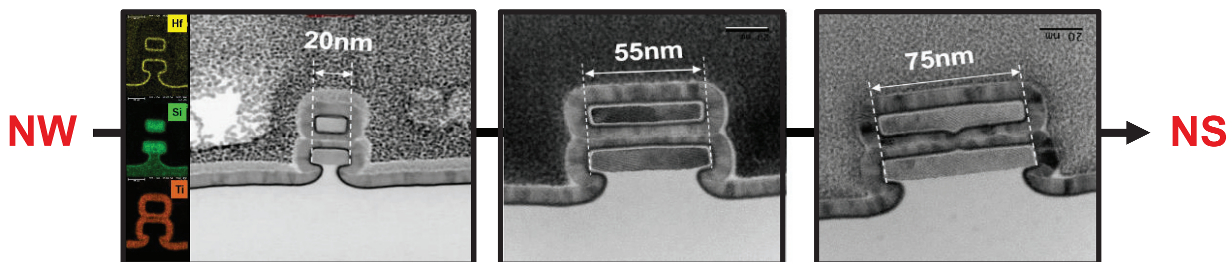
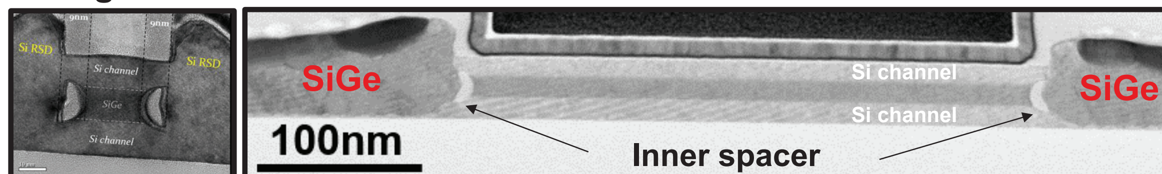
Vertically Stacked-Wires FETs

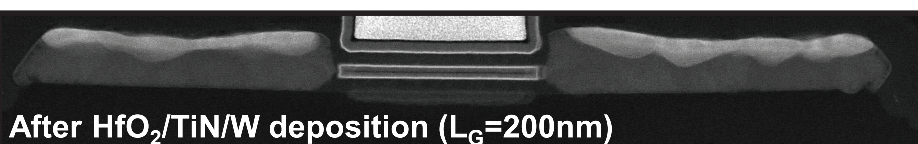
NW/NS Cross-section



Along source-drain direction



Short-L_G (20nm) **Long-L_G (>300nm)**



S. Barraud et al., IEDM 2016

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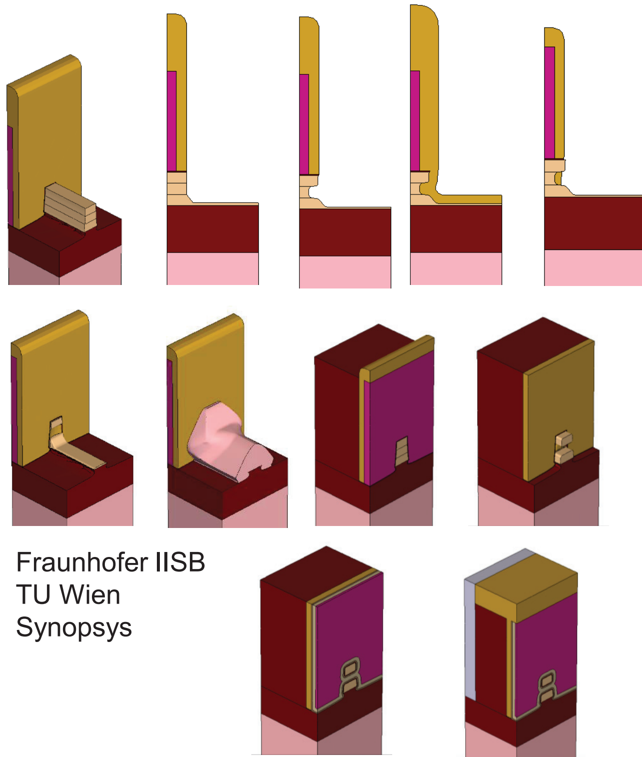
Simulation of Device Fabrication (WP3)



- SOI substrate
- SiGe/Si epitaxy
- Fin patterning (SIT process)
- Dumy gate deposition / CMP
- Dummy gate patterning
- Inner/Outer spacer formation
- In-situ doped (Si:P) source/drain
- ILD deposition / CMP
- Dummy gate removal
- Release of Si NW (SiGe etching)
- Gate dielectric (HfO_2 2nm)
- TiN deposition
- Fill metal (W) deposition / CMP
- Self-aligned contact (SAC) + M1 BEOL

- LETI data (SEM, TEM, strain mapping, …) provided for the **calibration/validation of process simulation**
- **Identification of relevant process parameter for variability**
- **Influence** of process parameters **on electrical performance of 3D devices**

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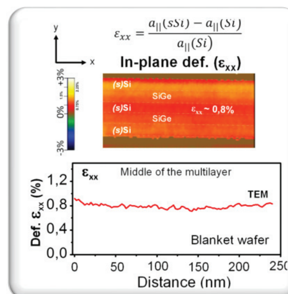
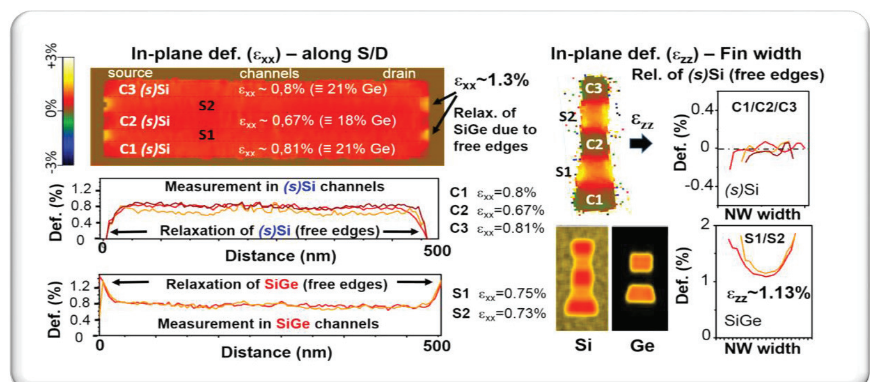
Strain Characterization

1. Superlattice (SiGe/Si)
2. Fin Patterning
   - Dummy Gate Deposition & RIE
   - Spacer Deposition and RIE
   - Inner spacer formation
3. Source/Drain Epitaxy
   - ILD & CMP
   - Dummy Gate Removal
   - Formation of Suspended NW (release of NW)
4. Gate Stack Formation
   - Contact/BEOL



Strain engineering is another key factor for stacked-wires FETs.

Strain maps were obtained by TEM using Precession Electron Diffraction technique*



Is initial strain (substrate-induced strain) can be used to boost performances?

* M.P. Vigouroux et *al.*, APL **105**, 191906 (2014)
* D. Cooper et *al.*, Nano Lett. **15**, 5289 (2015)

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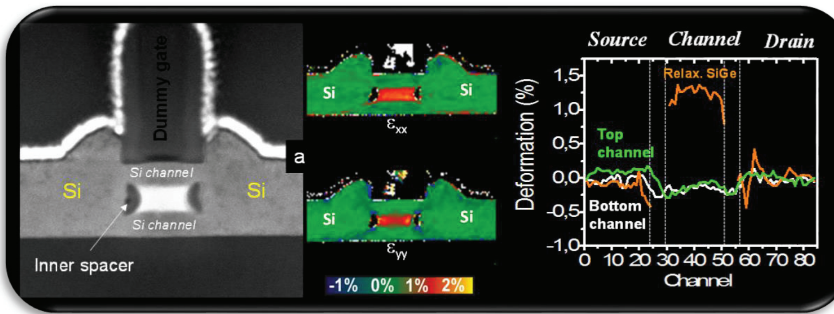
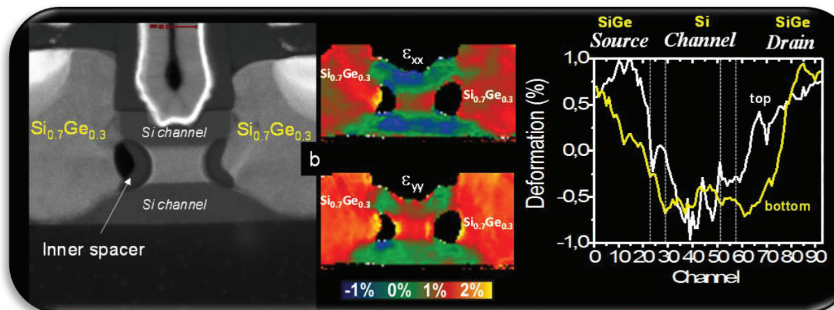
Strain Characterization

Deformation maps acquired by PED after Si Source/Drain



The silicon channels as well as the source and drain are unstrained → A deformation close to 0% is observed

Deformation maps acquired by PED after SiGe Source/Drain



Optimized engineering of process-induced stress techniques can be efficient in 3D stacked-NWs devices

S. Barraud et al., IEDM 2016

What have we learned?

- Horizontal GAA NW and NS also have the advantage of being fabricated with minimal deviation from FinFET (FF) devices in contrast to vertical NWs which require more disruptive technological changes.
- The benefits of epitaxially regrown SiGe:B S/D junctions was evidenced, with a significant compressive strain (~1%) injected in top and bottom Si *p*-channels → need to be extrapolated at 5nm design rules.
- Process Simulation well reproduces morphological characterization → relevant process parameter can now be used for variability studies.

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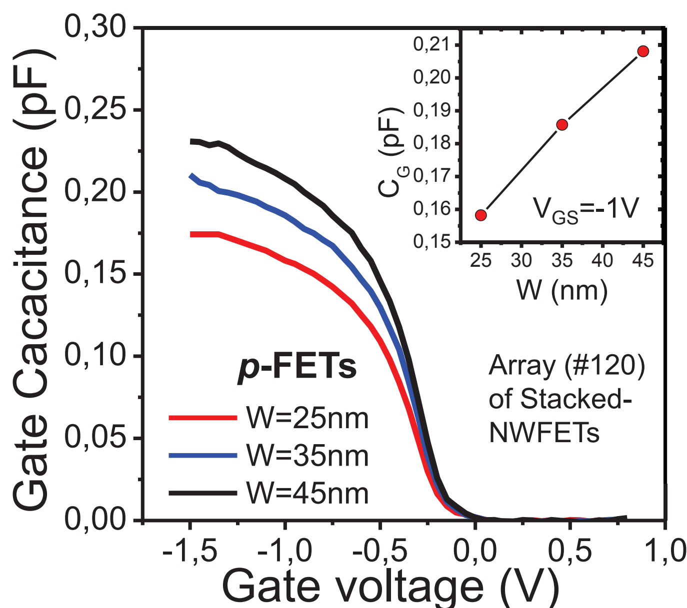
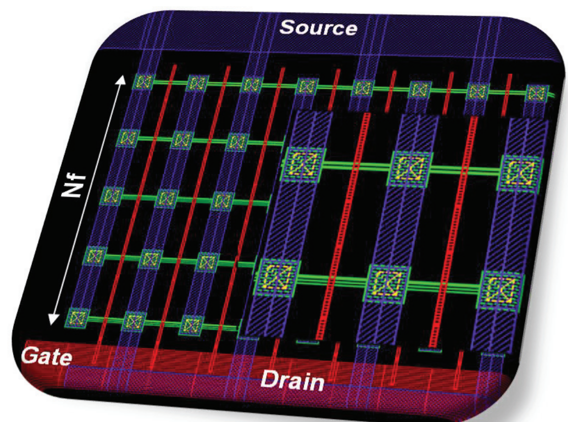
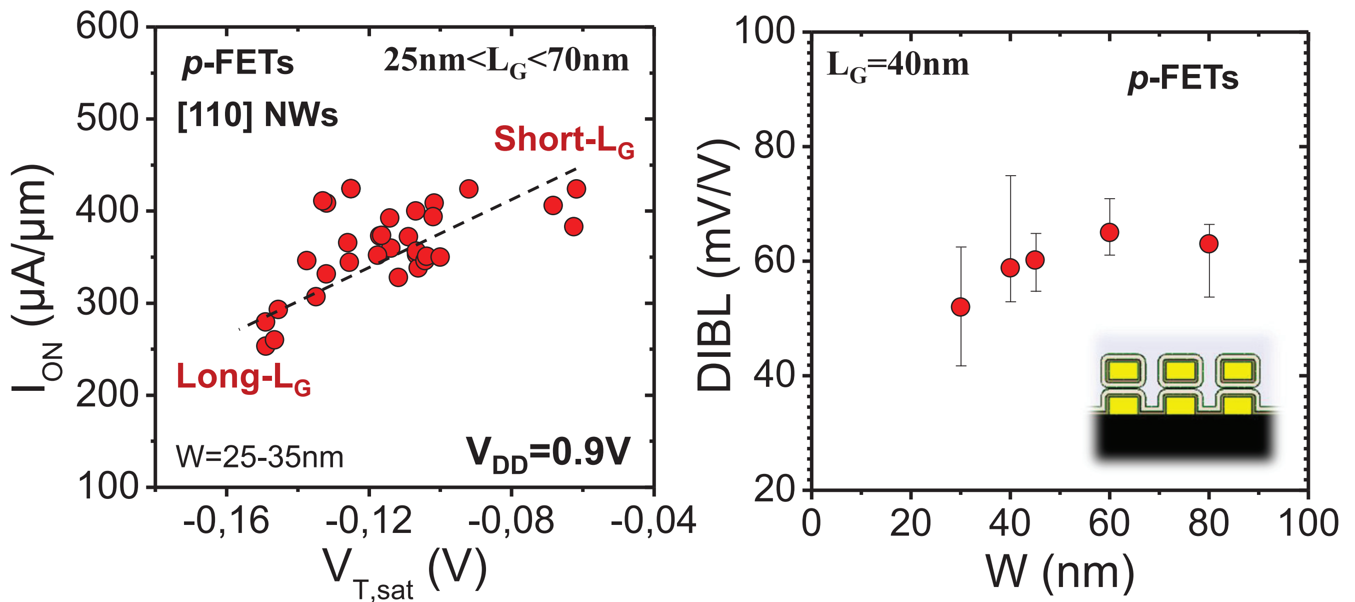
Electrical Characterization





The CV curves, obtained from a multi-fingers gate and an array (#120) of stacked wires

Electrical Characterization



DIBL is constant above W=60nm

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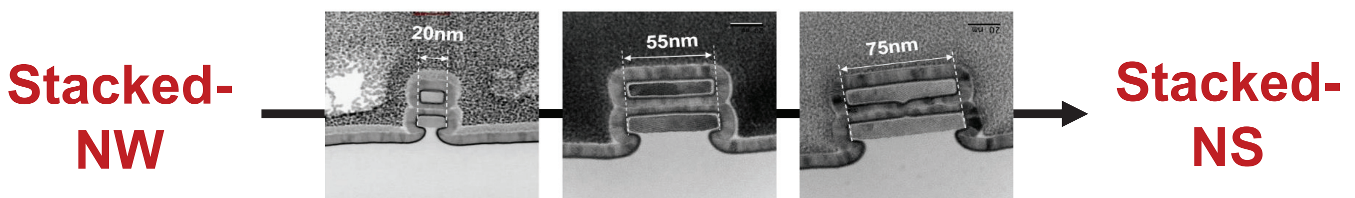
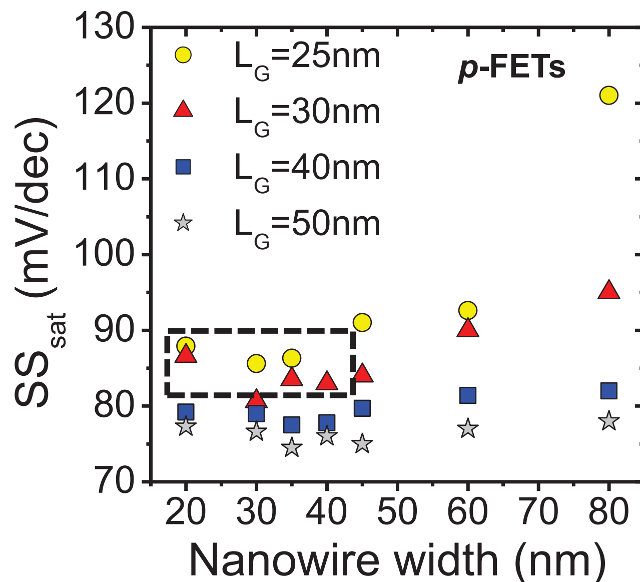
Electrical Characterization



No increase of SS_{sat} up to 40nm

→ High W_{eff} can be used with a good electrostatics control



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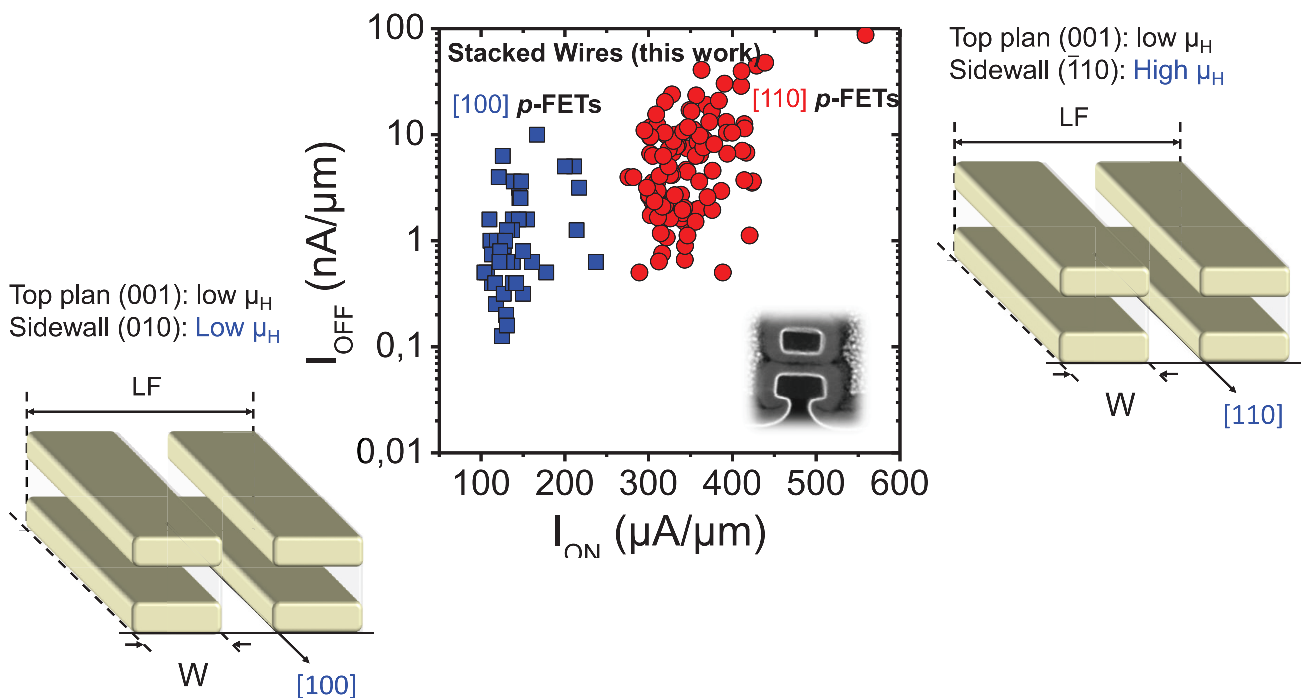
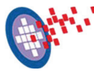
Electrical Characterization



Conclusions and Outlook

- Fabrication of vertically stacked Nanosheet MOSFETs (RMG process) are now demonstrated (inner spacers, SiGe:B S/D, 44/48nm CPP - IBM).
- Horizontal GAA Nanosheet also have the advantage of being fabricated with minimal deviation from FinFET (FF) devices in contrast to vertical NWs which require more disruptive technological changes.
- Strain characterization at different steps of fabrication (PED)
  Efficiency of process-induced strain (SiGe S/D) → significant compressive strain (~0.5 to 1%) in top and bottom Si *p*-channels.
- Design flexibility: Nanosheet transistors offer more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width.
- Morphological/Electrical data provided to partners for the calibration & the validation of advanced simulation tools.

Thank you!



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