Statistical Variability Analysis in 28nm UTBB FD-SOI devices

(Highlights from ECSEL JU Way2GoFast project)

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SUPERAID7 Workshop "Process Variations from Equipment Effects to Circuit and Design Impacts"
September 3, 2018, Dresden

Outline

Presentation

Introduction to project Way2GoFast

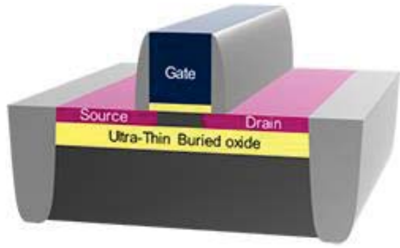
Statistical Variability analysis in 28nm FDSOI

Model for Circuit Design

Summary

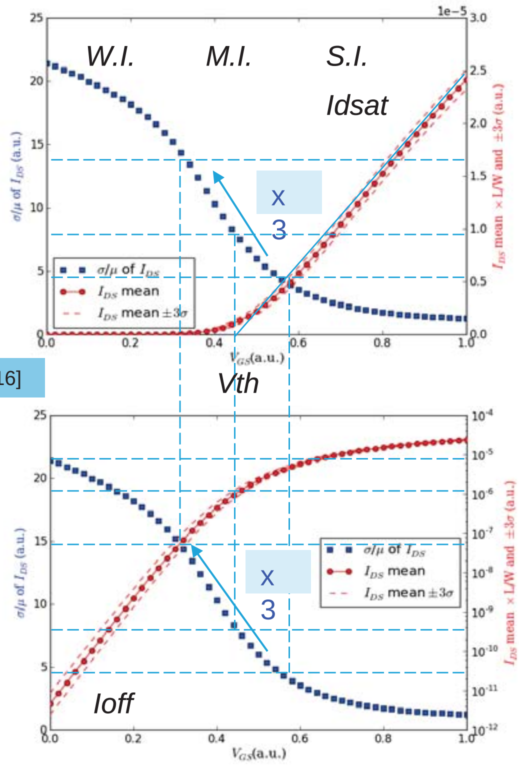
ECSEL Way2GoFast project

- UTBB FDSOI technology applications expand from Digital to mixed Digital-Analog-RF-mmW circuits
    - Market segments include Automotive, Connectivity, IoT, …
- Device Figures-of-merits (FoMs) addressed are multiple
    - Energy consumption remains as driving design parameter
    - Digital: Low dynamic power at given frequency, Low static power
    - Analog: Analog Gain, Variability (Matching, SCE), at low current
    - RF-mmW: High frequency response preserved at low voltage/low current



- Within ECSEL Way2GoFast project, during 2015 - 2017, 2 important developments were conducted in order to extend 28nm FDSOI technology applications to Low Power Digital-Analog-RF
    - Statistical Variability analysis, in cooperation with SYNOPSYS
    - Leti-UTSOI model enhancement for Low Power, in cooperation with CEA Leti

Variability Impact on Low Power Circuit Design



[SISPAD 2016]

- SV experiments in UTBB FDSOI
- Reduced Vdd or Id for Low Power
- Implies Near-Threshold operation
- SV impact x 3 from upper limit to lower limit of moderate inversion

- Objectives:
    - Device variability analysis
    - Model accuracy for circuit design throughout voltage range

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- **Characterization (Physical - Electrical)**
- TCAD device calibration (Physical - Electrical)
- GARAND device calibration
- Variability simulation with GARAND
- Device analysis

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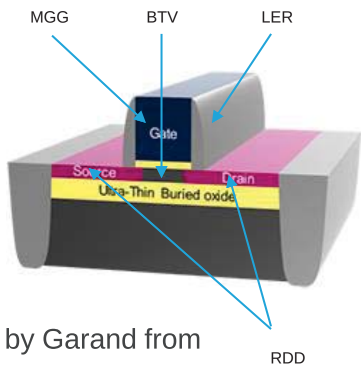
Summary

SV Characterization: Approach

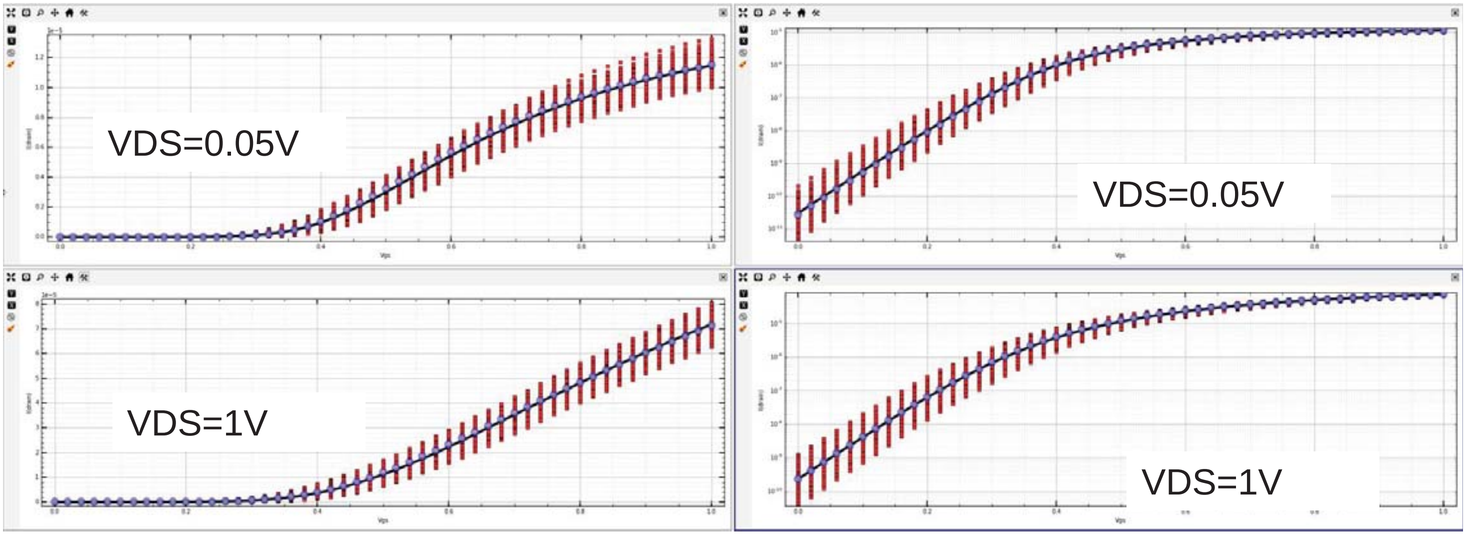
- Objective
  - To rely on most complete and consistent data set
  - Physical and Electrical characterization techniques
- Physical
  - Line Width/Edge Roughness (LWR/LER)
  - Metal Grain Granularity (MGG). Grain size & Orientation.
  - Body Thickness Variation (BTV)
  - Some unknowns remain
    - Random Discrete Dopants (RDD) -> Discrete profile determined by Garand from calibrated continuous doping profiles
    - MGG work-function values -> calibrated through variability simulation process
    - Statistical impact of trapped charges at the interfaces of the thin body channel



- Electrical
  - I(V) data from transistor array (256 pairs of DUT distributed in one direction), 1 die

Identification of median DUT

- One DUT selected as Golden from transistor array



Median
Golden DUT

Golden DUT closed to median I(V)
Small nMOS example

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TCAD device calibration (Physical - Electrical)

Garand device calibration

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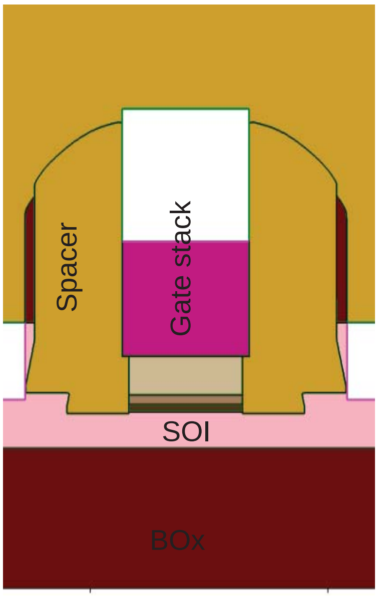
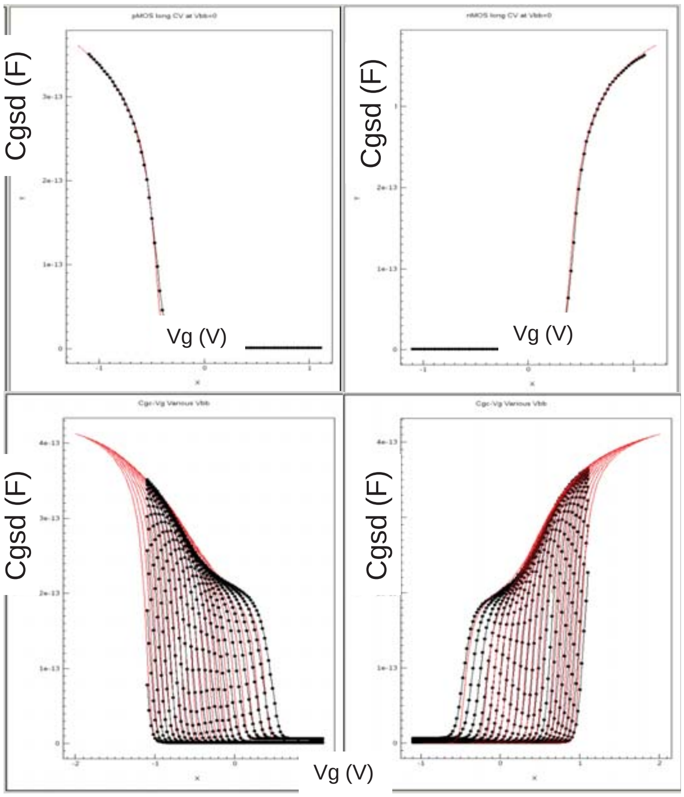
Sentaurus Device calibration: Electrostatic

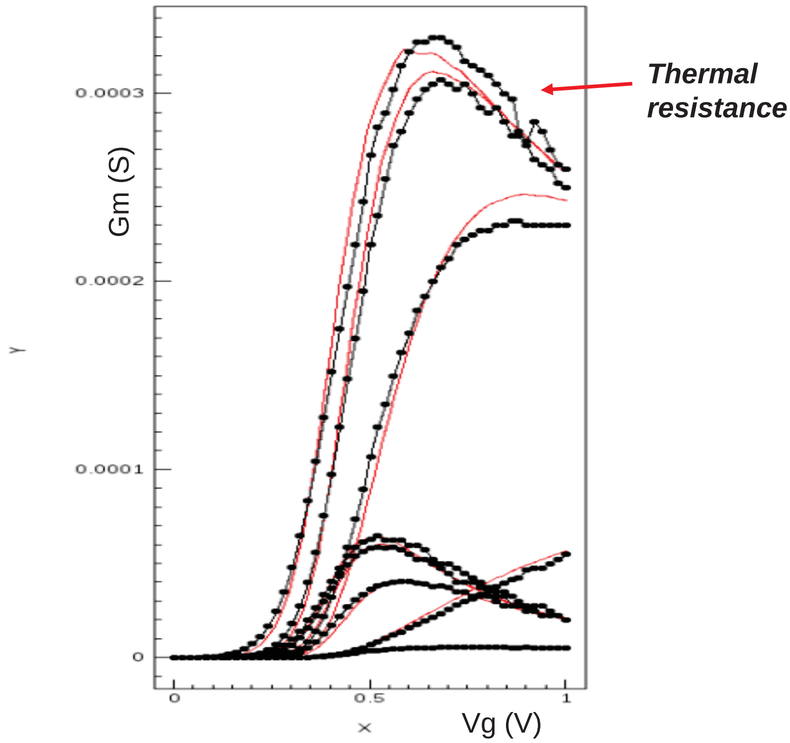




- CV at Vb=0
- Back and front inversion captured

Sentaurus Device Calibration: Transport

- Selected Models
  - Remote Coulomb Scattering
  - Remote Phonon Scattering
  - Ballistic mobility



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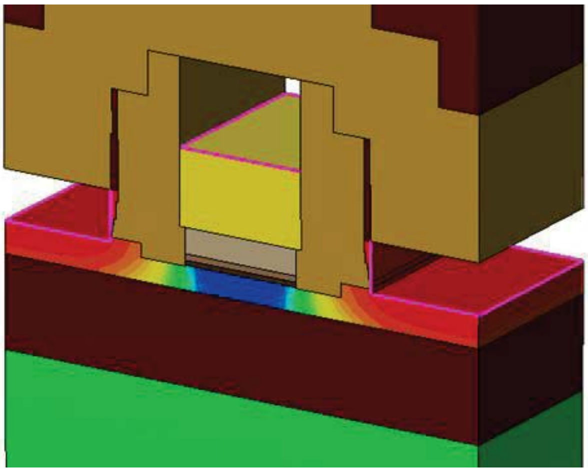
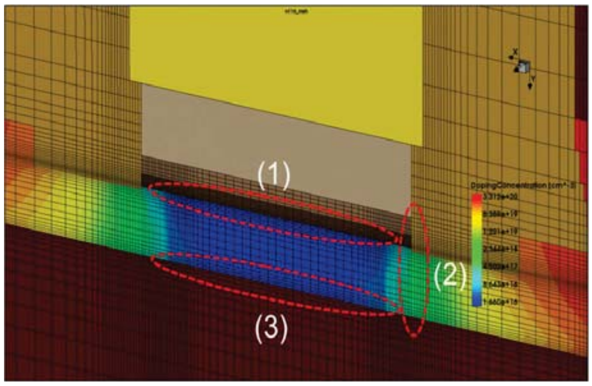
Simulation with Garand

- Device structure
  - Sentaurus 2D structure extended to 3D
  - Mesh refinement for regions (interfaces) exposed to LER and BTV
- Calibration strategy
  - Reference data: Device simulations from Sentaurus
  - Calibration Targets for Enigma tool
    - Charge distribution at middle of channel (density gradient DG)
    - Inversion charge Ninv vs Vgate voltage
    - Id (Vgate) at low and high Vd voltage for mobility fitting
  - Verification Cgg vs Vgate

Device structure

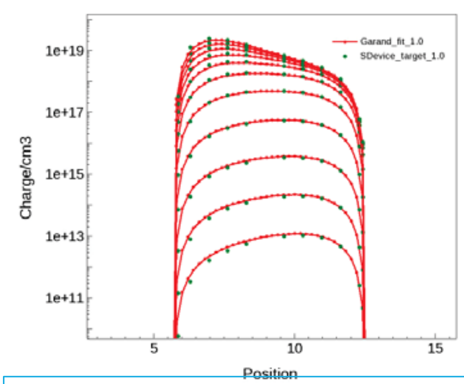


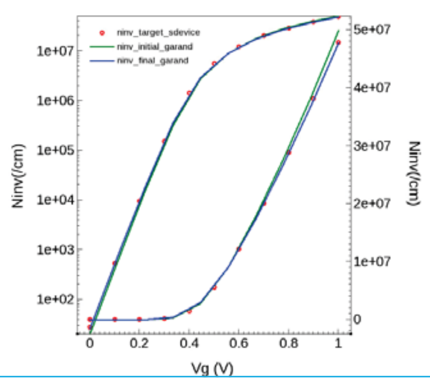


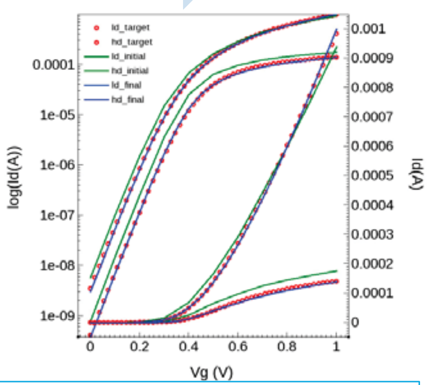
- Short gate length device extruded to 3D (left)
- Mesh refinement for regions exposed to LER and BTV (right)

Created Automated Garand Calibration flow for FDSOI technologies

Quantum correction [DG] calibration → Inversion charge [Ninv vs. Vg] calibration → Mobility Calibration



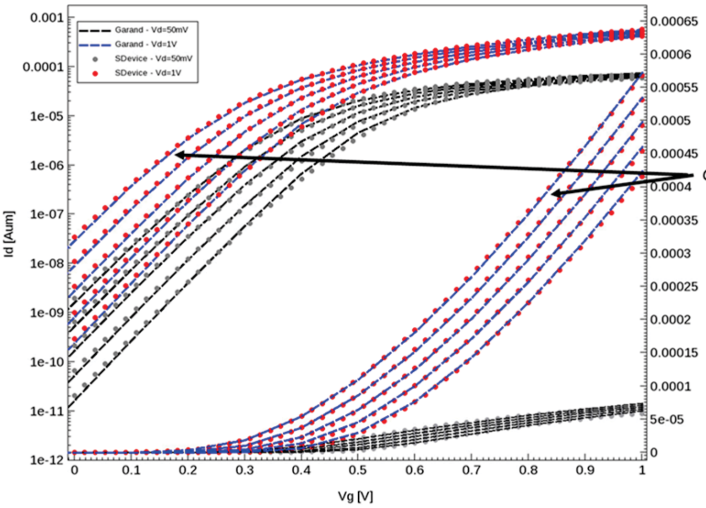


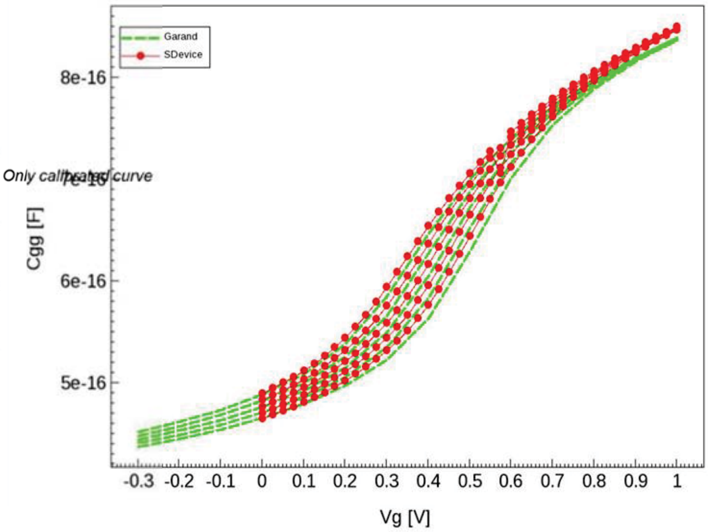


Developed during the project:

- Fully automated calibration for planar FDSOI technologies which enables Garand local variability analysis with an extremely low barrier-to-entry.
- Integrated into industry-standard framework tool Sentaurus Workbench.

Electrical inputs for Garand calibration





- Nominal DC calibration (Transport) over +/-1V BB *(Left)*
- Nominal AC verification (Electrostatic) over +/-1V BB *(Right)*

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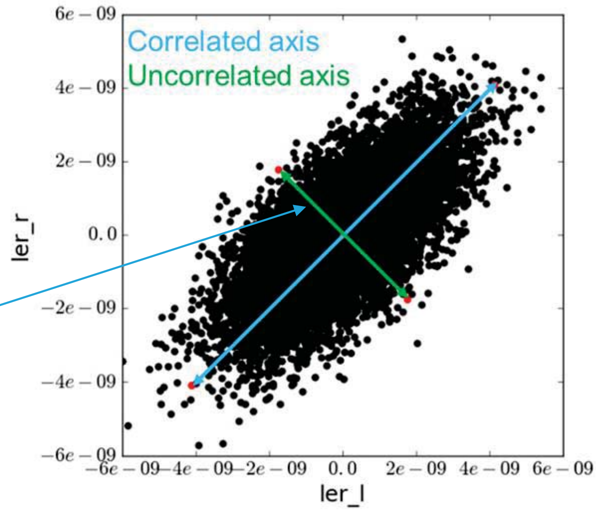
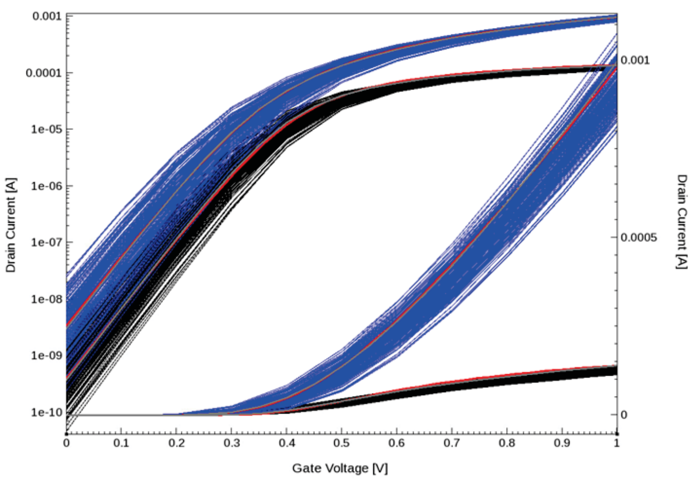
Local Variability inputs for Garand

Source	Parameter	comment
RDD	Supplied profile	Discretization by Garand
MGG	Average grain diameter	TEM data
	Orientation probability	TEM data
	Orientation Wf_delta	Literature for <111> & <200>, otherwise adjusted
LER	RMS	LER data wo edge/edge correlation
	LCOR	Best-guess
BTV	RMS	DRM/AFM data + adjust.
	LCOR	Best-guess

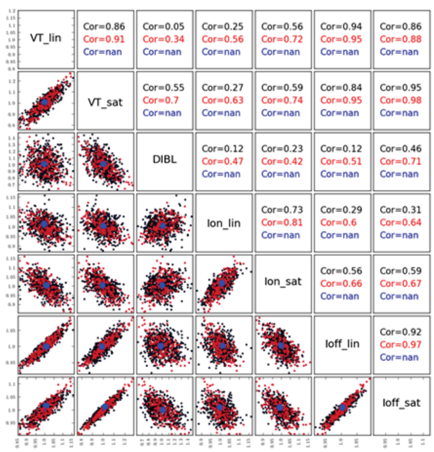


- Unknown parameters updated through iterative variability simulation (3-4)
- Enigma had to manage 2000 statistical simulations per iteration

Statistical Variability Analysis (nMOS)



- Simulation of nMOS Id(Vg) characteristics for 200 randomised devices



- Simulation/Hardware FOMs variations and correlations (normalized)

Sources contribution	σVT_{LIN}	σVT_{SAT}	σDIBL	σ ION_{LIN}	σ ION_{SAT}
RDD	3	3	3	**1**	2
LER	4	4	3	4	4
MGG	**1**	**1**	2	3	**1**
BTV	2	2	**1**	2	3

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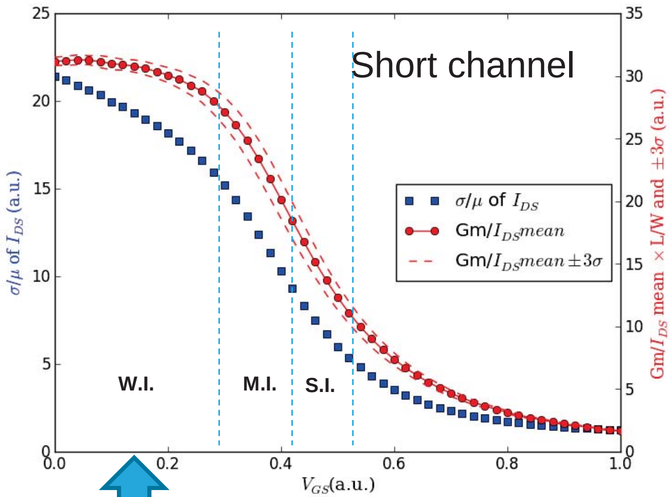
How gm/I accuracy serves statistical model accuracy?

Leti UTSOI enhancements for gm/I

Summary

How Gm/Id model accuracy serves statistical modeling?



- Strong inversion

$$Ids \propto \beta \times (Vgs - Vth - Dibl \times Vds)^a$$

$$\left(\frac{\sigma_{Ids}}{Ids}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\boldsymbol{gm}}{\boldsymbol{Ids}}\right)^2 \times [\sigma_{Vth}^2 + Vds \times \sigma_{Dibl}^2]$$

- Gm/Id is the amplification factor by which variability in electrostatics induces bias-dependent variability of current
- Applies for whatever inversion regime
- Gm/Id accuracy helps variations modeling

- Weak inversion

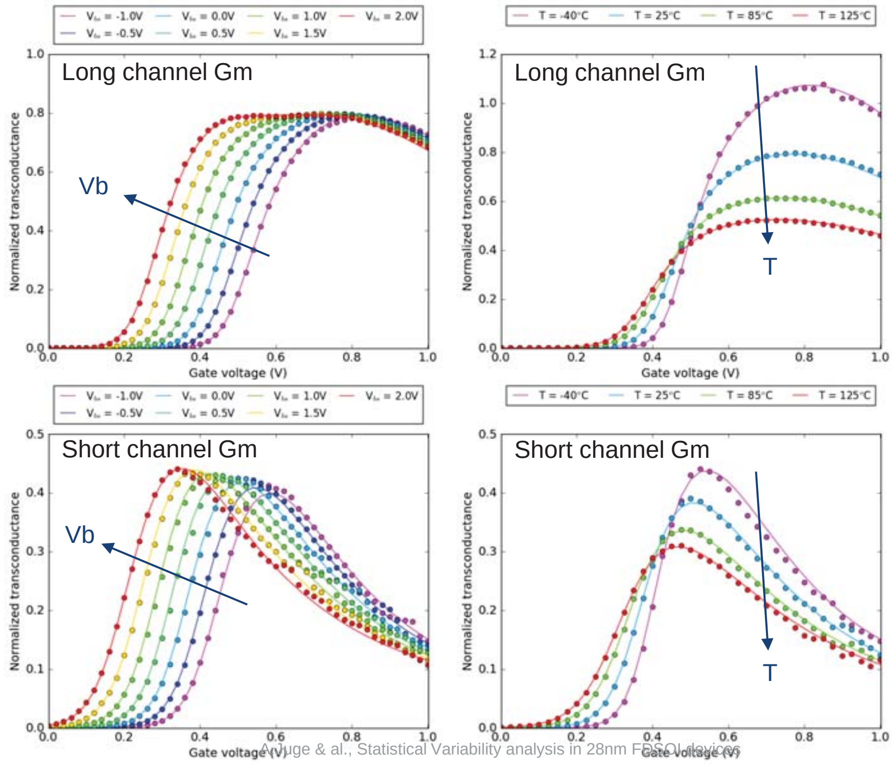
$$Ids \propto \beta \times \exp\,(Vgs - Vth - Dibl \times Vds)/\,(n \times ut))$$

$$\left(\frac{\sigma_{Ids}}{Ids}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\boldsymbol{gm}}{\boldsymbol{Ids}}\right)^2 \times \left[\sigma_{Vth}^2 + Vds^2 \times \sigma_{Dibl}^2 + (Vgs - Vth)^2 \times \left(\frac{\sigma_n}{n}\right)^2\right]$$

[SISPAD 2016]

Leti UTSOI model enhancement for Gm/I

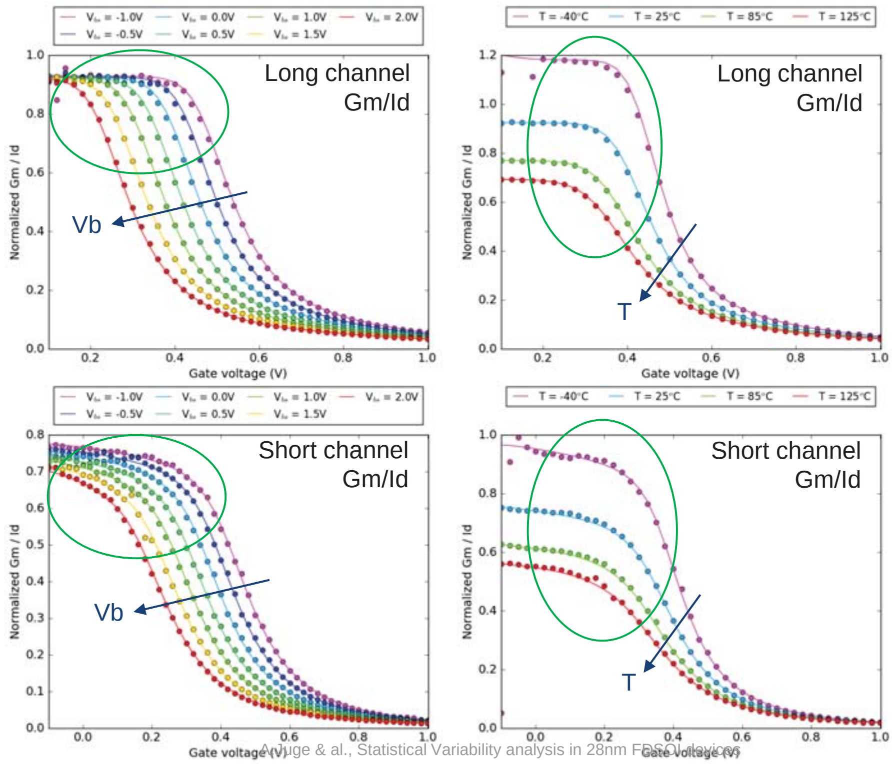
- Mobility and series resistance model improvements



- Refined model for Coulomb scattering dependence with transverse field
- Refined model for series resistance dependence over back bias

Leti UTSOI model enhancement for Gm/I

- Improvement of accuracy in moderate inversion region



- Refined modeling of source/drain depletion as a function of longitudinal field

Summary

- Modelling for Low Power Analog-RF in 28nm FDSOI technology highlighted
  - Support of ECSEL JU Way2GoFast project
  - Cooperation between CEA Leti, Synopsys, and ST
- Physical/Electrical characterization methodologies suited for FDSOI devices
  - Some unknown parameters remain (Work-function values per grain orientation)
- Variability analysis with Garand
  - Provided well-calibrated TCAD deck, and set of physical/electrical variability data, Garand can predict the local variability, including key figure of merit sigmas and correlations
  - Tool chain capabilities were extended (MGG,..).
  - Enigma provides capability of reverse-engineering to provide physical inputs not available
  - Calibration methodology ensures consistent variability inputs for nMOS and pMOS devices
  - Comprehensive analysis of statistical variability observed in 28nm FDSOI device characteristics
  - Classification of local variability sources provides guidance for LP device optimization
- Leti-UTSOI model for Low Power Circuit Design
  - Accuracy in Gm/Id metric is valuable for Variability modeling
  - Leti-UTSOI qualified for Low Power Analog-RF circuit design using 28nm FDSOI technology

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Thank you for your attention !