Process Variability and the SUPERAID7 Approach

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ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

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Outline

- Introduction
- Background pillars and new challenges
- Consortium and project data
- SUPERAID7 project structure
- Methodology used
- Examples for impact of process variability
- Conclusions and Outlook

Introduction – Importance of Variations

- ITRS 2013 Modeling and Simulation chapter:
  - One of 7 “Near-term difficult challenges (2013-2020)” “Hierarchical simulation”, with issues among others
    - “Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations” and
    - “Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently”
  - One of 12 Technological Requirements: “Modeling for Design Robustness, Manufacturing and Yield”

⇒ SUPERAID7: Development of a software system for the simulation of the impact of all kinds of process variations (including their correlations) on devices and circuits

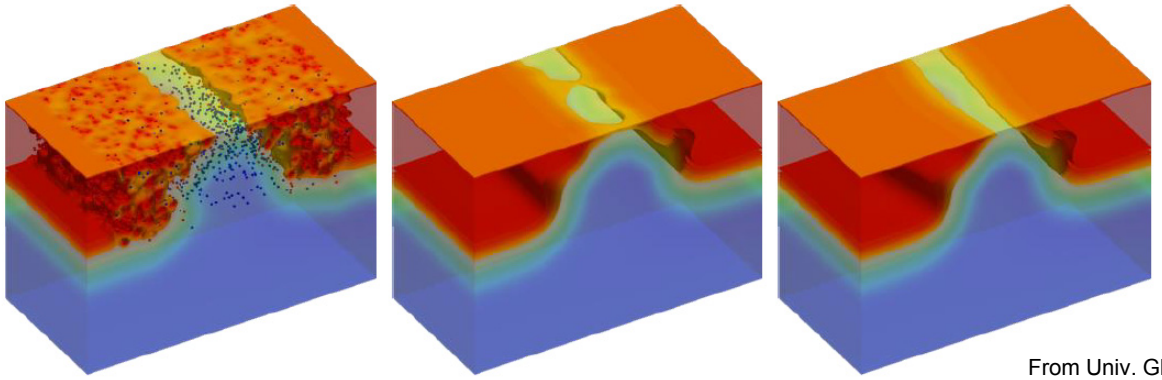
Introduction: Variations

- Numerous sources of process variations potentially influence the performance of active devices, interconnects and circuits:
  - Stochastical process variations resulting from the granularity of matter
  - Layout-induced process variations
  - Systematical variations resulting from non-idealities of process equipment
- Adequate assessment of the impacts of process variations requires to trace their effects from their source up to device / interconnect / circuit level
  - Same source of variations may influence various process results – e.g. sizes of different features, even in case of different nominal values
  - Correlations of variations of different process results must be traced and their impact on device and circuits assessed

Introduction: Stochastical Variations

- Stochastical variations caused by the granularity of matter
  - Random Dopant Fluctuations RDF
  - Line Edge Roughness LER
  - Metal Grain Granularity MGG

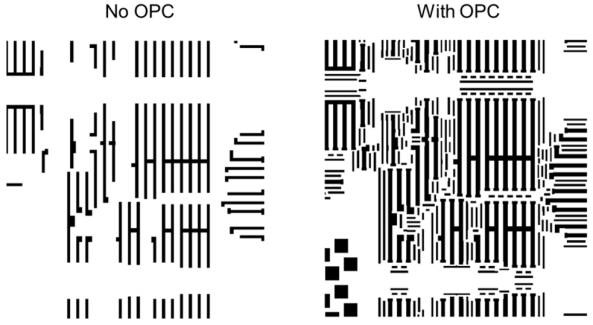
  discussed since long in the literature esp. for bulk devices



From Univ. Glasgow

Introduction: Layout-induced Process Variations

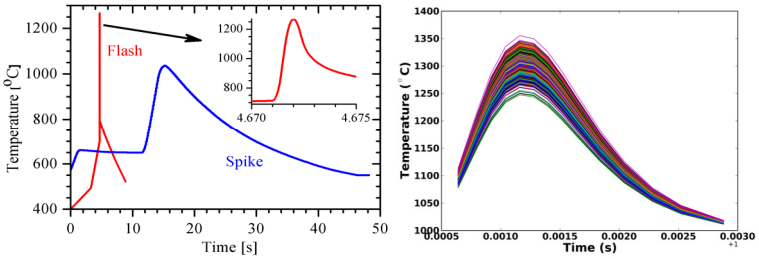
- Well known in the lithography community:
  - Printing of features influenced by other near-by features
  - Routinely considered in design: "Optical Proximity Correction" OPC
- So far hardly considered in other process steps, e.g.:
  - Pattern-dependent effects in deposition, etching (,CMP)
  - Pattern-dependent temperature profiles in millisecond / spike annealing, due to changes in reflectivity
  - …..



From Fraunhofer IISB

Introduction: Systematic Process Variations

- Caused by non-idealities / drifts of equipment parameters
  - Lithography esp. defocus, illumination dose / threshold
  - Deposition / etching: Variations across / between wafers due to inhomogeneity in gas flow and temperature distributions; source characteristics
  - For low-energy / Plasma Immersion Implantation: Variations in tilt and rotation angle ⇒ variations in residual channeling
  - Millisecond / flash annealing: Not completely reproducible temperature profiles



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Background Pillars and New Challenges

- SW / model background:
  - Advanced physics-based programs for the simulation of lithography, deposition and etching (Fraunhofer IISB, TU Wien)
  - Statistical device simulator GARAND (originally GSS/GU), plus compact model extraction tools
  - Background models / modeling expertize for processes, devices and circuits (all partners)
  - Process integration results from advanced sub-10nm semiconductor technology (CEA/Leti)
  - Where appropriate: Use of commercial equipment / plasma simulation tools (e.g. Q-VT) and commercial process / device simulation tools (Sentaurus from Synopsys)

Background Pillars and New Challenges

- Preceding EU FP7 project SUPERTHEME (Circuit Stability Under process Variability and Electro-Thermal-Mechanical Coupling, 10/2012-12/2015)
  - Hierarchical simulation of the impact of process variations on bulk devices, including esp. *More than Moore* devices
  - Quantification of sources of process variations, by 4 equipment company partners
  - Highly three-dimensional devices necessary for sub-10 nm node not considered – except for idealized FinFET structure
  - See www.supertheme.eu

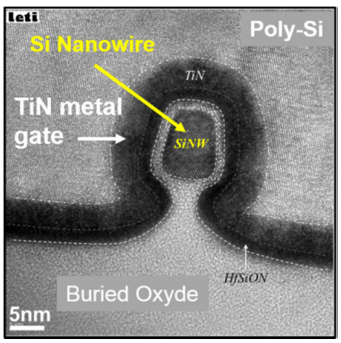
SUPERTHEME

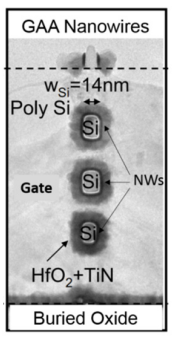
Background Pillars and New Challenges

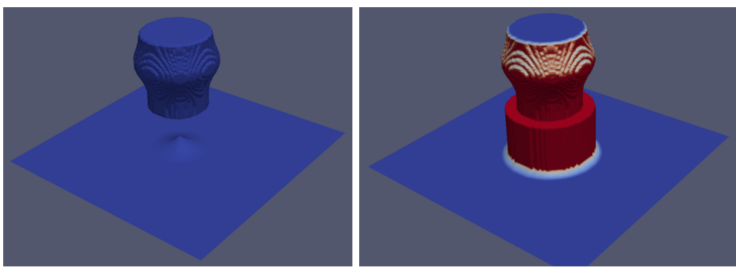
- New challenges for SUPERAID7 (I)
  - Sub-10nm devices such as (stacked) nanowires / nanosheets are highly three-dimensional and have non-ideal shapes

    ⇒ Accurate 3D simulation of topographies incl. their variability mandatory

    ⇒ Development of an integrated physics-based topography simulator (lithography/deposition/etching) necessary & one core activity in project



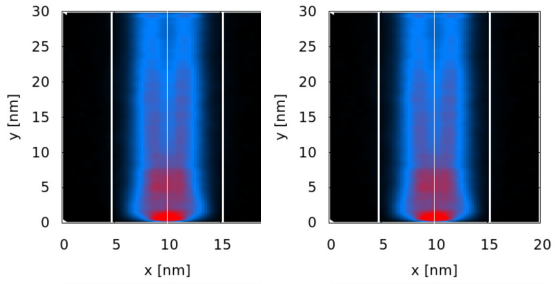




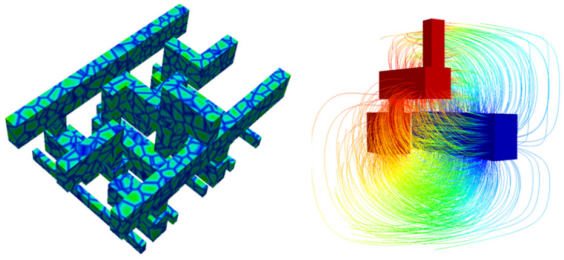
Left: SEM micrographs of nanowires (from LETI);
right: Coupled litho/etching simulation (from Fraunhofer IISB)

Background Pillars and New Challenges

- New challenges for SUPERAID7 (II)
  - Small feature sizes and /or rough interfaces necessitate refined and efficient modeling of quantum effects
    ⇒ Improved models for carrier transport in nanowires being developed: Confined carrier transport models
  - Interconnect performance, reliability and variability increasingly important for aggressively scaled devices
    ⇒ Development of physical models for interconnect simulation



Electron density in ideal and rough nanowire (from TU Wien)



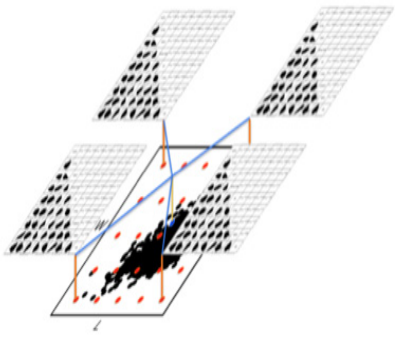
Interconnect structure for 14 nm FinFET based double inverter – Metal Line Granularity and electrical field lines (from Synopsys)

Fraunhofer IISB

SUPERAID 7

Background Pillars and New Challenges

- New challenges for SUPERAID7 (III)
  - Existing compact models not applicable to highly three-dimensional device structures as addressed in SUPERAID7
    ⇒ Development /extension / use of new compact model LETI-NSP
  - Compact models to include variations of complicated device geometries
    ⇒ Traditional approach based on small set of simple geometrical parameters (e.g. 3*3 matrix of gate transistor length and width) no more applicable
    ⇒ Use varying process parameter itself as variable



From GSS/Synopsys

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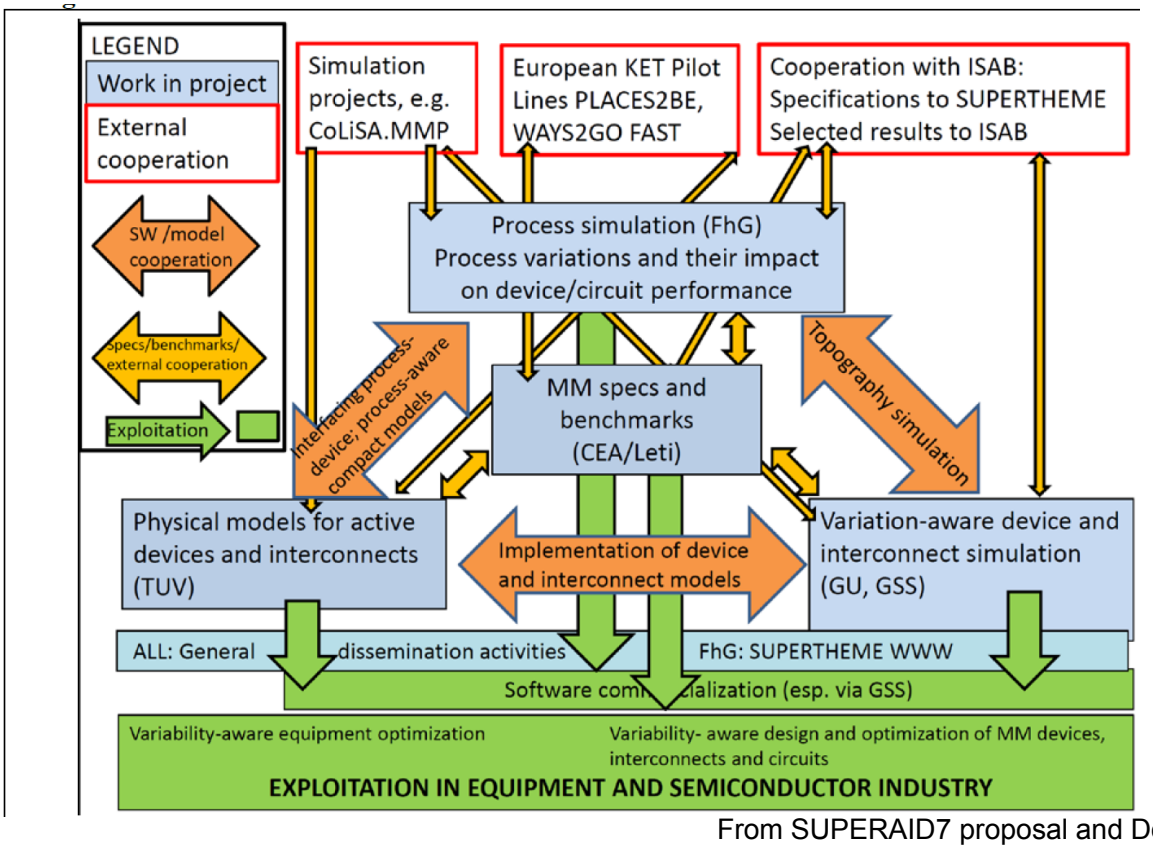
SUPERAID 7

Consortium and Project Data

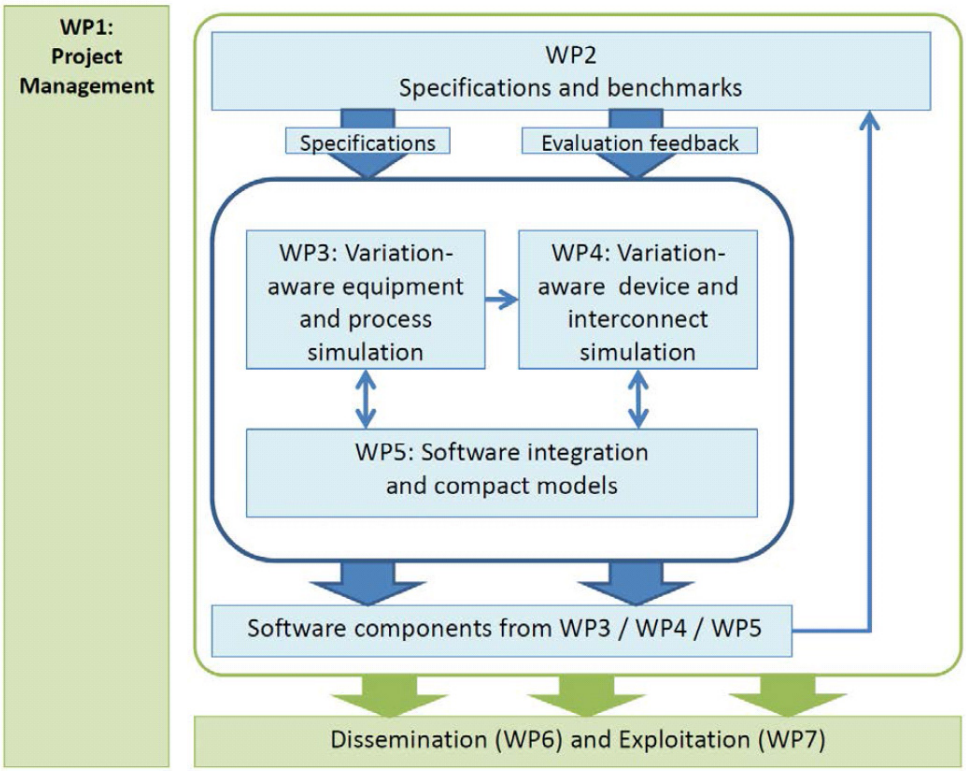
- Project partners
  - Research institutes: Fraunhofer IISB (coordinator), CEA/Leti
  - Universities: University of Glasgow, TU Wien
  - SW house: GSS – replaced July 2017 by Synopsys (due to take-over)
- Project duration: 01/2016 – 12/2018
- EC funding: 3377527.50 Euros from H2020 call ICT-25-2015 “Generic micro- and nano-electronic technologies
- See www.superaid7.eu

SUPERAID7 Project Structure



From SUPERAID7 proposal and DoA

SUPERAID7 Project Structure



From SUPERAID7 proposal and DoA

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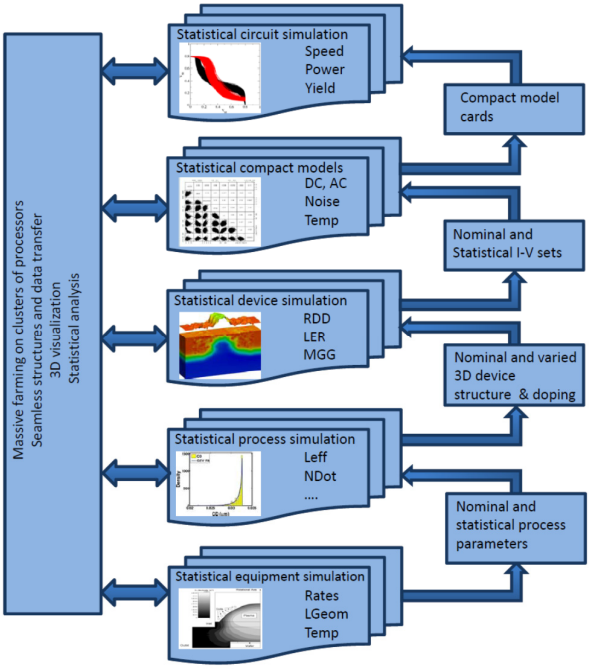
SUPERAID 7

Methodology Used: SW Architecture

- Equipment simulation: Use of external tools to derive variations of etching and deposition rates
- Process simulation: Development of a new integrated topography simulator. Use of Sentaurus Process for the doping steps
- Device simulation: Extension of statistical device simulator GARAND
- Prototype tool for interconnect simulation
- New compact model for 3D devices
- Extension of variability-aware compact modeling approach



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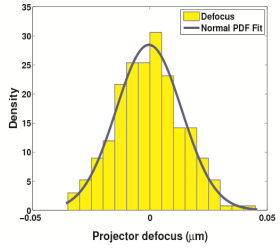
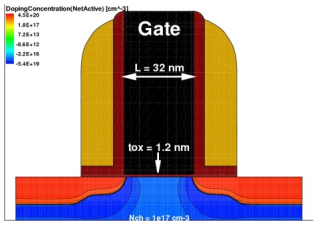
Methodology Used: Compact Model Extraction

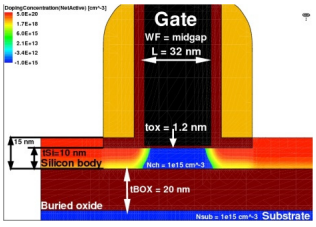
- Approach modified from procedure used in SUPERAID7 and published earlier:
  - LETI-NSP for compact modeling
  - For systematic variations: First identify those most relevant for device / circuit in question, considering each of them in isolation ⇒ limitation of DoE space from many to typically 2 or 3 parameters
  - Statistical compact model extraction as before: Three step extraction of statistical compact models including statistical variations (RDF, LER, MGG) for set of nominal devices, including the dependence on device geometry
  - Traditional approach: Convolution of statistical compact models with PDFs of relevant varying geometrical process results (e.g. gate length/width)
  - Modification: Variation of 3D device shape cannot always be described by physical parameters like length and width ⇒ partly include varying process inputs parameter into compact model extraction

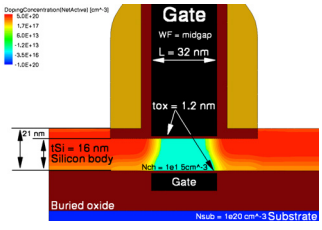
Example 1: Device Architectures as Filter for Variations

Impact of lithography focus variations on transistor performance





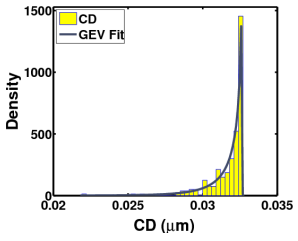


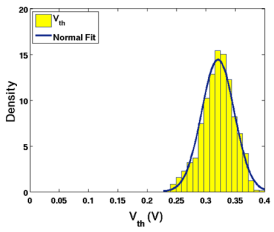


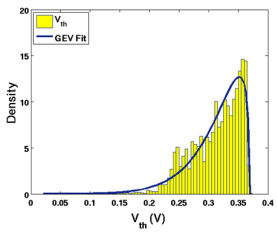
Focus variations ⇓ CD variations

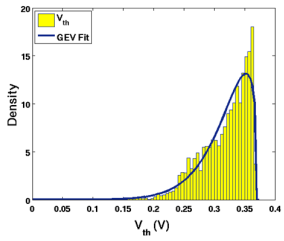
Device architecture: Bulk | SG FD SOI | DG FD SOI

acts as filter for CD variations and leads to variations e.g. of V_{th}





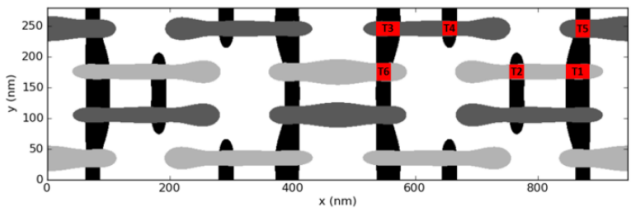


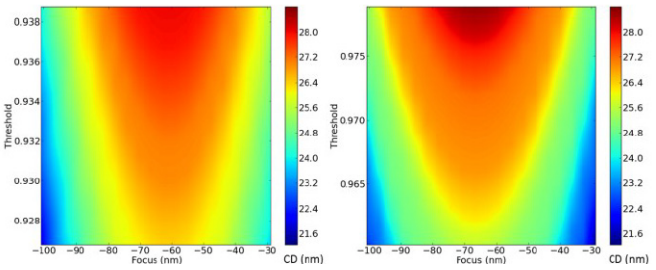


J. Lorenz et al., *Proc. 2009 Intl. Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, 2009, pp. 17-18.

Example 2: Impact of Correlations

- Impact of lithography defocus and dose/threshold variations on SRAM cell based on 20 nm / 25 nm gate length FinFET technology
  - LELE double patterning used
  - ⇒ Poly mask layer is split into two incremental mask layers, with statistically independent variations
  - ⇒ Variations correlate within transistor groups T1/T2/T6 and T3/T4/T5, but not between them. Example: PDF of gate length for T2 and T4.

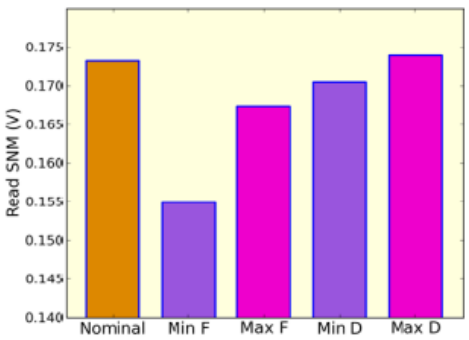


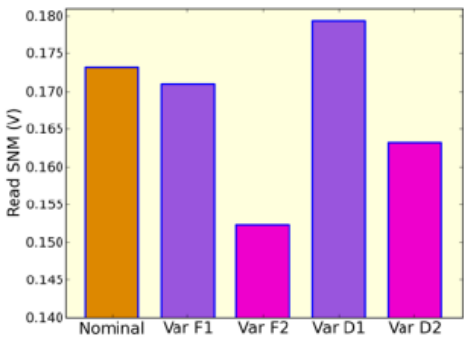


From P. Evanschitzky, A. Burenkov, J. Lorenz, Proc. SISPAD 2013

Example 2: Impact of Correlations

- Impact of lithography defocus and dose/threshold variations on SRAM cell based on 20 nm / 25 nm gate length FinFET technology
  - Different PDFs for channel lengths of the transistors
  - SRAM: Signal Noise Margin depending on variations and their correlations:
    - Left: Correlated variations – either all minimum or all maximum values
    - Right: Anticorrelated variations

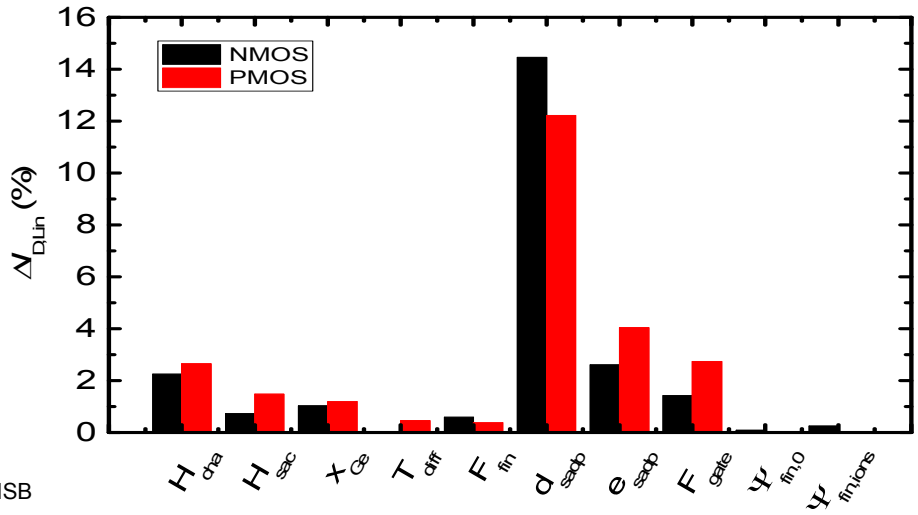




From P. Evanschitzky, A. Burenkov, J. Lorenz, Proc. SISPAD 2013

Example 3: Screening for most relevant systematic process variations

- Example for a nanowire process from CEA/LETI
  - Most relevant variations are SiGe mole fraction x_{Ge}, the fin SADP deposition factor d_{sadp} and the gate litho defocus.



From Fraunhofer IISB

Conclusions

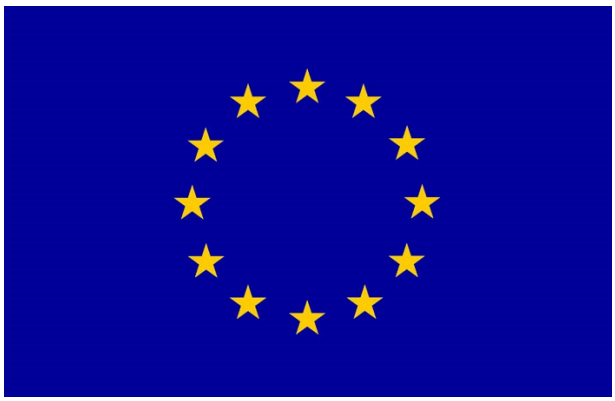
- The impact of various kinds of systematical and stochastic variations on sub-10nm devices and circuits is important and needs to be assessed and minimized
- A hierarchical simulation approach is necessary and presented in this workshop to deal with the impact of variations, ranging from equipment simulation to statistical device simulation and compact model extraction
- Accurate and efficient process and device models are needed for variability studies
- The most relevant sources of variations must be identified and used in a DoE to minimize the complexity of simulation
- Systematic variations may influence several quantities in parallel, and partly cause correlations between these quantities. Such correlations must be considered in circuit simulation

Outlook

- The importance of process variations and of the simulation and minimization of their impact will be further growing
- The approach presented in this workshop needs to be customized to the industrial process flow in question, especially regarding the large variety of systematic process variations which depend on details of the technology used.
- Work within SUPERAID7 and at its partners on the further extension of variation-aware compact models is ongoing

Acknowledgements

- Contribution of all colleagues at partners highly appreciated
- Valuable inputs from EC review team and from SUPERAID7 ISAB
- Funding from EC highly appreciated



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THANK YOU FOR YOUR ATTENTION!