# Simulation Tools for DTCO of Advanced Technology Nodes

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ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

September 3, 2018, Dresden, Germany

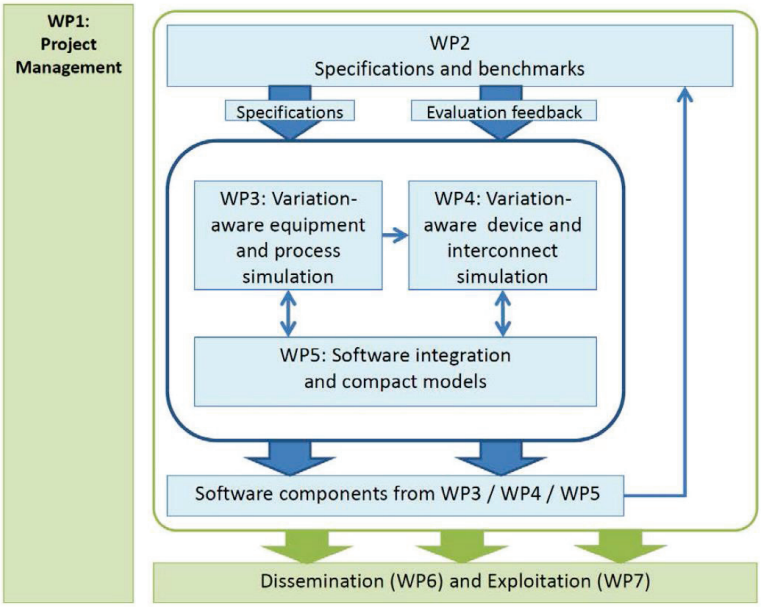


## Outline

- Introduction
  - Project Context and Goals
- DTCO and Technology
- Tools and Software for DTCO
- Example FinFET PPY Analysis
- Conclusions and Outlook

# Introduction – Project Context

- Synopsys/GSS contributions are utilizing inputs from many WPs and partners.
- Tools and methodologies developed as part of WP3 and 4
- Extensive R&D into toolchain and data integration carried out in WP5
- Inputs and integration with tools and flows from WP3

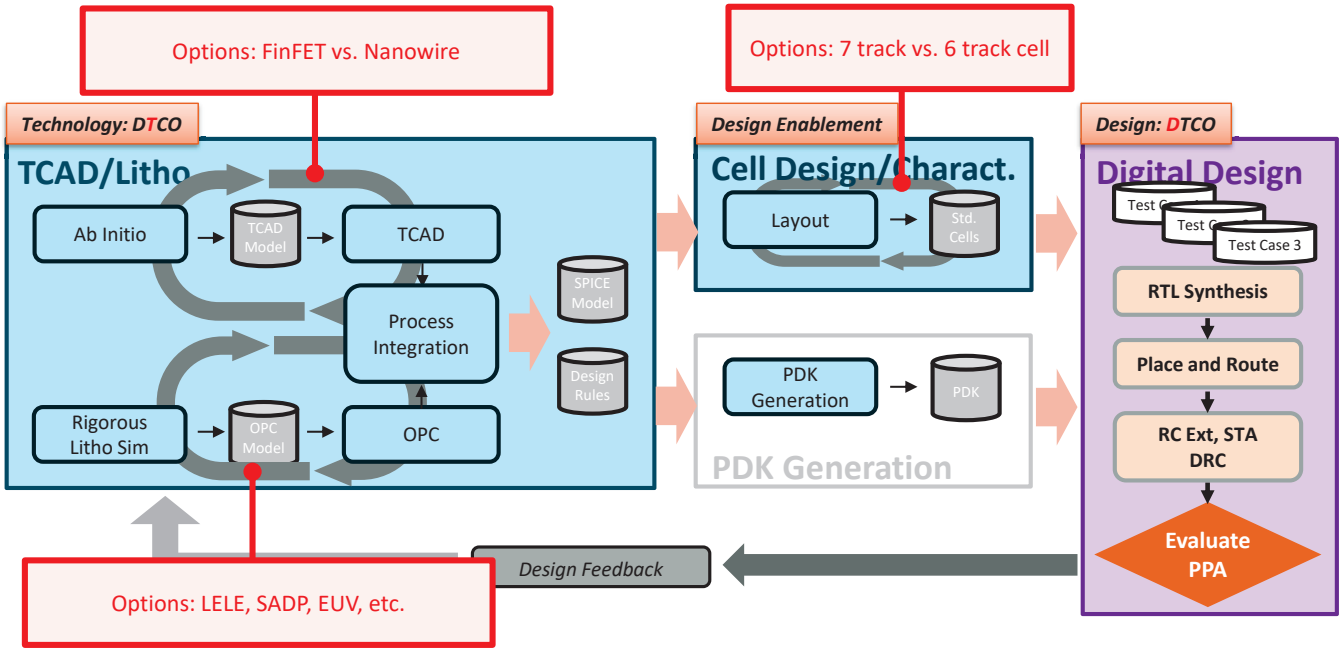





# Introduction: The DTCO Concept

- What is Design Technology Co-Optimisation (DTCO) ?
  - A holistic approach to the development of technology and design in order to deliver an optimal product.
- DTCO is utilised in Foundries but it based on Silicon which limits turnaround and number of possible options
- Simulation based DTCO provides an efficient and rapid methodology for the estimation of PPA (Y)
  - Architecture choices
  - Process options
  - Performance booster assessment
  - Design rule optimisation
  - Assessment of the impact of process choices on PPA(Y)

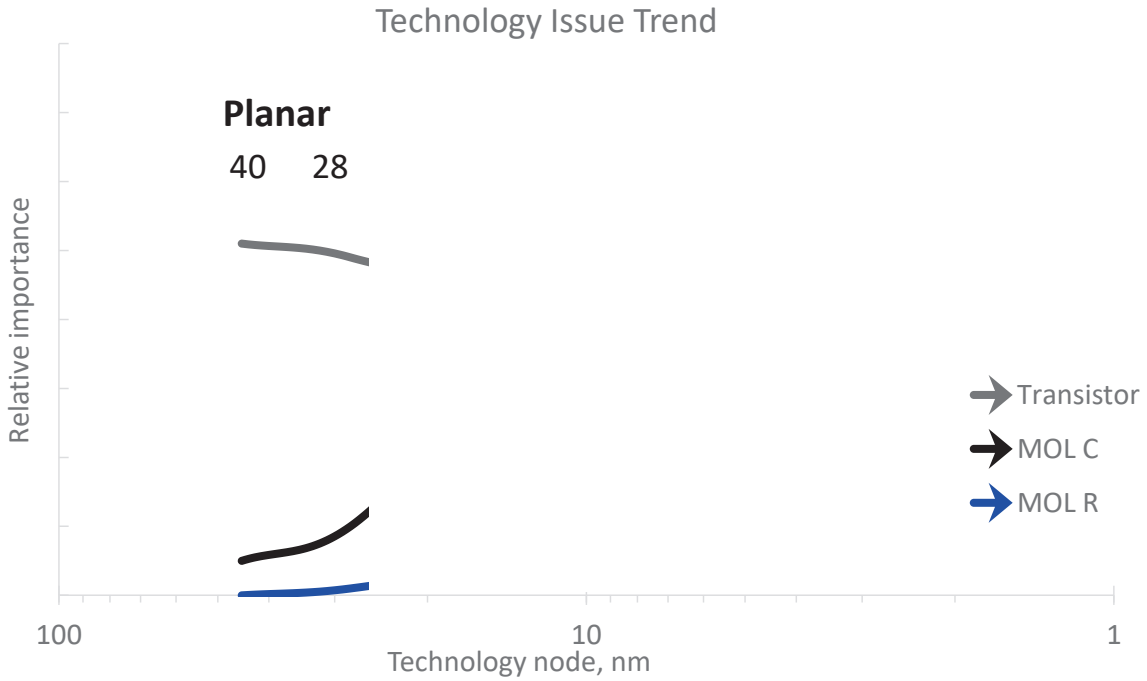
# Introduction: The DTCO Concept





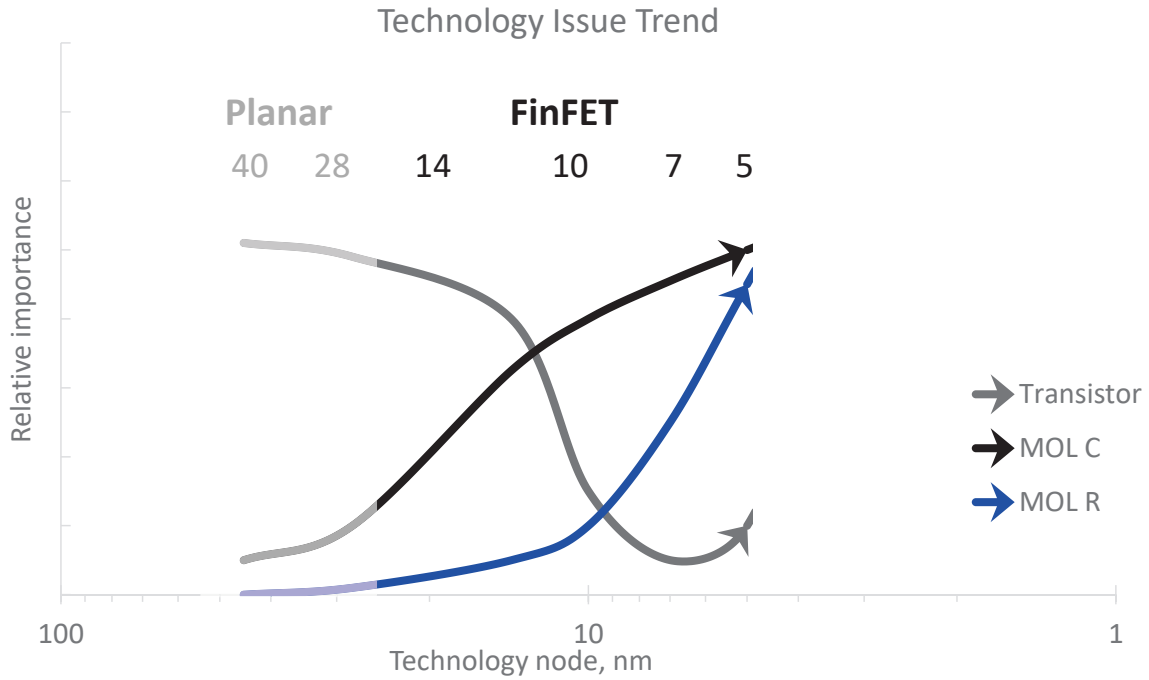



# Major Technology Issues Addressed by DTCO




- For planar MOSFET, DTCO was mainly about transistor tuning

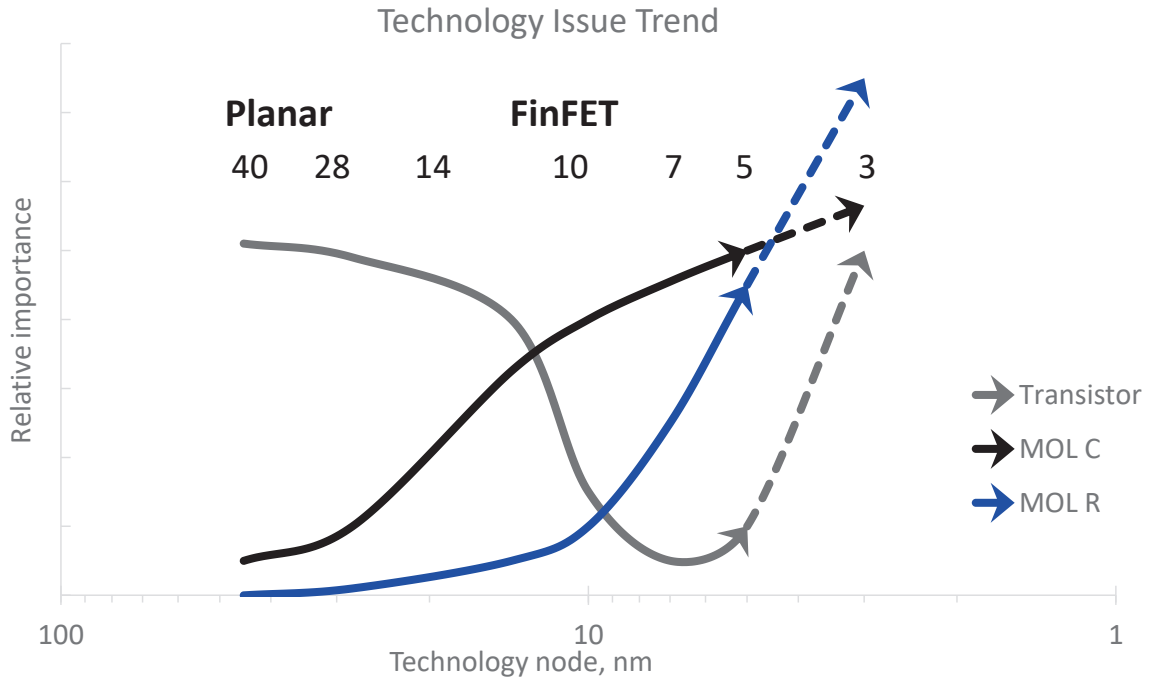
# Major Technology Issues Addressed by DTCO




- For FinFETs, transistors became less of an issue
- MOL capacitance became a critical issue instead
- At 7nm, MOL resistance emerged as a critical issue and it keeps getting worse with scaling

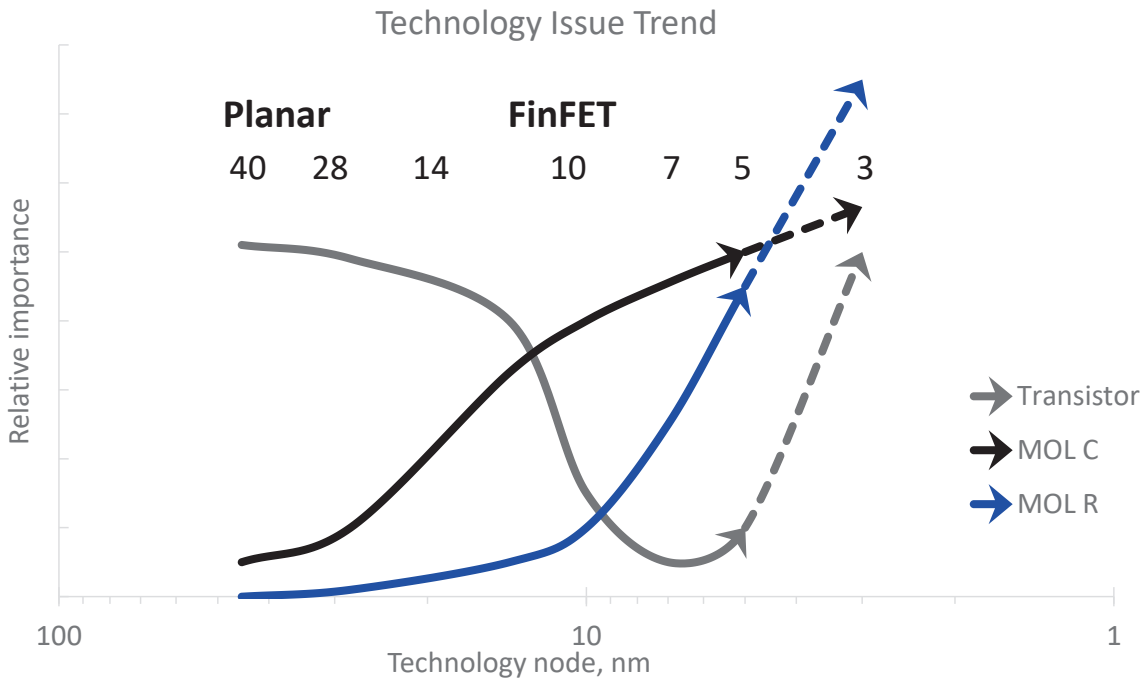


# Major Technology Issues Addressed by DTCO




- The potential transition to nano-wires or nano-slabs brings back the focus on transistor
- PEX issues are only getting worse with scaling

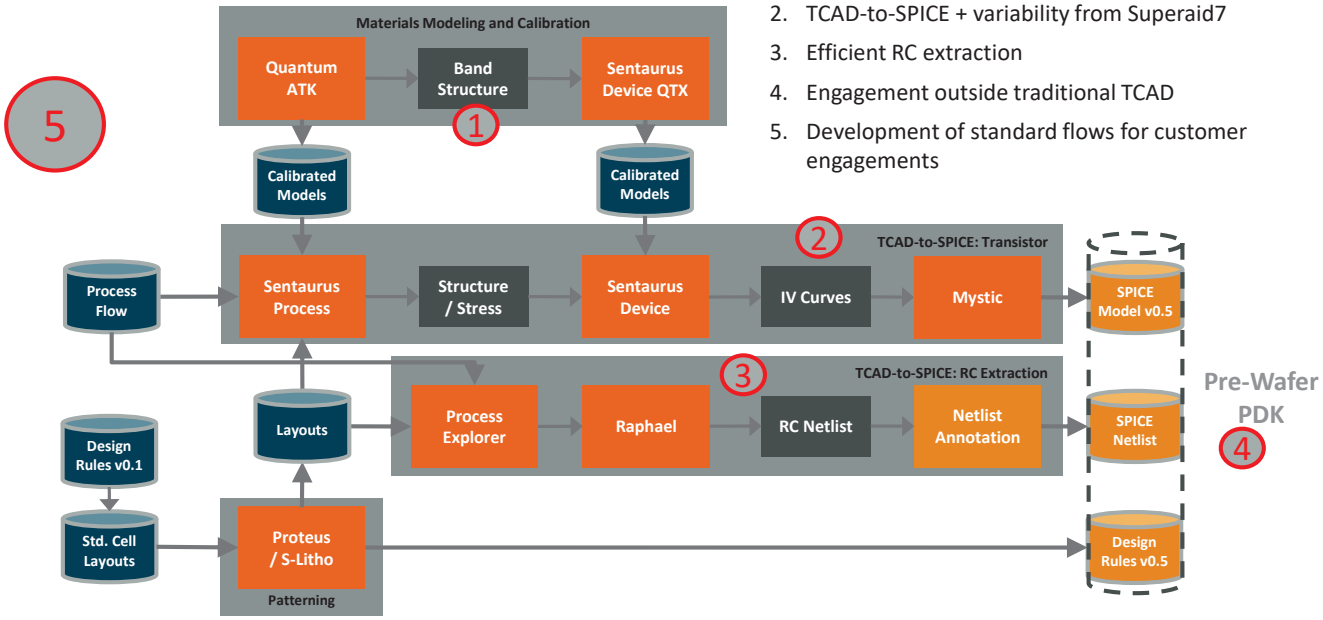
# Major Technology Issues Addressed by DTCO




- The potential transition to nano-wires or nano-slabs brings back the focus on transistors
- PEX issues are only getting worse with scaling: C and R
- **DTCO tool flows address all of these issues simultaneously!**



# Example : Pre-Wafer DTCO *Flow*



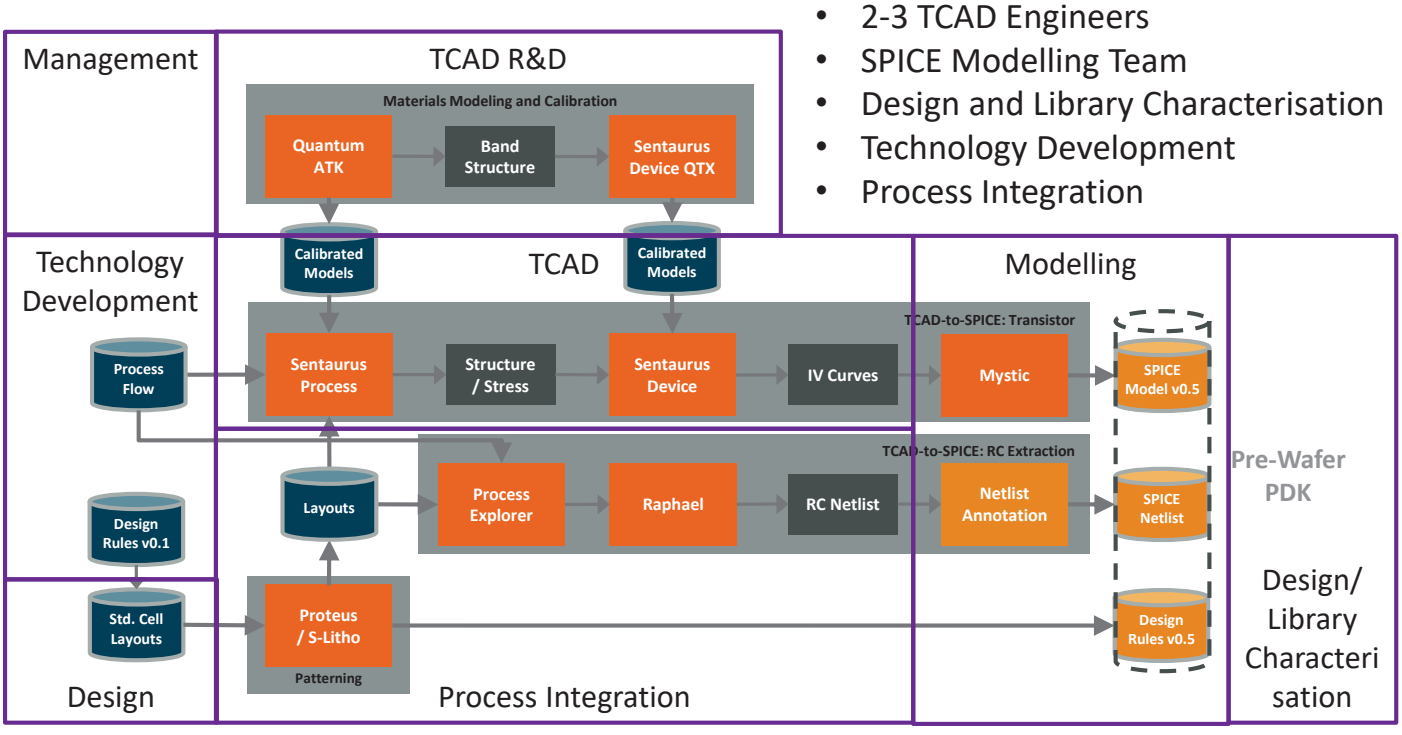

1. Materials Modelling and predictive simulation.
2. TCAD-to-SPICE + variability from Superaid7
3. Efficient RC extraction
4. Engagement outside traditional TCAD
5. Development of standard flows for customer engagements

# Superaid7: DTCO Tool Flows

- DTCO tool flows are complex and non-linear
  - Requires interaction between expert users with domain specific knowledge
  - Require efficient information interchange
  - Need highly integrated and robust tools (WP4)
- Addressed in Superaid7 via
  - Development of integrated DCTO workflows in WP5
    - Toolchain integration via Enigma, SWB and Data management
  - Advanced spice modelling methodologies
    - Capturing process and statistical variability
  - Significant automation
    - Device simulator autocalibration
    - RC extraction



# Example : Pre-Wafer DTCO *Flow*




- 2-3 TCAD Engineers
- SPICE Modelling Team
- Design and Library Characterisation
- Technology Development
- Process Integration

# FinFET DTCO Example

Aims

- Provide a SPICE model with variability capabilities
- TCAD as the primary (only) calibration data provider
- Enable users to perform
  - Quick PPA analysis
  - Process optimisation
  - Process corner analysis

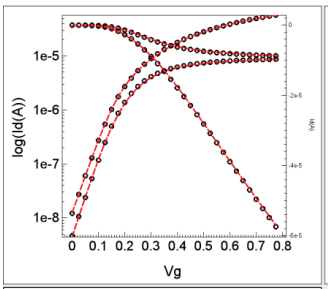






# Base model extraction - Mystic

Automated spice model extraction methodologies and software. (WP4)




*nMOS IV/CV characteristics*

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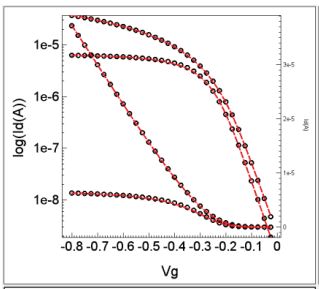


*pMOS IV/CV characteristics*

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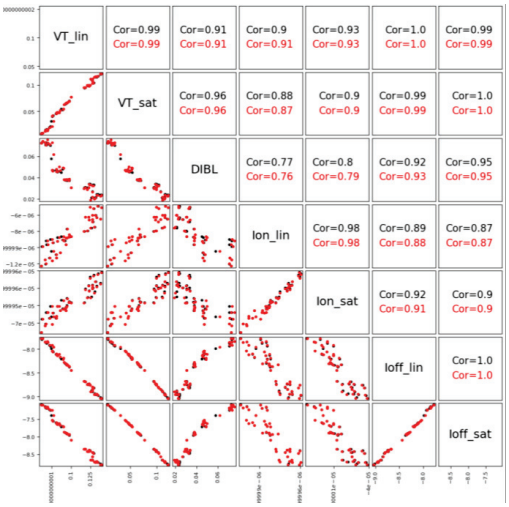
# Base model extraction - Mystic

- Script based Mystic extraction.
- Targeting robustness and re-usability.
- Linked to TCAD
  - Sprocess and Sdevice via SWB and Enigma
- 14nm FinFET example:
  - ***86 TCAD splits*** and ***5 process variations*** modelled.
  - Single extraction strategy.

| Parameter | Nominal | Range | Comment |
|---|---|---|---|
| L | 25 | +/- 2nm | Gate length variation |
| H | 40 | +/-2nm | Gate height |
| W | 8 | +/-2nm | Fin thickness |
| A_fin | 88 | +/-1 | Fin angle factor |
| T_spacer | 8 | +/-2nm | Spacer thickness |

*nMOS fitting across the DoE:*



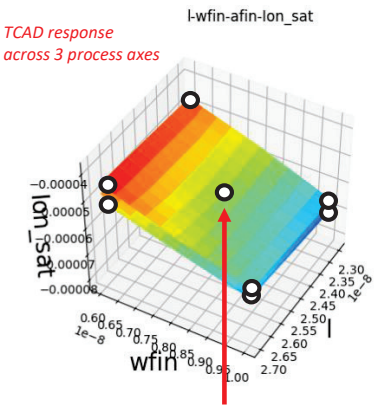





# Process variation modelling

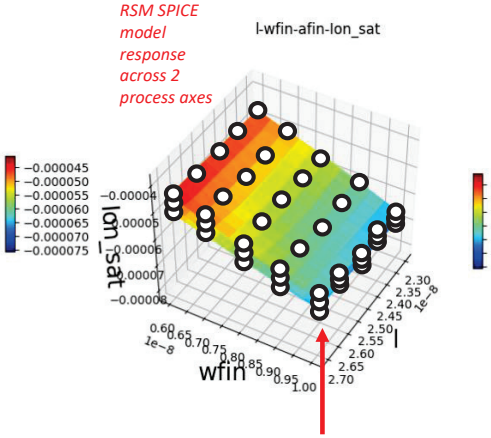
- TCAD to SPICE approach w/RandomSpice allows users to generate a response-surface model to handle arbitrary process variations
  - Spice modelling methodology developed as part of WP5

*TCAD response across 3 process axes*



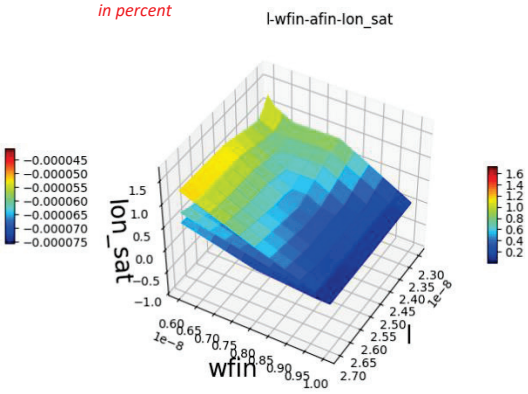

*TCAD simulation points: 5 axis optimal grid = **43 TCAD simulations***

*RSM SPICE model response across 2 process axes*




*SPICE model simulation points 5 axis full grid = 5^5 = **3125 SPICE simulations***

*Relative error in percent*



# Process variation modelling

- Allows users to evaluate circuit behaviour across a wide range of process splits (as well as interpolating between TCAD simulation points

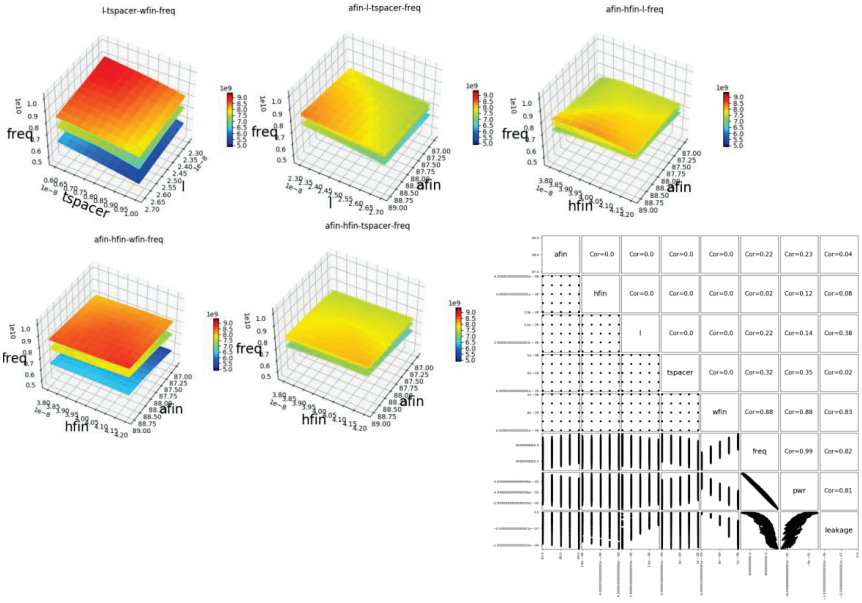
*Raw data outputs:*

| | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 1 | afin | tspacer | hfin | wfin | l | leakage | pwr | freq |
| 2 | 87 | 6.00E-09 | 3.80E-08 | 6.00E-09 | 2.30E-08 | -4.85E-08 | -4.04E-05 | 6439695400 |
| 3 | 87 | 6.00E-09 | 3.80E-08 | 7.00E-09 | 2.30E-08 | -1.43E-07 | -4.62E-05 | 7220518100 |
| 4 | 87 | 6.00E-09 | 3.80E-08 | 8.00E-09 | 2.30E-08 | -3.30E-07 | -5.11E-05 | 7846169320 |
| 5 | 87 | 6.00E-09 | 3.80E-08 | 9.00E-09 | 2.30E-08 | -5.89E-07 | -5.51E-05 | 8331151420 |
| 6 | 87 | 6.00E-09 | 3.80E-08 | 1.00E-08 | 2.30E-08 | -7.92E-07 | -5.83E-05 | 8703509000 |
| 7 | 87 | 7.00E-09 | 3.80E-08 | 6.00E-09 | 2.30E-08 | -4.83E-08 | -3.90E-05 | 6240174450 |
| 8 | 87 | 7.00E-09 | 3.80E-08 | 7.00E-09 | 2.30E-08 | -1.38E-07 | -4.42E-05 | 6960600350 |
| 9 | 87 | 7.00E-09 | 3.80E-08 | 8.00E-09 | 2.30E-08 | -3.23E-07 | -4.95E-05 | 7653802140 |
| 10 | 87 | 7.00E-09 | 3.80E-08 | 9.00E-09 | 2.30E-08 | -5.80E-07 | -5.33E-05 | 8125635030 |
| 11 | 87 | 7.00E-09 | 3.80E-08 | 1.00E-08 | 2.30E-08 | -7.90E-07 | -5.69E-05 | 8563809250 |
| 12 | 87 | 8.00E-09 | 3.80E-08 | 6.00E-09 | 2.30E-08 | -4.78E-08 | -3.74E-05 | 6012085830 |
| 13 | 87 | 8.00E-09 | 3.80E-08 | 7.00E-09 | 2.30E-08 | -1.37E-07 | -4.29E-05 | 6785101930 |
| 14 | 87 | 8.00E-09 | 3.80E-08 | 8.00E-09 | 2.30E-08 | -3.09E-07 | -4.64E-05 | 7245649850 |
| 15 | 87 | 8.00E-09 | 3.80E-08 | 9.00E-09 | 2.30E-08 | -5.68E-07 | -5.12E-05 | 7877538080 |
| 16 | 87 | 8.00E-09 | 3.80E-08 | 1.00E-08 | 2.30E-08 | -7.84E-07 | -5.52E-05 | 8383772990 |
| 17 | 87 | 9.00E-09 | 3.80E-08 | 6.00E-09 | 2.30E-08 | -4.70E-08 | -3.56E-05 | 5756667250 |
| 18 | 87 | 9.00E-09 | 3.80E-08 | 7.00E-09 | 2.30E-08 | -1.36E-07 | -4.15E-05 | 6585808900 |
| 19 | 87 | 9.00E-09 | 3.80E-08 | 8.00E-09 | 2.30E-08 | -3.06E-07 | -4.52E-05 | 7087165490 |
| 20 | 87 | 9.00E-09 | 3.80E-08 | 9.00E-09 | 2.30E-08 | -5.52E-07 | -4.89E-05 | 7582014990 |
| 21 | 87 | 9.00E-09 | 3.80E-08 | 1.00E-08 | 2.30E-08 | -7.73E-07 | -5.34E-05 | 8162388230 |
| 22 | 87 | 1.00E-08 | 3.80E-08 | 6.00E-09 | 2.30E-08 | -4.59E-08 | -3.37E-05 | 5472822210 |
| 23 | 87 | 1.00E-08 | 3.80E-08 | 7.00E-09 | 2.30E-08 | -1.32E-07 | -3.92E-05 | 6253432840 |
| 24 | 87 | 1.00E-08 | 3.80E-08 | 8.00E-09 | 2.30E-08 | -3.02E-07 | -4.39E-05 | 6907050910 |

*Axes*

*RO response*

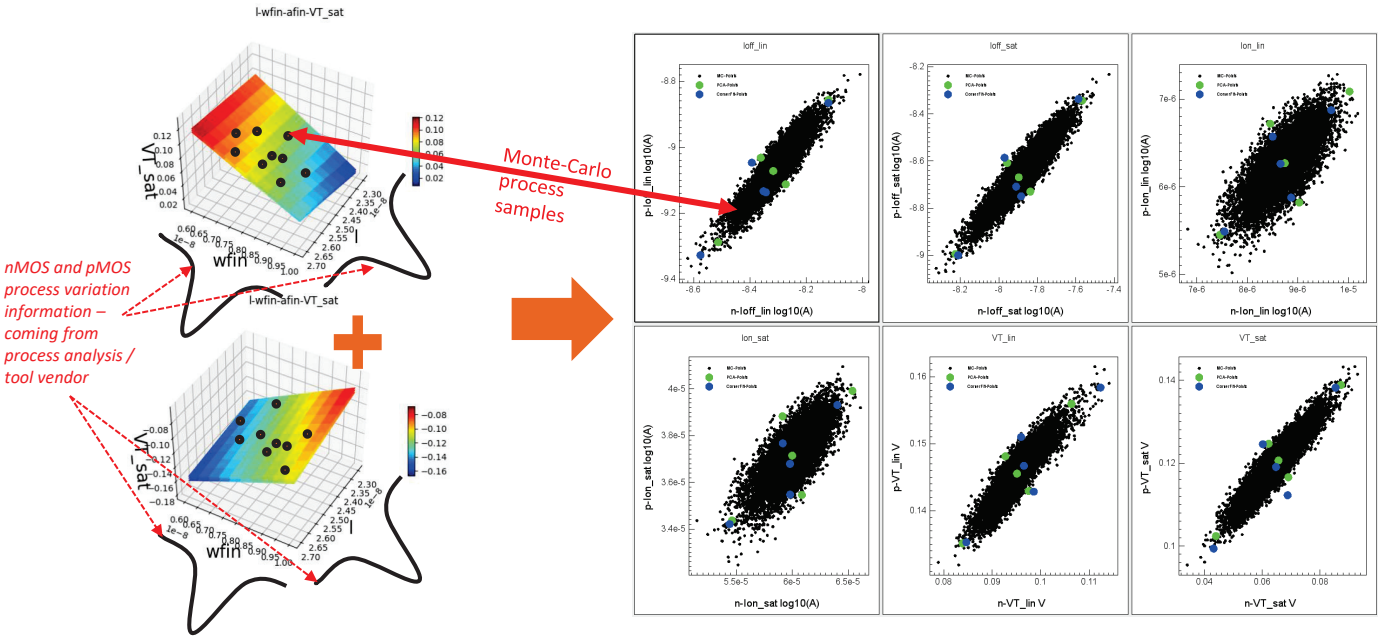
*3125 SPICE simulations*





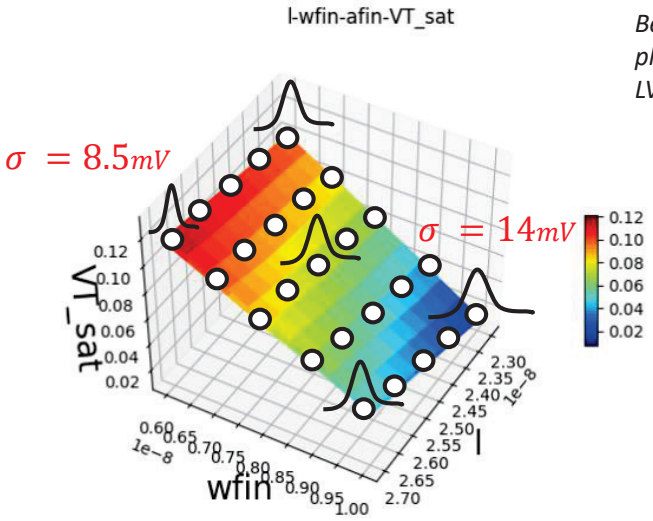

# Process corners

- Introduce Monte-Carlo process variation via RSM SPICE model.
  - Apply distributions to DoE axes
- Extract process corners based on expected variations.



# Local variation (LV) modelling

- Local variation simulations are performed across the DoE and added to the RSM using Garand (WP4)



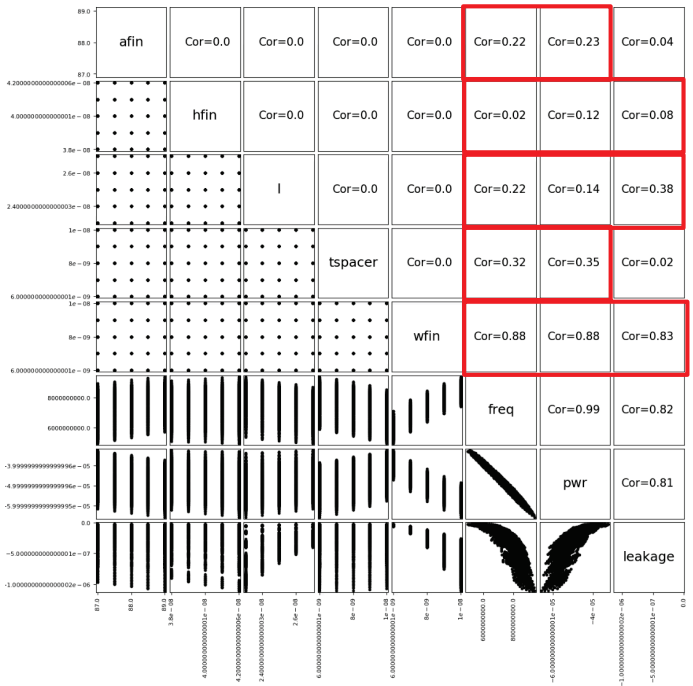

*Because LV data is underpinned by physical TCAD simulation we capture LV changes across the PV space.*

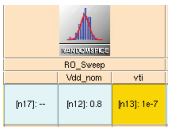






# RO Response Analysis



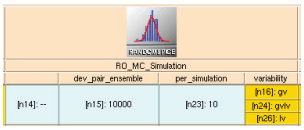




| | Frequency | Power | Leakage |
|---|---|---|---|
| Afin | Small | Small | None |
| Hfin | None | None | None |
| Lg | Small | None | Medium |
| Tspacer | Medium | Medium | None |
| Wfin | High | High | High |

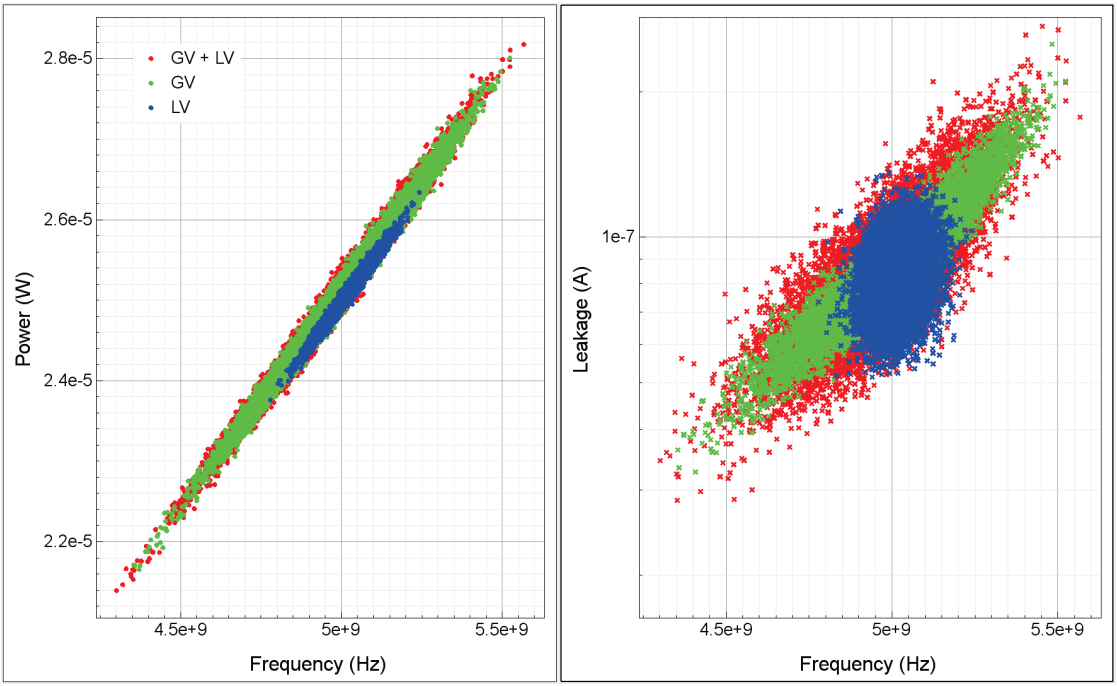
*Wfin dominates impact on RO response*

# RO Monte-Carlo response – Nfin =1

Individual and combined variability simulation results for nominal design point.



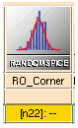

*Analysis with Nfin=1*








# RO Corner analysis

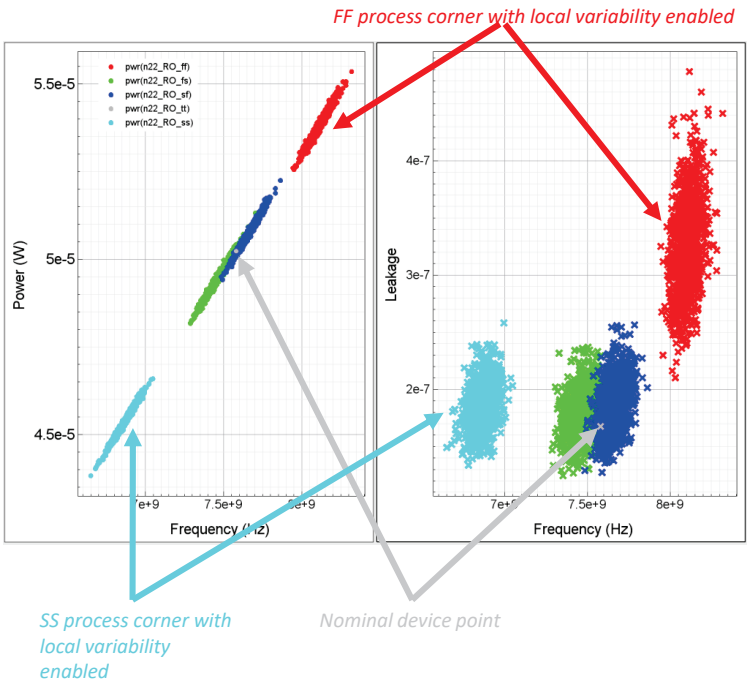



*Analysis run at Nfin=2*

From GV: FF to SS corner spread:
~ 1.6GHz

From GV+LV: FF to SS corner spread:
~ 1.6GHz

As previously seen, the global variation dominates the RO response



# Conclusions and Outlook

- Technology scaling is presenting increasing challenges
  - The relative impact of various factors is changing rapidly
  - DTCO is helping to address these challenges
- DTCO flows are, by nature, complex and require tightly integrated working practices and toolchains that support this.
- Developments during Superaid7 are helping to make true DTCO a reality
  - Project outputs are already part of commercialized software and flows