Leti-NSP model: SPICE model for advanced multigate MOSFETs

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Outline

- Introduction
- Innovative solution for SPICE modeling
- Quantum confinement and mobility models
- Model features
- Model validation
- Code and user’s manual
- Conclusion and outlook
Introduction

- Context: more Moore from International Roadmap for Devices and Systems

<table>
<thead>
<tr>
<th>YEAR OF PRODUCTION</th>
<th>2027</th>
<th>2030</th>
<th>2033</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic industry &quot;Node Range&quot; Labeling (nm)</td>
<td>7</td>
<td>7.5</td>
<td>8</td>
</tr>
<tr>
<td>IDM-Forecast node labeling</td>
<td>11-11.5</td>
<td>13-13.5</td>
<td>14-14.5</td>
</tr>
<tr>
<td>Logic device structure options</td>
<td>finFET</td>
<td>finFET</td>
<td>LGAA</td>
</tr>
<tr>
<td>Logic device mainstream device</td>
<td>finFET</td>
<td>LGAA</td>
<td>LGAA</td>
</tr>
</tbody>
</table>

LGAA = Vertically stacked NS/NW GAA MOSFET
VGAA = Vertical NS/NW GAA MOSFET

Advanced Gate All Around (GAA) MOSFET are introduced for sub-7nm nodes: require SPICE models for IC design

Introduction

- Challenges of GAA MOSFET modeling

1. GAA MOSFET can have different shapes: cylindrical, rectangular (sheet)
2. In the case of stack-GAA: the nanowires/nanosheets can have size differences
**Introduction**

- Our solution is Leti-NSP model dedicated to advanced multigate MOSFET.
- Leti-NSP model can simulate:
  - Vertically stacked GAA MOSFET (nanosheet and/or nanowire)
  - Vertical channel GAA MOSFET (nanosheet and/or nanowire)
  - FinFET / Trigate MOSFET

**Model’s core:** modeling of vertically stacked GAA is complex and challenging

- Main goals: find a compact formalism for
  - Accuracy: physical approach
  - CPU time efficiency: single instance

- Main difficulties:
  - the surface potential is not constant along the NW/NS perimeter
  - GAA can have different sizes: surface potentials are not the same for all GAA
Innovative Solution for SPICE Modeling

- Concept of Leti-NSP model: GAA MOSFET architecture and its asymptotic cases

- 2 asymptotic cases: Symmetrical double gate and cylindrical GAA MOSFET

Innovative Solution for SPICE Modeling

- Concept of Leti-NSP model: GAA MOSFET architecture and its asymptotic cases

1 - Unique model for these both asymptotic cases

2 - Solution for stacked-nanosheet GAA MOSFET and vertical GAA MOSFET
Innovative Solution for SPICE Modeling

- Asymptotic cases: unique equation (Poisson’s equation + boundary conditions)

\[
(x_g - x)^2 + \frac{4 \cdot \varepsilon_{si}}{H \cdot C'_{ox}} \cdot (x_g - x) = \delta \cdot \exp(x - x_n)
\]

See O. Rozeau et al, IEDM’16

Planar SDG

Cylindrical

Innovative Solution for SPICE Modeling

- Nanosheet GAA MOSFET partitioning

- Innovative solution in NSP model: an unique effective surface potential is obtained by the resolution of a unified equation for nanosheet
Innovative Solution for SPICE Modeling

- NSP-model can reproduced all GAA shapes without fitting parameters

![Gate capacitance graphs](image)

Case of stacked-nanosheet GAA MOSFET

\[
C'_{ox} = \sum_{i=1}^{N_W} \frac{W_i}{W_{total}} \cdot C'_{ox,i}
\]

\[
H = \sum_{i=1}^{N_W} \frac{W_i}{W_{total}} \cdot H_i
\]

\[
W_{total} = \sum_{i=1}^{N_W} W_i
\]

The inversion charge is accurately and analytically modeled without fitting parameters
Quantum Confinement and Mobility Models

- Case of stacked-nanosheet GAA MOSFET

![Graph showing gate capacitance vs. gate voltage for different channel widths (W=8nm, W=16nm, W=24nm) with classical TCAD simulations in blue and 2D Poisson-Schrödinger simulations in red.]

- Quantum confinement has a significant impact on the inversion charge.

![Diagram illustrating quantum confinement effects with simulations: TB_SIM. Details: Effective mass: 6 bands $k.p$ (higher than 10 sub-bands are solved).]

Quantum Confinement and Mobility Models

- Dedicated compact model for GAA MOSFET (IEDM'16)

- Triangular-potential approximation (Stern 72)

- Structural confinement has a stronger impact on $C_{inv}$ in GAA than in planar bulk MOSFET

![Graph showing gate capacitance vs. gate voltage with blue and red lines indicating classical Poisson equation and 2D Poisson-Schrödinger, respectively.]

- For Leti-NSP model: dedicated solution including accurate modeling of $C_{gg}$ slope without fitting parameter for the user.
Quantum Confinement and Mobility Models

- MODEL versus Simulations: Stacked-NS MOSFET (IEDM’16)

![Gate capacitance versus Gate voltage graph](image1)

- Single effective mass: defined as a function of device polarity, Si orientation and Ge concentration for pFET without fitting parameters for users

Quantum Confinement and Mobility Models

- Mobility partitioning in GAA MOSFET

- In NSP model, 2 distinct mobility models is implemented for inner part and outer parts

\[
\mu_{\text{inner}} = \frac{\mu_0}{1 + (f_{\muE} \cdot E_{\text{eff}})^{\theta_{\mu}} 
+ C_{\text{SS}} \cdot \left(1 + \frac{q_{\text{eff}}}{q_{\text{lith}}}\right)^{\theta_{\text{CS}}}}
\]

\[
\mu_{\text{outer}} = \frac{\mu_0}{1 + (f_{\muES} \cdot E_{\text{eff}})^{\theta_{\muS}} 
+ C_{\text{SS}} \cdot \left(1 + \frac{q_{\text{eff}}}{q_{\text{lith}}}\right)^{\theta_{\text{CSS}}}}
\]

- For model accuracy, quantum confinement is included in the inversion charge and electrical field calculations
Quantum Confinement and Mobility Models

- Model evaluation: nfet

Electrical field dependence

![Graph showing the electrical field dependence of nfet with symbols for experimental data and lines for the Leti-NSP model.](image)

Width dependence

![Graph showing the width dependence of nfet with symbols for experimental data and lines for the Leti-NSP model.](image)

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Quantum Confinement and Mobility Models

- Model evaluation: pfet

Electrical field dependence

![Graph showing the electrical field dependence of pfet with symbols for experimental data and lines for the Leti-NSP model.](image)

Width dependence

![Graph showing the width dependence of pfet with symbols for experimental data and lines for the Leti-NSP model.](image)
Overview of Model Features

- For all device sizes

**Model features: Leti-NSP model v1.0.0**

- Interface states
- Quantum mechanical effect (confinement)
- Channel doping effect
- Management of SiGe channel for pFET
- Mobility model including sidewall effects
- Temperature scaling and self-heating effect

### Quantum confinement modeling

- Gate capacitance (fF/µm²)
- Gate voltage (V)

### Mobility model including sidewall effects

- Mobility (cm²/Vs)
- Mobility model including sidewall effects

### Channel doping effect

- Threshold voltage roll-off
- L-scaling of mobility model
- Drain Induced Barrier Lowering
- Velocity saturation
- Channel length modulation in saturation
- Series resistances with bias dependence
Overview of Model Features

- Other parasitic effects

**Model features: Leti-NSP model v1.0.0**

- Inner and Outer fringe capacitances
- All external parasitic capacitances including device to substrate capacitances
- External access resistances
- Gate resistance with scaling effects
- Gate tunneling currents
- GIDL/GISL currents
- Junction currents and charges

Dedicated instance parameters for all GAA geometries

MODEL Validation

- **MODEL** versus TCAD simulations from Leti

Example of drain current and transconductance versus gate voltage

**Linear**

**Saturation**
Model Validation

- MODEL versus TCAD simulations from Leti

Example of drain current and drain conductance versus drain voltage

Note: other validations on hardware have been done but can’t show here (confidential)
Model Validation

- Leti-NSP model versus standard model requirements

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Leti-NSP</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical representation (currents, charges and derivatives)</td>
<td>√</td>
<td>See previous slides</td>
</tr>
<tr>
<td>2\textsuperscript{nd} and 3\textsuperscript{rd} continuous derivatives in all transitions and regimes</td>
<td>√</td>
<td>Checked</td>
</tr>
<tr>
<td>Symmetry and Gummel test</td>
<td>√</td>
<td>See next slide</td>
</tr>
<tr>
<td>Large signal analysis</td>
<td>√</td>
<td>By model itself</td>
</tr>
<tr>
<td>No model defects</td>
<td>√</td>
<td>Not detected</td>
</tr>
<tr>
<td>Model calculation efficiency</td>
<td>√</td>
<td>Optimized code</td>
</tr>
<tr>
<td>Physical and structurally meaningful model parameters</td>
<td>√</td>
<td>Physical model</td>
</tr>
<tr>
<td>Geometrical scaling</td>
<td>√</td>
<td>Done</td>
</tr>
<tr>
<td>Empirical parameters</td>
<td>√</td>
<td>Similar to PSP model</td>
</tr>
<tr>
<td>Model binning</td>
<td>√</td>
<td>Next release</td>
</tr>
<tr>
<td>Model extraction efficiency</td>
<td>√</td>
<td>Optimized and checked on</td>
</tr>
<tr>
<td></td>
<td></td>
<td>several extractions</td>
</tr>
<tr>
<td>Operating Point output</td>
<td>√</td>
<td>Done</td>
</tr>
</tbody>
</table>

Model Validation

- Leti-NSP mode: symmetry test at near to $V_{ds}=0\text{V}$

Gummel test is ok with all effects activated.
Code and User’s Manual

- Leti-NSP model: code and manual are available - ready for IC design

Conclusions and Outlook

- History:
  - Model development has been started in 2015
  - 6 versions were provided to our partners (use in PDK)
- For next releases, we plan to include:
  - binning parameters
  - noise models (Flicker, thermal and induced gate noise)
  - model for junction-less MOSFET (dev. on going)
  - non-quasi static effects
  - model for tunnel-FET (partially dev.)
- Leti-NSP model is available and compatible with the CMC requirement for standardization