Leti-NSP model: SPICE model for advanced multigate MOSFETs

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ESSDERC/ ESSCIRC Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”

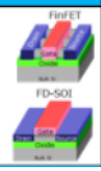
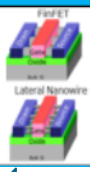
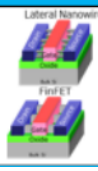
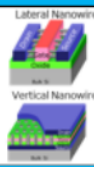
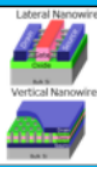
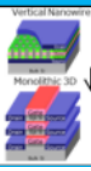
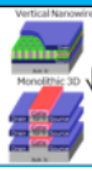
September 3, 2018, Dresden, Germany

Outline

- Introduction
- Innovative solution for SPICE modeling
- Quantum confinement and mobility models
- Model features
- Model validation
- Code and user’s manual
- Conclusion and outlook

Introduction

- Context: more Moore from International Roadmap for Devices and Systems

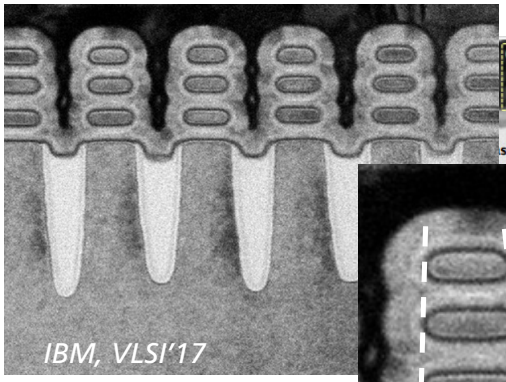
YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							
LGAA = Vertically stacked NS/NW GAA MOSFET *VGAA = Vertical NS/NW GAA MOSFET*							

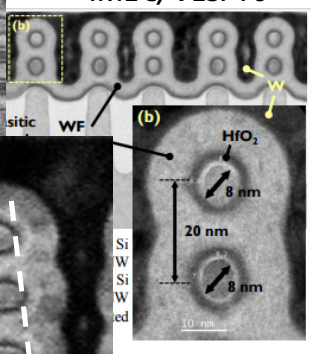
From irds.ieee.org: More Moore report 2017 edition

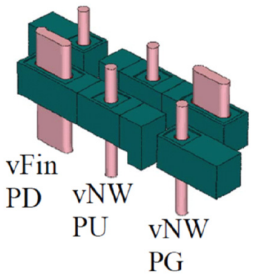
- Advanced Gate All Around (GAA) MOSFET are introduced for sub-7nm nodes: require SPICE models for IC design

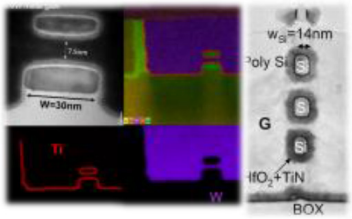
Introduction

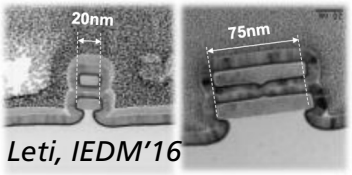
- Challenges of GAA MOSFET modeling

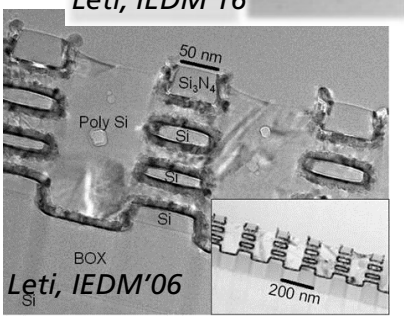








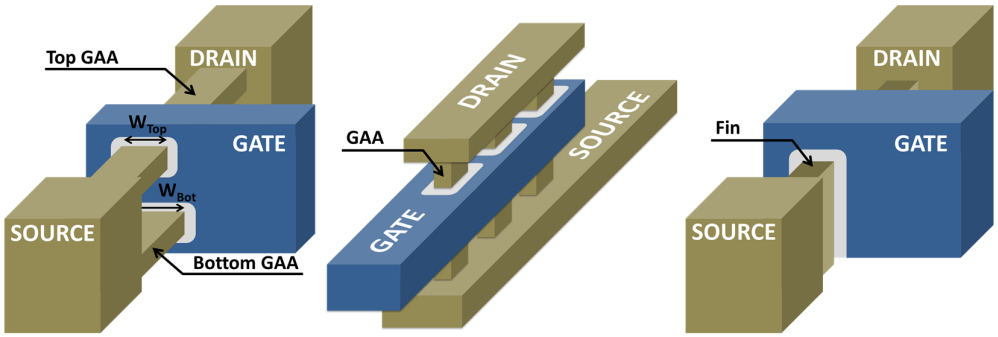




1. GAA MOSFET can have different shapes: cylindrical, rectangular (sheet)
2. In the case of stack-GAA: the nanowires /nanosheets can have size differences

Introduction

- Our solution is Leti-NSP model dedicated to advanced multigate MOSFET.
- Leti-NSP model can simulate:
  - Vertically stacked GAA MOSFET (nanosheet and/or nanowire)
  - Vertical channel GAA MOSFET (nanosheet and/or nanowire)
  - FinFET / Trigate MOSFET



Vertically stacked GAA MOSFET | *Vertical channel GAA MOSFET* | *FinFET/Trigate MOSFET*

Introduction

- Model's core: modeling of vertically stacked GAA is complex and challenging
- Main goals: find a compact formalism for
  - Accuracy: physical approach
  - CPU time efficiency: single instance
- Main difficulties:
  - the surface potential is not constant along the NW/NS perimeter
  - GAA can have different sizes: surface potentials are not the same for all GAA

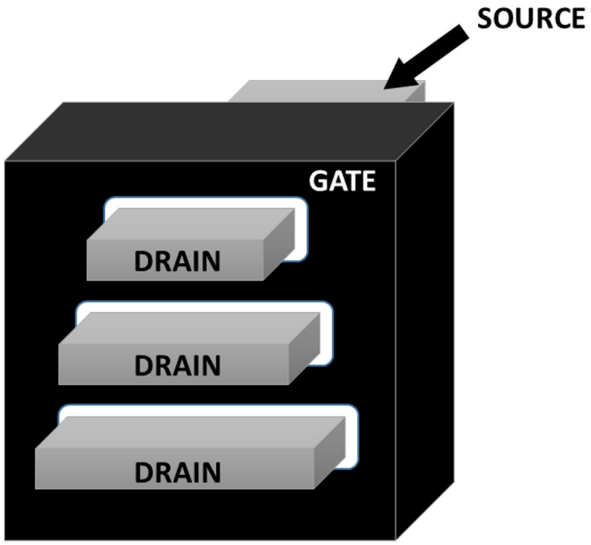
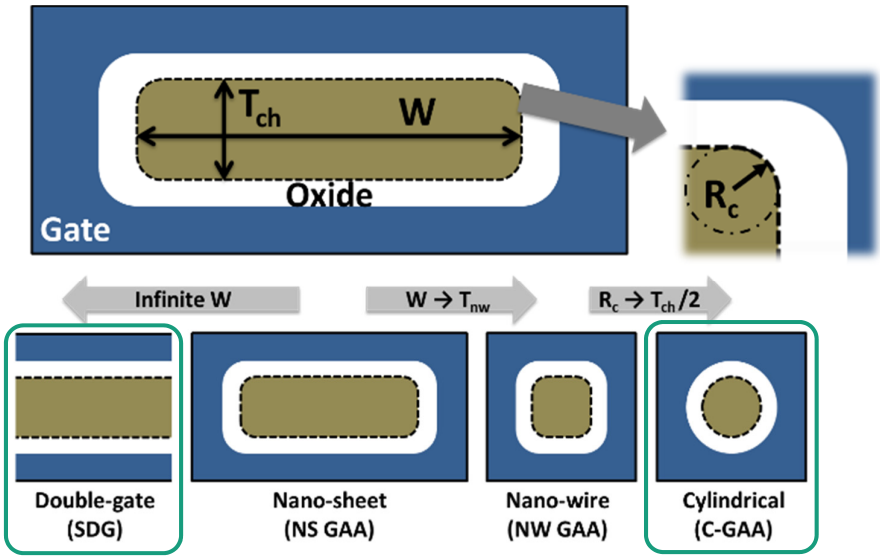


Illustration of vertically stacked GAA MOSFET: 3 Nanosheets

Innovative Solution for SPICE Modeling

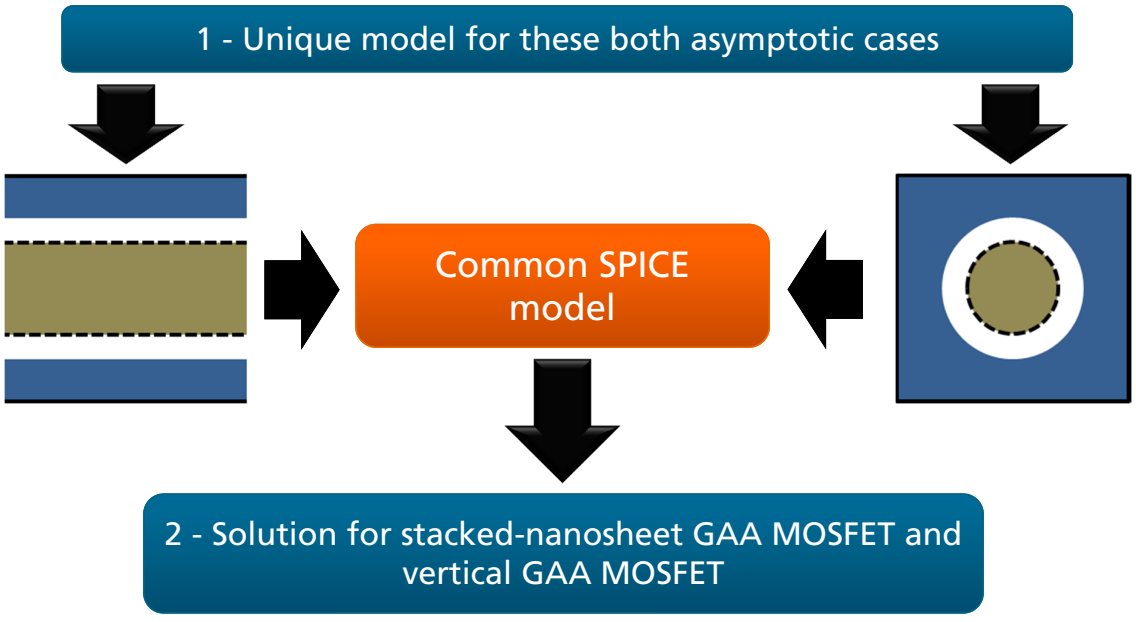
- Concept of Leti-NSP model: GAA MOSFET architecture and its asymptotic cases



- 2 asymptotic cases: Symmetrical double gate and cylindrical GAA MOSFET

Innovative Solution for SPICE Modeling

- Concept of Leti-NSP model: GAA MOSFET architecture and its asymptotic cases



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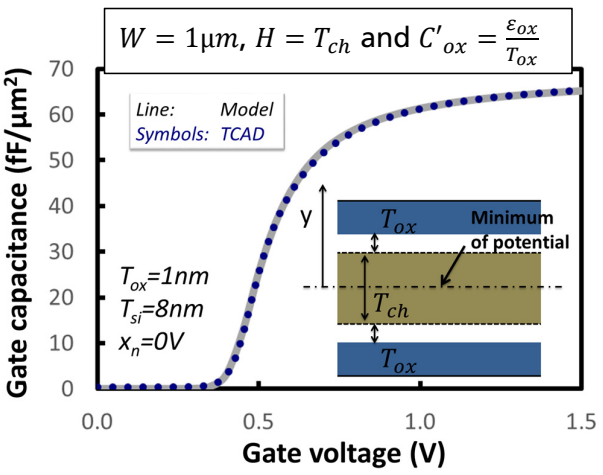
Innovative Solution for SPICE Modeling

- Asymptotic cases: unique equation (Poisson's equation + boundary conditions)

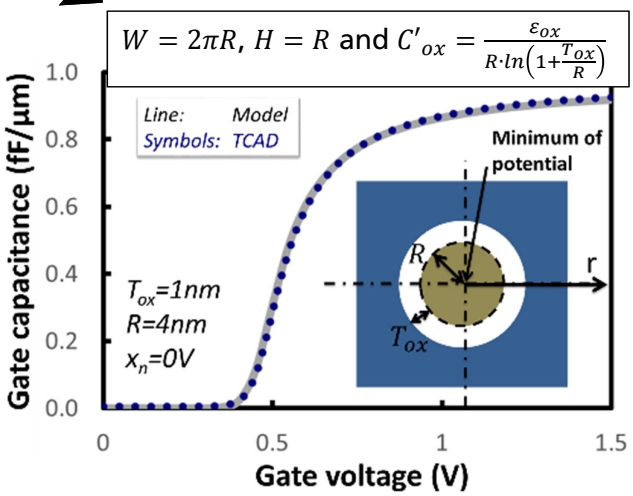
$$(x_g - x)^2 + \frac{4 \cdot \varepsilon_{si}}{H \cdot C'_{ox}} \cdot (x_g - x) = \delta \cdot exp(x - x_n)$$

See O. Rozeau et al, IEDM'16

Planar SDG

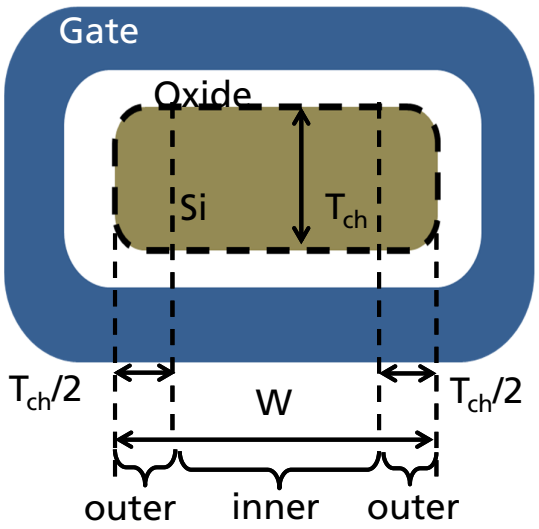


Cylindrical



Innovative Solution for SPICE Modeling

- Nanosheet GAA MOSFET partitioning



Outer parts: W_{outer} , $C'_{ox,outer}$, H_{outer}

Inner part: W_{inner} , $C'_{ox,inner}$

$$W_{eff} = W_{outer} + W_{inner}$$

$$H = \frac{W_{outer}}{W_{eff}} \cdot H_{outer} + \frac{W - T_{ch}}{W_{eff}} \cdot T_{ch}$$

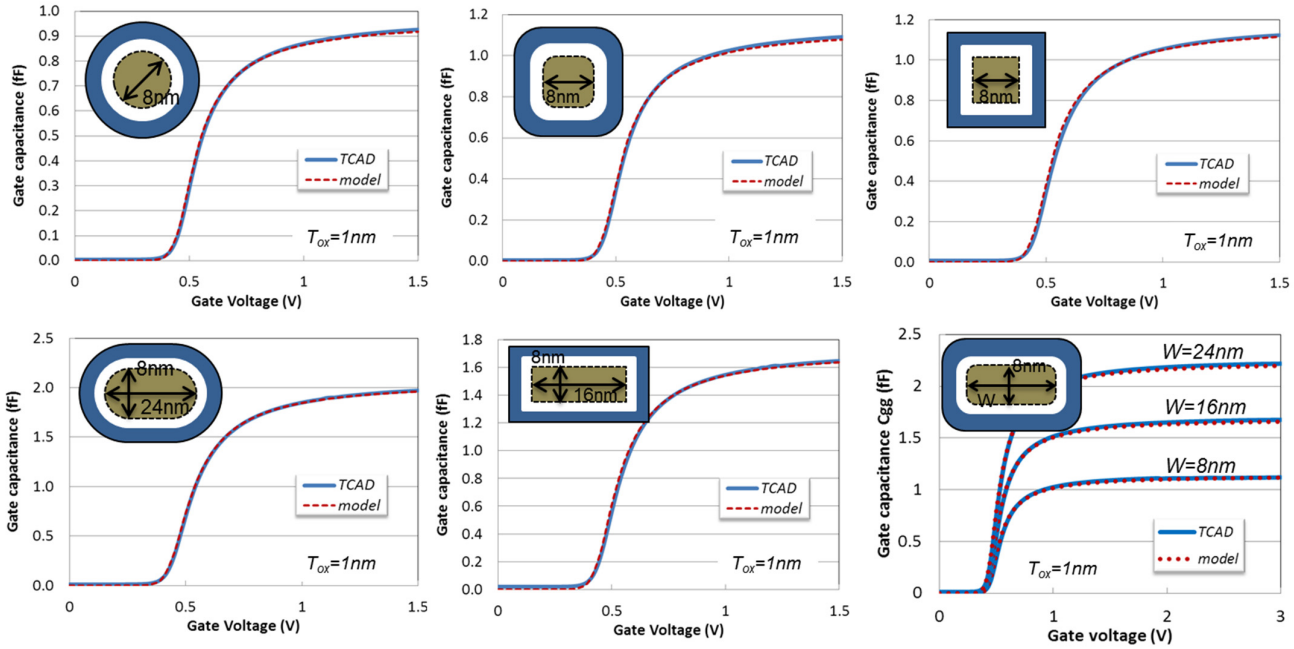
$$C'_{ox} = \frac{W_{outer}}{W_{eff}} \cdot C'_{ox,outer} + \frac{W - T_{ch}}{W_{eff}} \cdot C'_{ox,inner}$$

$$C'_{si} = \frac{\varepsilon_{si}}{H}$$

- Innovative solution in NSP model: an unique effective surface potential is obtained by the resolution of an unified equation for nanosheet

Innovative Solution for SPICE Modeling

- NSP-model can reproduced all GAA shapes <u>without</u> fitting parameters



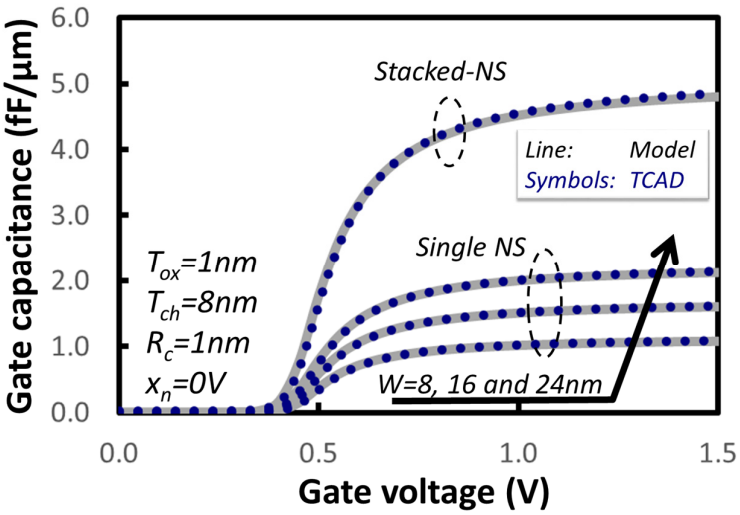
Innovative Solution for SPICE Modeling

- Case of stacked-nanosheet GAA MOSFET

$$\mathbf{C'_{ox}} = \sum_{\mathbf{i=1}}^{\mathbf{N_W}} \frac{W_i}{W_{total}} \cdot \mathbf{C'_{ox,i}}$$

$$\mathbf{H} = \sum_{\mathbf{i=1}}^{\mathbf{N_W}} \frac{W_i}{W_{total}} \cdot \mathbf{H_i}$$

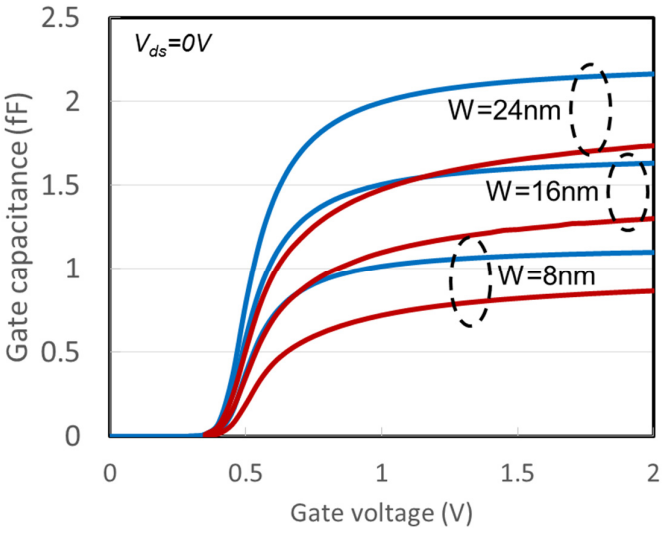
$$W_{total} = \sum_{\mathbf{i=1}}^{\mathbf{N_W}} W_i$$



- The inversion charge is accurately and analytically modeled <u>without</u> fitting parameters

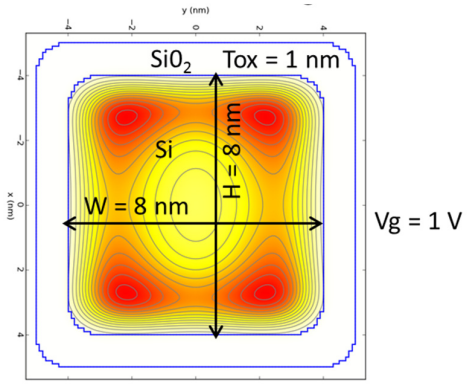
Quantum Confinement and Mobility Models

- Case of stacked-nanosheet GAA MOSFET



Blue: classical TCAD simulations

Red: 2D Poisson-Schrödinger



Simulations: TB_SIM

- Effective mass: 6 bands k.p (higher than 10 sub-bands are solved)

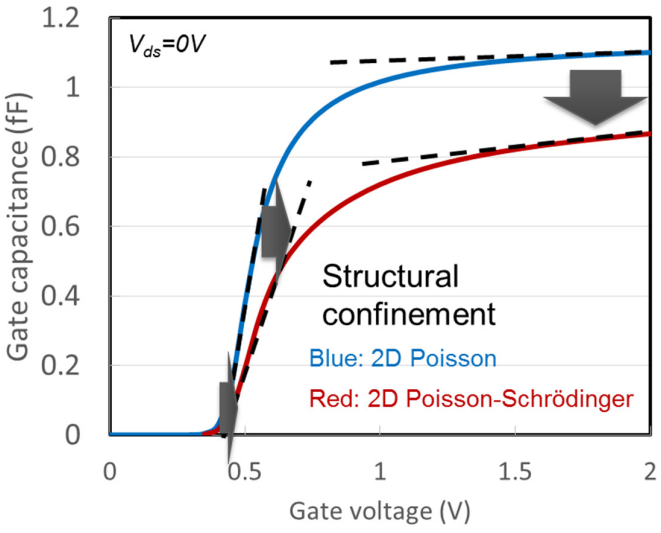
- Quantum confinement has a significant impact on the inversion charge

Quantum Confinement and Mobility Models

- Dedicated compact model for GAA MOSFET (IEDM'16)

- Triangular-potential approximation (Stern 72)

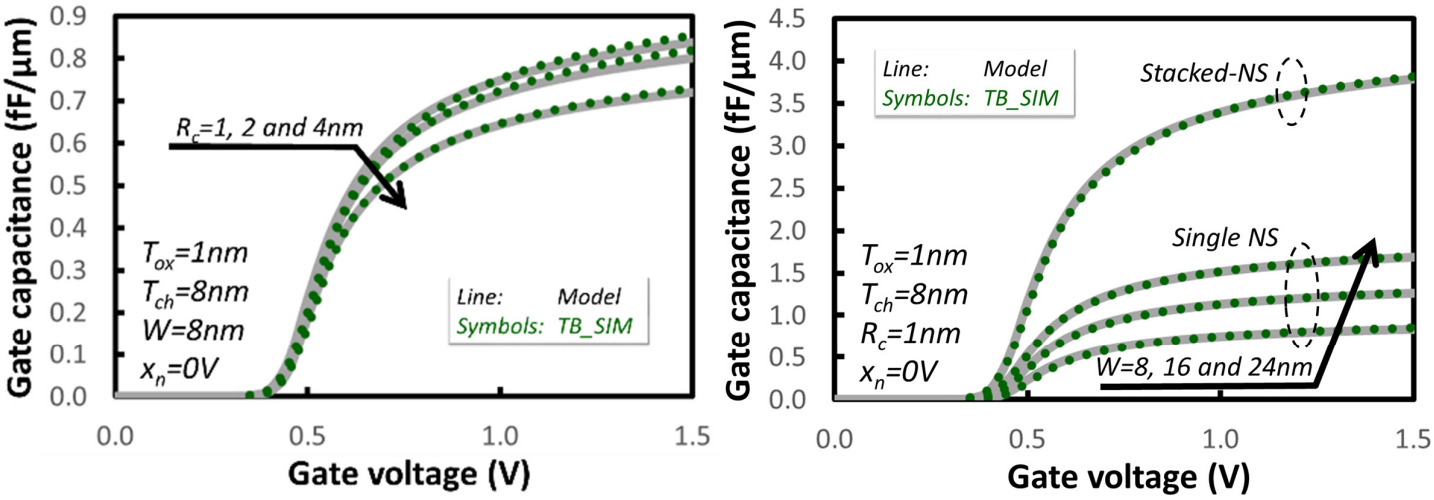
- Structural confinement has a stronger impact on C_{inv} in GAA than in planar bulk MOSFET



- For Leti-NSP model: dedicated solution including accurate modeling of Cgg slope without fitting parameter for the user

Quantum Confinement and Mobility Models

- MODEL versus Simulations: Stacked-NS MOSFET (IEDM'16)

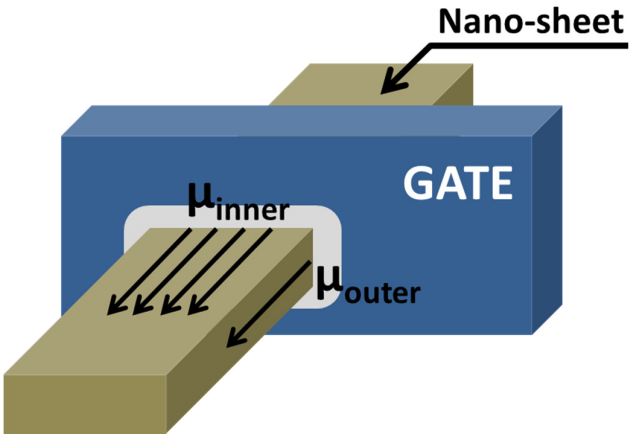


- Single effective mass: defined as a function of device polarity, Si orientation and Ge concentration for pFET <u>without fitting parameters</u> for users

Quantum Confinement and Mobility Models

- Mobility partitioning in GAA MOSFET

- In NSP model, 2 distinct mobility models is implemented for inner part and outer parts



$$\mu_{inner} = \frac{\mu_0}{1 + \left(f_{\mu E} \cdot E_{eff}\right)^{\theta_\mu} + C_S \cdot \left(1 + \frac{q_{ieff}}{q_{ith}}\right)^{-\theta_{CS}}}$$

$$\mu_{outer} = \frac{\mu_{0S}}{1 + \left(f_{\mu ES} \cdot E_{eff}\right)^{\theta_{\mu S}} + C_{SS} \cdot \left(1 + \frac{q_{ieff}}{q_{ith}}\right)^{-\theta_{CSS}}}$$

High field effect

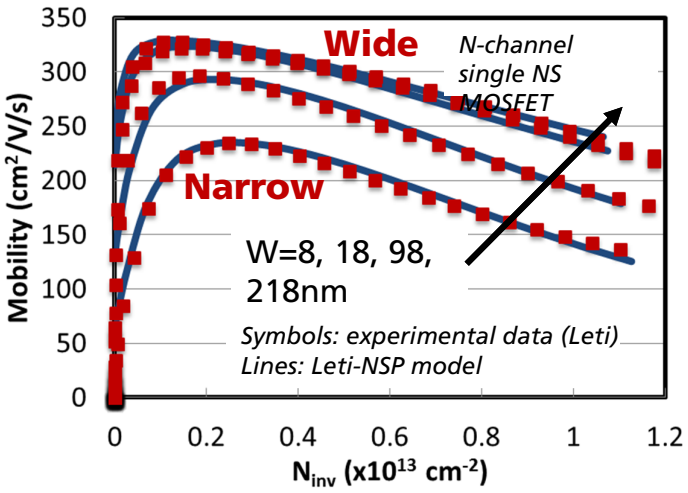
Coulomb scattering

- For model accuracy, quantum confinement is included in the inversion charge and electrical field calculations

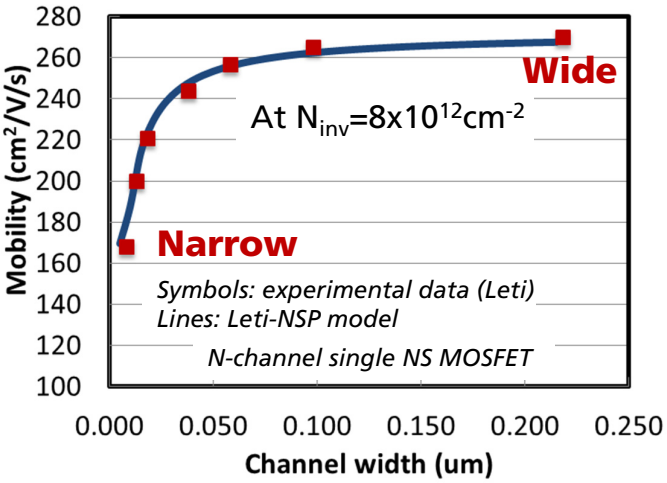
Quantum Confinement and Mobility Models

- Model evaluation: nfet

Electrical field dependence



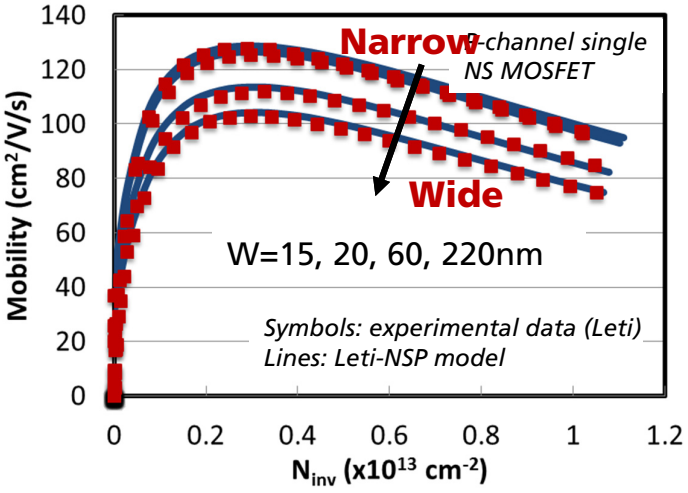
Width dependence



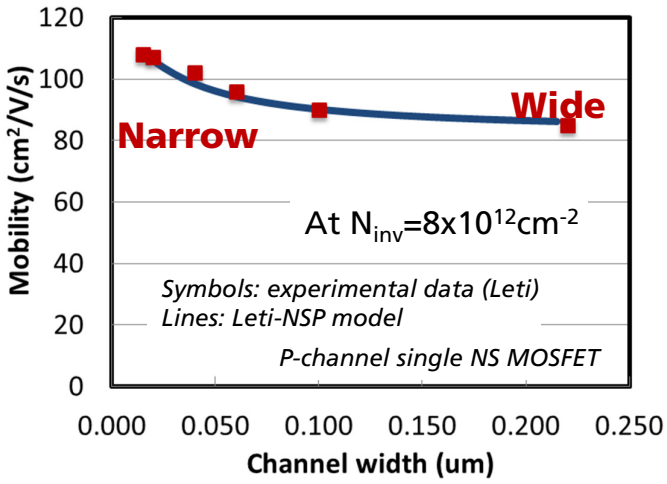
Quantum Confinement and Mobility Models

- Model evaluation: pfet

Electrical field dependence



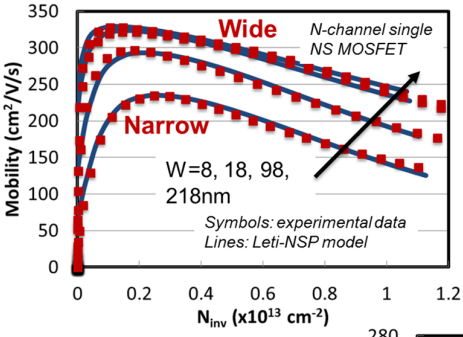
Width dependence



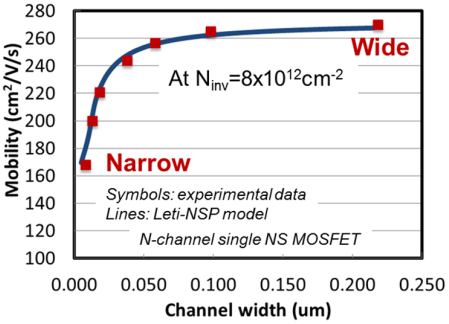
Overview of Model Features

- For all device sizes

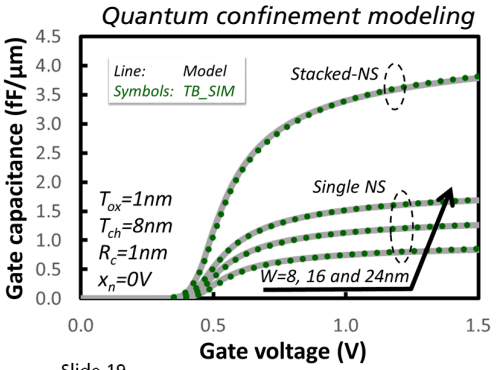
Model features: Leti-NSP model v1.0.0
Interface states
Quantum mechanical effect (confinement)
Channel doping effect
Management of SiGe channel for pfet
Mobility model including sidewall effects
Temperature scaling and self-heating effect



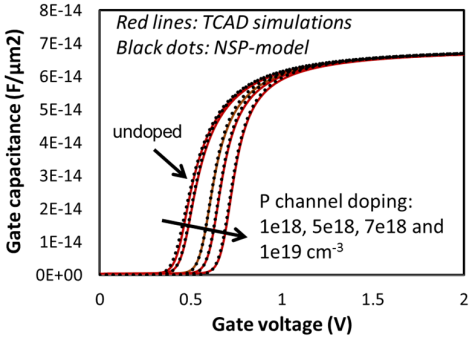
Mobility model including sidewall effects



Quantum confinement modeling



Channel doping effect



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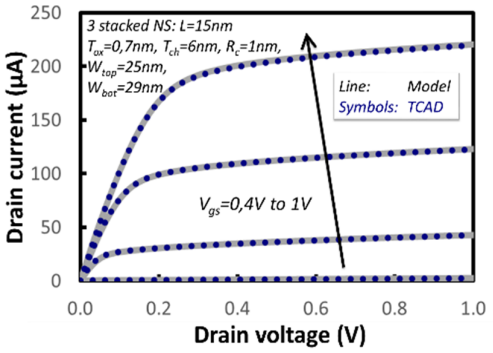
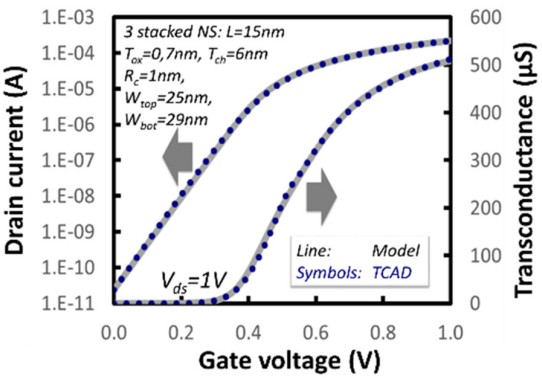
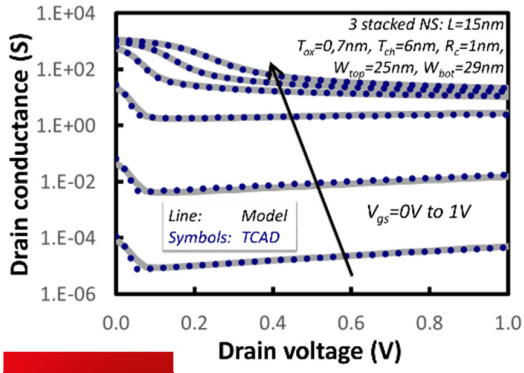
Overview of Model Features

- Short channel effects

Model features: Leti-NSP model v1.0.0
Threshold voltage roll-off
L-scaling of mobility model
Drain Induced Barrier Lowering
Velocity saturation
Channel length modulation in saturation
Series resistances with bias dependence







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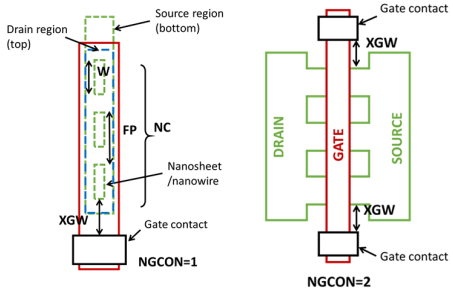
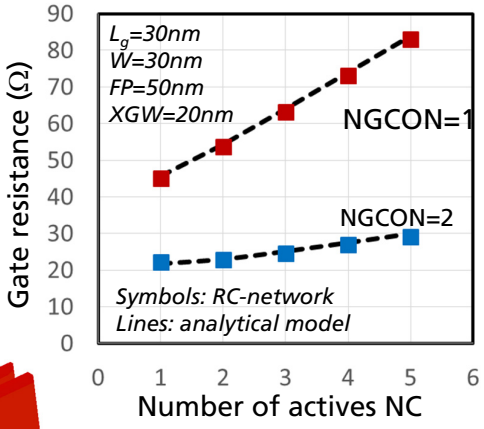
Overview of Model Features

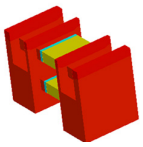
- Other parasitic effects

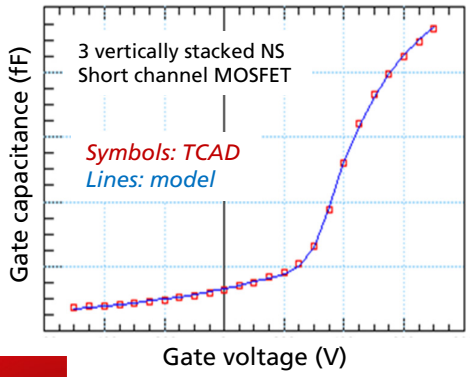
Model features: Leti-NSP model v1.0.0
Inner and Outer fringe capacitances
All external parasitic capacitances including device to substrate capacitances
External access resistances
Gate resistance with scaling effects
Gate tunneling currents
GIDL/GISL currents
Junction currents and charges

Dedicated instance parameters for all GAA geometries







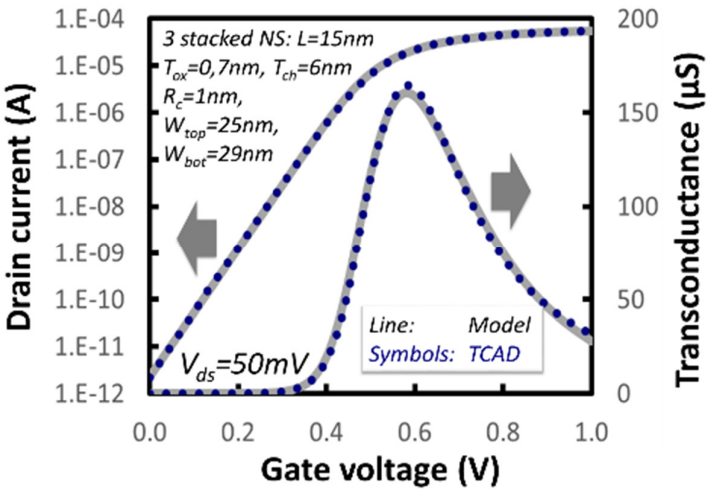


Model Validation

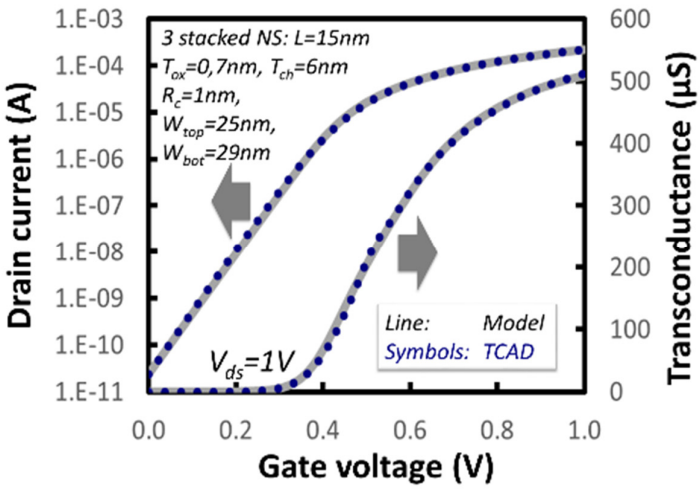
- MODEL versus TCAD simulations from Leti

Example of drain current and transconductance versus gate voltage

Linear



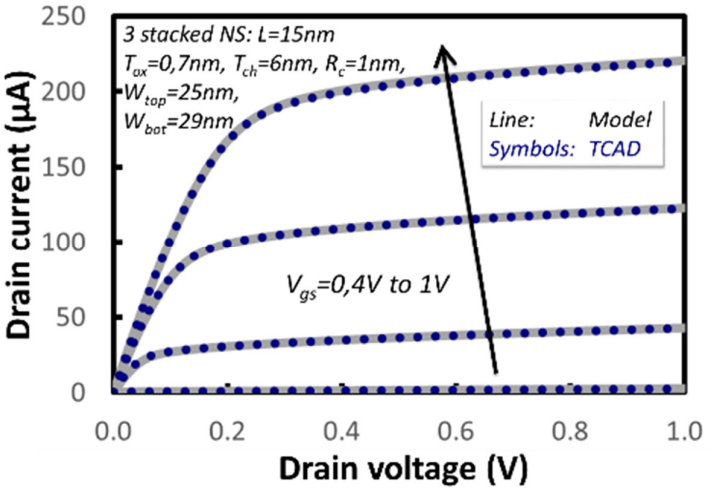
Saturation

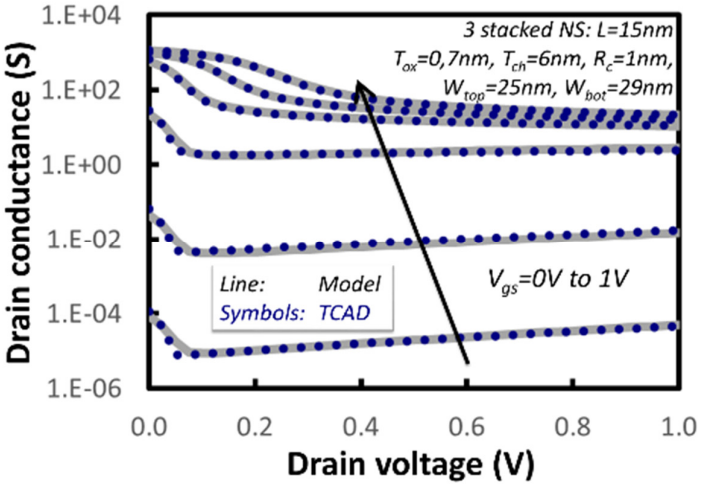


Model Validation

- MODEL versus TCAD simulations from Leti

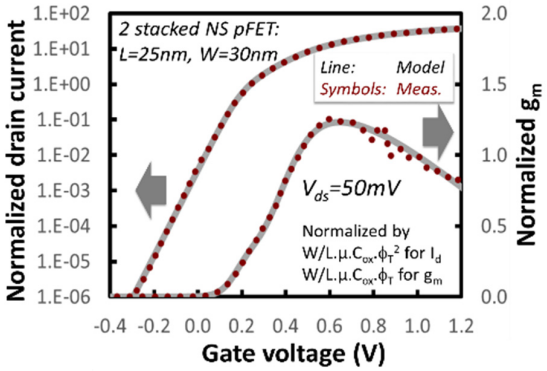
  Example of drain current and drain conductance versus drain voltage

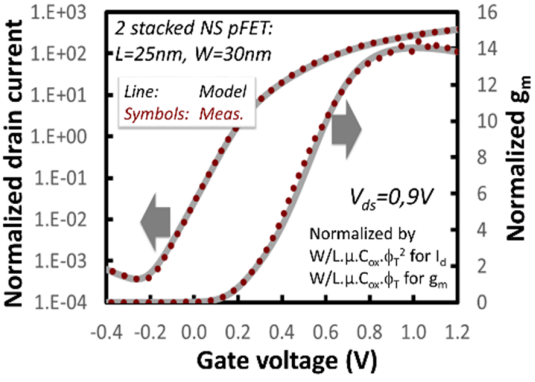


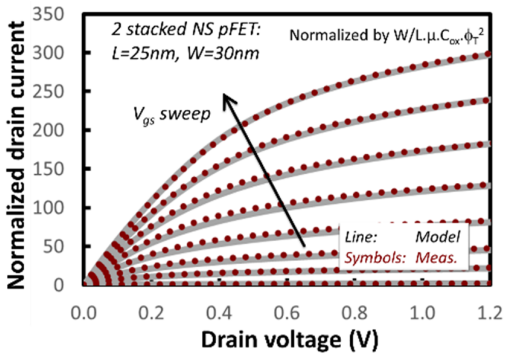


Model Validation

- Experimental data from Leti







Note: other validations on hardware have been done but can't show here (confidential)

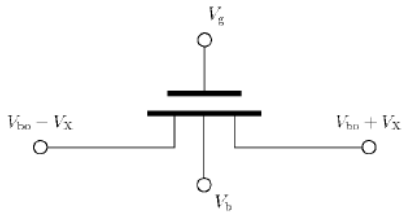
Model Validation

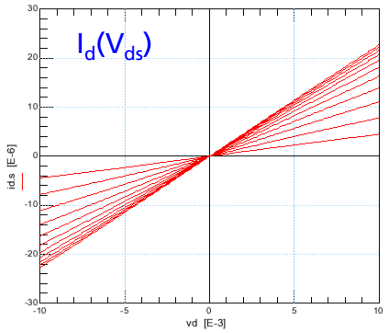
- Leti-NSP model versus standard model requirements

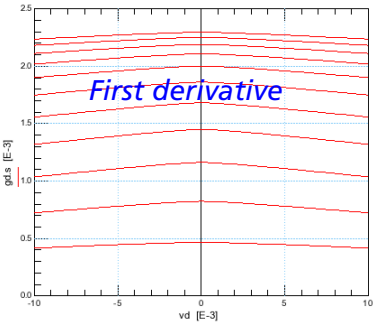
Requirements	Leti-NSP	Comments
Physical representation (currents, charges and derivatives)	√	See previous slides
2nd and 3rd continuous derivatives in all transitions and regimes	√	Checked
Symmetry and Gummel test	√	See next slide
Large signal analysis	√	By model itself
No model defects	√	Not detected
Model calculation efficiency	√	Optimized code
Physical and structurally meaningful model parameters	√	Physical model
Geometrical scaling	√	Done
Empirical parameters	√	Similar to PSP model
Model binning	√	Next release
Model extraction efficiency	√	Optimized and checked on several extractions
Operating Point output	√	Done

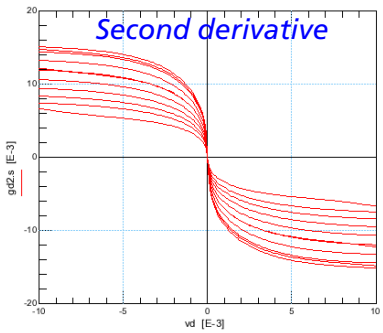
Model Validation

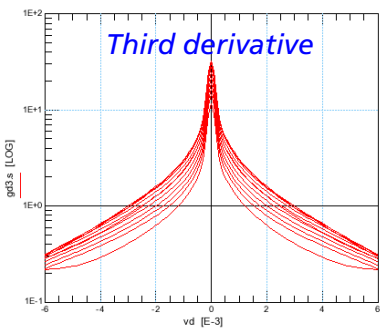
- Leti-NSP mode: symmetry test at near to V_{ds}=0V







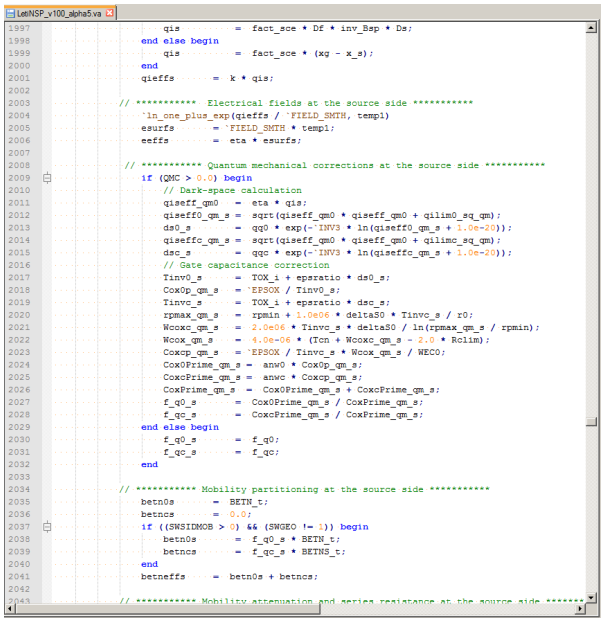




Gummel test is ok with all effects activated.

Code and User's Manual

- Leti-NSP model: code and manual are available - ready for IC design



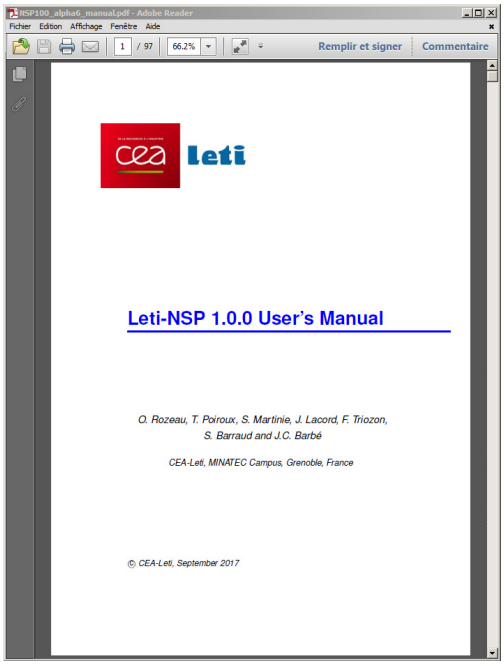
```
                qis          =  fact_sce * Df * inv_Bsp * Ds;
            end else begin
                qis          =  fact_sce * (xg - x_s);
            end
            qieffs       =  k * qis;

        // ********** Electrical fields at the source side **********
            `ln_one_plus_exp(qieffs / `FIELD_SMTH, temp1)
            esurfs       =  `FIELD_SMTH * temp1;
            eeffs        =  eta * esurfs;

        // ********** Quantum mechanical corrections at the source side **********
            if (QMC > 0.0) begin
                // Dark-space calculation
                qiseff_qm0   =  eta * qis;
                qiseff0_qm_s =  sqrt(qiseff_qm0 * qiseff_qm0 + qilim0_sq_qm);
                ds0_s        =  qq0 * exp(-`INV3 * ln(qiseff0_qm_s + 1.0e-20));
                qiseffc_qm_s =  sqrt(qiseff_qm0 * qiseff_qm0 + qilimc_sq_qm);
                dsc_s        =  qqc * exp(-`INV3 * ln(qiseffc_qm_s + 1.0e-20));
                // Gate capacitance correction
                Tinv0_s      =  TOX_i + epsratio * ds0_s;
                Cox0p_qm_s   =  `EPSOX / Tinv0_s;
                Tinvc_s      =  TOX_i + epsratio * dsc_s;
                rpmax_qm_s   =  rpmin + 1.0e06 * deltaS0 * Tinvc_s / r0;
                Wcoxc_qm_s   =  2.0e06 * Tinvc_s * deltaS0 / ln(rpmax_qm_s / rpmin);
                Wcox_qm_s    =  4.0e-06 * (Tcn + Wcoxc_qm_s - 2.0 * Rclim);
                Coxcp_qm_s   =  `EPSOX / Tinvc_s * Wcox_qm_s / WECO;
                Cox0Prime_qm_s =  anW0 * Cox0p_qm_s;
                CoxcPrime_qm_s =  anWc * Coxcp_qm_s;
                CoxPrime_qm_s  =  Cox0Prime_qm_s + CoxcPrime_qm_s;
                f_q0_s       =  Cox0Prime_qm_s / CoxPrime_qm_s;
                f_qc_s       =  CoxcPrime_qm_s / CoxPrime_qm_s;
            end else begin
                f_q0_s       =  f_q0;
                f_qc_s       =  f_qc;
            end

        // ********** Mobility partitioning at the source side **********
            betn0s       =  BETN_t;
            betncs       =  0.0;
            if ((SWSIDMOB > 0) && (SWGEO != 1)) begin
                betn0s       =  f_q0_s * BETN_t;
                betncs       =  f_qc_s * BETNS_t;
            end
            betneffs     =  betn0s + betncs;

        // ********** Mobility attenuation and series resistance at the source side *******
```



Leti-NSP 1.0.0 User's Manual

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Conclusions and Outlook

- History:
  - Model development has been started in 2015
  - 6 versions were provided to our partners (use in PDK)
- For next releases, we plan to include:
  - binning parameters
  - noise models (Flicker, thermal and induced gate noise)
  - model for junction-less MOSFET (dev. on going)
  - non-quasi static effects
  - model for tunnel-FET (partially dev.)
- Leti-NSP model is available and compatible with the CMC requirement for standardization